

# IEEE 1000BASE-T1 System Implementation Specification

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Version 1.6



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|-------------------|--|
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This specification provides general definitions and requirements for 1000BASE-T1 interfaces, which are intended to be used on automotive applications.

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## **2 Abbreviations**

|            |  |
|------------|--|
| <b>PHY</b> | PHY is a Physical layer interface device, often called transceiver |
| <b>ECU</b> | Electronic Control Unit – a device in a vehicle                    |

|                    |  |
|--------------------|--|
| <b>BIN</b>         | Bus Interface Network                                  |
| <b>OEM</b>         | Vehicle Manufacturer / Original Equipment Manufacturer |
| <b>CIDM</b>        | Characteristic Impedance Differential Mode             |
| <b>IL</b>          | Insertion Loss   |
| <b>RL</b>          | Return Loss  |
| <b>S-Parameter</b> | Scattering Parameter                                   |
| <b>TDR</b>         | Time Domain Reflectometry                              |
| <b>SCC</b>         | Standalone Communication Channel                       |
| <b>UTP</b>         | Unshielded Twisted Pair                                |
| <b>STP</b>         | Shielded Twisted Pair                                  |
| <b>EMC</b>         | Electromagnetic Compatibility                          |
| <b>PoDL</b>        | Power over Data Line                                   |
| <b>ESD</b>         | Electrostatic Discharge                                |
| <b>CMC</b>         | Common Mode Choke                                      |
| <b>SQI</b>         | Signal Quality Indication                              |
| <b>SNR</b>         | Signal Noise Ratio                                     |
| <b>SoC</b>         | System-On-Chip   |

### 3 Scope

The purpose of this document is to provide general definitions and requirements for 1000BASE-T1 interfaces, which are intended to be used on automotive applications.

The main focus of this document is to define a general set of requirements for qualification and testing purposes following the OPEN Alliance generated test specifications. The implementation of 1000BASE-T1 interface shall be applicable with the application notes of the semiconductor manufacturer of the specific PHY as DUT.

If a semiconductor manufacturer makes use of different approach for the implementation of 1000BASE-T1 interfaces, the semiconductor manufacturer must address this to their customers and find an appropriate alternative test approach. It is still recommended to use the same definitions for all tests. Some or even all OPEN Alliance tests specifications might be not applicable.

The same Bus Interface Network (BIN) shall be used for all tests of transceivers/ICs:

- EMC [7],
- Interoperability [6],
- Conformance (PMA [4], PCS [5] and PHY Control [3]).

This document describes one setup which is one working example within IEEE requirements; it is possible to establish many other solutions in full accordance with the IEEE requirements.

The System Implementation Specification does not describe a setup optimized for any specific goal.

100BASE-T1 System Implementation Specification shall be applied for 1000BASE-T1 PHYs operating at 100Mb/s.

Within the conformance tests there may be tests where the implementation of the BIN is not relevant. The specified implementation shall be used where necessary.

Communication systems using Power over Data Line (PoDL) or system implementation using STP cables are not covered by this specification.

Energy efficiency functionalities of 1000BASE-T1 PHYs are not covered by this specification.

Topics related to transmission speed changes from 1Gb/s to 100Mb/s or vice versa are out of the scope of this document.

## 4 Motivation

This document defines implementation of 1000BASE-T1 interfaces in automotive applications.

The requirements are valid for all kinds of transceivers which are intended to be used in automotive applications:

- Stand-alone transceiver (PHYs),
- Switches with integrated or separated transceiver cells and
- Integrated circuits (e.g. SoCs, SBCs, ASICs) with integrated transceiver cells.

This document contains requirements which shall be applied to passive components used for the BIN.

The respective definitions and requirements for system testing (ECU level qualification) are defined as well.

A transceiver (PHY or switch port) of a 1000BASE-T1 system implemented according to the above defined implementation shall fulfill the requirements defined in this specification.

All tests shall be conducted in an identical configuration of the transceiver and the associated components.

In the current document the following defined terminology convention applies. The usage of

- “Shall” expresses in the text a mandatory requirement.
- “Should” expresses in the text an optional requirement.
- “Must” expresses in the text a normative requirement.
- “Can” expresses in the text a permitted practice or method.

All tolerance values mentioned in this specification include initial tolerance, aging and temperature effects according to the application profile (service life, temperature profile) as specified in the Component Requirement Specifications of the affected components.

## 5 Normative references

- [1] IEEE P802.3bp™: Physical Layer Specifications and Management Parameters for 1 Gb/s Operation over a Single Twisted Pair Copper Cable
- [2] IEEE P802.3-2015 IEEE Standard for Ethernet
- [3] OPEN ALLIANCE: 1000BASE-T1 PHY Control Test Suite – Revision 1.0
- [4] OPEN ALLIANCE: 1000BASE-T1 Physical Media Attachment Test Suite – Revision 1.0
- [5] OPEN ALLIANCE: 1000BASE-T1 Physical Coding Sublayer Test Suite – Revision 1.0
- [6] OPEN ALLIANCE: 1000BASE-T1 Interoperability Test Suite – Revision 1.0
- [7] OPEN ALLIANCE: 1000BASE-T1 Transceiver EMC Specification – Revision 1.0
- [8] OPEN ALLIANCE: Automotive Ethernet ECU Test Specification Layer 1 1000BASE-T1 – Revision 1.0
- [9] OPEN ALLIANCE: Switch Semiconductor Test Specification, V1.0
- [10] OPEN ALLIANCE: 1000BASE-T1 Common Mode Choke Test Specification – Revision 1.0
- [11] OPEN ALLIANCE: 1000BASE-T1 Link Segment Type A (UTP) Channel and Components v2.0
- [12] OPEN ALLIANCE: 802.3bp Sleep/Wake-up Specification for Automotive Gigabit Ethernet – Revision 1.0
- [13] OPEN ALLIANCE: 1000BASE-T1 Advanced diagnostic features for automotive Ethernet PHYs – Revision 1.0
- [14] OPEN ALLIANCE: 1000BASE-T1 EMC Test Specification for ESD suppression devices – Revision 1.0
- [15] ISO / IEC 11801:2002 Information technology — Generic cabling for customer premises

## 6 Overview

This document includes three main chapters:

- Implementation for 1000BASE-T1, chapter 7  
This chapter defines the interface implementation for automotive applications together with requirements on components used to realize this BIN.
- 1000BASE-T1 testing requirements and system requirements, chapter 8  
This chapter defines further system requirements for systems implemented according to the system implementation.
- System test environment definition, chapter 9  
This chapter defines the system test environment, in which the transceiver as implemented system requirements shall be evaluated.

## 7 Implementation for 1000BASE-T1

### 7.1 General

For 1000BASE-T1 automotive Ethernet, it is recommended that the physical layer implementation of a BIN is implemented in accordance with this section of the Specification. All component ratings listed in this document shall be valid within the specified temperature range (e.g. -40°C ... +85°C / 105°C / 125°C) of the implemented system.

### 7.2 Interface circuitry definition

A 1000BASE-T1 interface is recommended to be implemented according to the requirements defined in IEEE P802.3bp™ [1] and as shown in this chapter, including Figure 1 and Table 1.

The interface consists of the Transceiver Block with transceiver supply decoupling and filtering, optional data-line filter and optional ESD protection and the BIN consisting of:

- Common mode choke (CMC)
- DC block capacitors
- Common mode termination network
- Optional ESD protection device

The ECU connector is also a part of the interface.

All interface components should be selected in accordance with the data sheets and application notes of the semiconductor manufacturer, as well as OEM's qualification requirements. The optimized BIN circuit is defined by the semiconductor manufacturer, and in accordance with the IEEE and various other requirements, which includes e.g. OEMs' qualification requirements.

All components of the 1000BASE-T1 interface are recommended to be implemented as required in this chapter and in chapter 7.3.

The layout and the configuration, including the schematic, of the transceiver interface shall be reviewed by the semiconductor manufacturer.

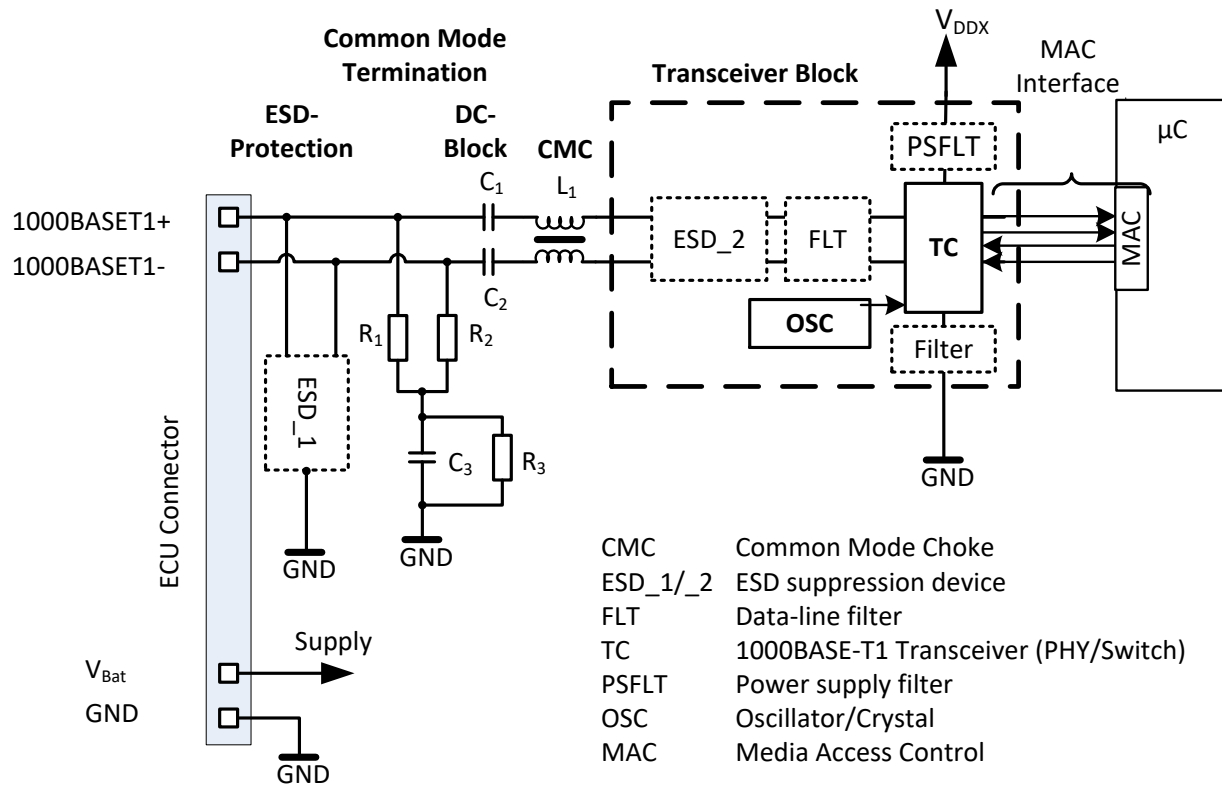
For layout design information of a specific system implementation the application notes of semiconductor manufacturers shall be considered.

If configuration of the transceiver by software is necessary (i.e. configuration script), this is also recommended to be implemented according to the application notes of the semiconductor manufacturers. The layout and the configuration of the transceiver shall be reviewed by the semiconductor manufacturer.

An exemplary documentation for the used circuitry in a test documentation is provided in appendix chapter 10.1.

Note:

For short start up time it is recommended to e.g. use hardware strap-in pins for PHY configuration.



**Figure 1 An example of a typical UTP interface circuitry/schematic for 1000BASE-T1.**

Figure 1 can be used as reference and guideline for the ECU developments. Deviations from the schematic in Figure 1 are allowed, in particular for grounding concepts, for example, other grounding concepts might be required in case of shielding. Correspondingly, PoDL implementations would require a different circuit.



| Ref   | Part   | Remarks  |
|---|--|--|
|   | <b>Transceiver Block</b>   | The transceiver block (transceiver including the optional ESD protection device (ESD_2) and data-line filter (FLT) according to application notes) has to fulfill the requirements of the OPEN Alliance specifications (refer to [IEEE802.3bp]) <sup>1</sup> . |
| L1  | <b>Common mode choke</b>   | Has to fulfill the requirements according to [10].   |
| C <sub>1</sub> , C <sub>2</sub>   | <b>Capacitor</b><br>100nF<br><b>Tolerance</b><br>≤ 10%<br><b>voltage range</b> <sup>2</sup><br>≥ 50V |  |
| R <sub>1</sub> , R <sub>2</sub>   | <b>Resistor</b><br>1kOhm<br><b>Tolerance</b><br>≤ 0,5% (even after ESD test)                         | Common Mode Termination circuitry: The resistors need sufficient power rating.   |
| C <sub>3</sub>  | <b>Capacitor</b>   | Common Mode Termination circuitry: The capacitor needs sufficient dielectric-strength. The capacitance value in accordance to semiconductor manufacturers' application notes.  |
| R <sub>3</sub>  | <b>Resistor</b>  | To avoid static charge of the cable harness<br>The resistance value in accordance to semiconductor manufacturers' application notes.   |
| ESD_1   | <b>ESD protection device</b>   | Optional.<br>The ESD protection device in accordance to semiconductor manufacturers' application notes.  |
|   | <b>ECU connector</b>   | It must fulfill the requirements according to [11]. Further requirements and information can be found in chapter 6.3.3.  |
| <p><sup>1</sup> It is required to follow the definitions of semiconductor manufacturer for external passive components and circuit, software configuration (script) and software flow definitions, which are defined in data sheets and application notes.</p> <p><sup>2</sup> According to car manufacture specifications for supply voltages ≥56V voltage range for 48V electrical systems, typically 100V min. electric strength recommended for ceramic caps. For 12V systems typ. 50V electrical strength is enough. .</p> |  |  |

**Table 1: An example of typical interface component requirements.**

### 7.3 Requirements for 1000BASE-T1 ECU interface components

The components used in a 1000BASE-T1 interface implementation shall fulfill the following requirements. The testing requirements are described in chapter 8.2.

#### 7.3.1 1000BASE-T1 Transceivers (standalone or integrated in switch)

All transceivers (PHYs or Switches) used in a 1000BASE-T1 interface shall comply with IEEE P802.3bp™ [1].

##### 7.3.1.1 Transceiver functional requirements

All transceivers (PHYs or Switches) used in a 1000BASE-T1 interface shall be tested according to the following requirements:

- The PHY/switch shall support test modes according to [1].
- The PHY/switch shall support a mode which deactivates all signaling on the BIN, while the BIN termination is still active (e.g. called "TX\_off" or "scrambler\_off").
- The PHY/switch shall provide link status information via a register, according to [2].
- The PHY/switch shall provide a communication\_ready status information via a register, according to [13].
- The PHY/switch shall provide information on CRC or symbol failures on physical layer level via a register.
- The PHY/switch shall be able to detect a short between bus lines and provide this information via a register according to [13].
- The PHY/switch shall be able to detect interruptions of bus lines and provide this information via a register according to [13].
- The PHY/switch shall be able to correct the polarity and provide this information via a register.
- The PHY/switch shall provide link quality information (e.g. SQI based on SNR) via a status register according to [13].
- The PHY/switch shall provide Forward Error Correction (FEC) counter via a status register according to [13].

If one of the above is not fulfilled a reason/substitution for this shall be documented. An exemplary documentation is provided in chapter 10.2.

### **7.3.1.2 Transceiver conformance, EMC and interoperability requirements**

All transceivers (PHYs or Switches) used in a 1000BASE-T1 interface shall be conformant to 1000BASE-T1 according to the following test specifications:

- OPEN ALLIANCE: 1000BASE-T1 PHY Control Test Suite – Revision 1.0 [3]
- OPEN ALLIANCE: 1000BASE-T1 Physical Media Attachment Test Suite – Revision 1.0 [4]
- OPEN ALLIANCE: 1000BASE-T1 Physical Coding Sublayer Test Suite – Revision 1.0 [5]
- OPEN ALLIANCE: 1000BASE-T1 Interoperability Test Suite – Revision 1.0 [6]
- OPEN ALLIANCE: 1000BASE-T1 Transceiver EMC Specification – Revision 1.0 [7]

Further details of this test are described in chapter 8.2.

### **7.3.1.3 Evaluation/testing capabilities for integrated circuits**

To allow evaluation, 1000BASE-T1 Test Mode functionality with Test Modes 1 to 5 [1] shall be implemented for each 1000BASE-T1 interface of the tested integrated circuit.

The tested integrated circuit shall be able to deactivate data transmission ("SEND\_Z", e.g. "TX off" or "Scrambler off") of each 1000BASE-T1 interface. See also chapter 8.4.3 (Evaluation/testing capabilities).

Note:

This is to allow MDI return loss and MDI Mode conversion reflection test with proper termination inside the transceiver (i.e. 100 Ω).

### **7.3.1.4 Further transceiver requirements**

Further qualification of transceivers on system level shall be done according to [7] and [9].

### 7.3.2 Common mode choke for 1000BASE-T1 interfaces

All CMCs used in a 1000BASE-T1 interface shall be tested according to [10].

The requirements of the CMC Test Specification (recommended values in the appendix C of [10]) are mandatory.

### 7.3.3 ECU connectors for 1000BASE-T1 interfaces (MDI interface)

The complete channel as well as all individual components (cables and connectors as well as assembled cable harness) of a 1000BASE-T1 link shall fulfill the channel requirements according to [11]. Therefore all components of the link shall be designed and assembled to ensure the required RF parameters.

The ECU connector implementation as well as the MDI Test Head shall fulfill the connector requirements of [11].

### 7.3.4 ESD elements

A landing pad according to the transceiver's application note for an optional ESD element shall be on the interface layout.

The ESD element can either be placed in the transceiver block or directly in front of the CMC – as shown in Figure 1.

An ESD element placed between connector and CMC has to fulfill the requirements defined in [14].

### 7.3.5 Clock tolerance requirements

A typical clock source with 25MHz is used for clock generation, its tolerance shall be less than  $\pm 100\text{ppm}$  ( $\pm 0.01\%$ ) (1000BASE-T1 link start-up is very sensitive to clock tolerances). For details refer to the transceiver's application notes.

The clock tolerance requirement  $\leq \pm 100\text{ppm}$  shall be fulfilled including aging and temperature effects.

## 7.4 Recommendation for pinout

A recommendation for pinout rules on 1000BASE-T1 ICs and ECU connector shall ensure that later system implementation allows:

- harmonized wiring schemes
- connection in the application as well as during test and debug
- working with 100BASE-T1 PHYs using the defined 100BASE-T1 option of 1000BASE-T1 PHYs
- PCB layout and geometrical hardware setup for good EMC results and good transmission behavior.

Note:

Connectors are vendor specific and may not match with connectors from different vendors.

Note:

ICs are vendor specific and may have different packages and pinout for each semiconductor manufacturer.

A potential layout may have the structure as shown in Figure 2. The layout shows a straight connection from the 1000BASE-T1 bus pins toward the connector. For this all components are placed on the top side of the PCB. This is the most natural placement of the connectors, but also for CMC and the IC.

PCB layout is an important topic in order to meet the EMC and MDI requirements defined in [4], [6], [8] and [14].

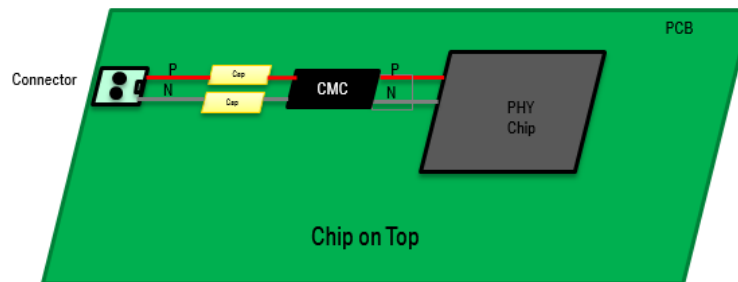


Figure 2: Example PCB arrangement – 3-D Top View

The shown PCB arrangement reflects a typical arrangement of IC pinout and EMC test boards of 100BASE-T1 and 1000BASE-T1 ICs.

Main goal of the recommendation is that in any case a direct, on to one non-crosses wiring harness can be used in conjunction with the connector system needed for 1000BASE-T1.

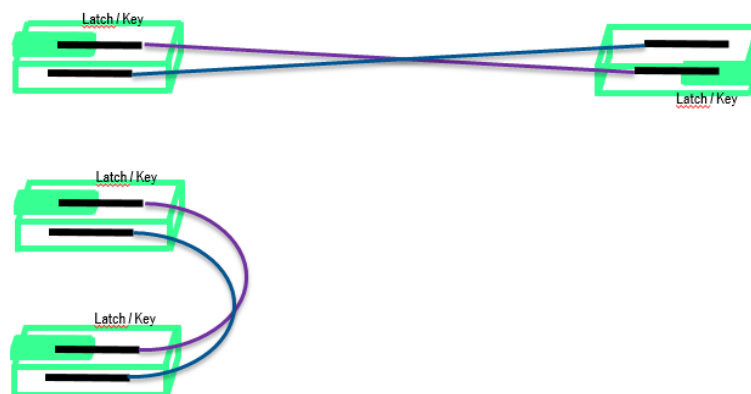


Figure 3: Example one to one direct cable assembly

Note:

At each side of the wiring harness the assignment of the according wire is the same.

### 7.4.1 1000BASE-T1 Transceivers (standalone)

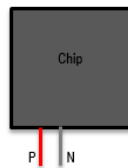
It is recommended that 1000BASE-T1 Transceivers (standalone) continue to use the scheme in clockwise direction when observing the IC from the top side.

|              |
|--------------|
| -1000BASE-T1 |
| +1000BASE-T1 |

Note:

Name may vary for different semiconductor manufacturers: Eth-/Eth-; Eth\_N/Eth\_P; Bus\_N/Bus\_P; -/+; N/P.

Figure 4 shows a recommended pin arrangement:



**Figure 4: Example Top view PHY IC**

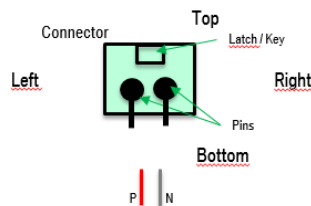
### 7.4.2 1000BASE-T1 ECU connectors

It is recommended to use a harmonized assignment of connector pins according to the differential bus signals. A recommended approach is to use the scheme below according to the layout example shown in Figure 4 and the recommended IC pinout.

For a 90° PCB header the recommended definition is:

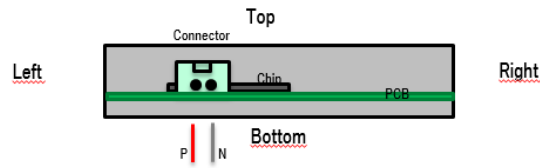
|              |            |
|--------------|------------|
| -1000BASE-T1 | Right side |
| +1000BASE-T1 | Left side  |

When viewed from the front; the PCB header place at top of the PCB is shown in Figure 5.



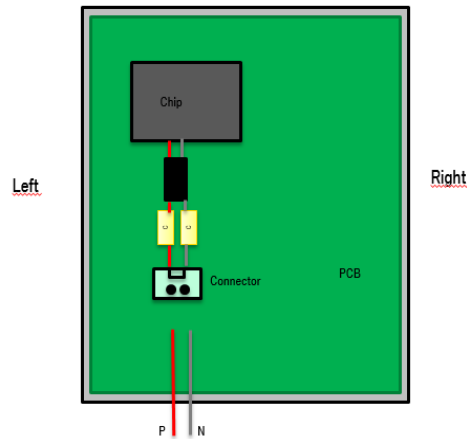
**Figure 5: Example Front View 90° PCB Connector**

The result of this approach is shown in Figure 6 for a 90° PCB Header in a single port application:



**Figure 6: Example Front View ECU 90° PCB Connector**

The result of this approach shown in Figure 7 for an implementation with connectors integrated in the top housing of an ECU.



**Figure 7: Example Top View ECU Straight Connector (-press fit,...)**

### 7.4.3 Multi-port connector

If there are more differential ports implemented in the same mechanical housing of a connector, the scheme for arrangement shall be maintained in the same way as described in 7.4.2. The reference point is according to the orientation mechanism of the connector system. In the example in Figure 5 the “latch / key” shows this requirement in a symbolic form.

### 7.4.4 1000BASE-T1 switches and multi-port transceivers

It is recommended to use the definition for connector pinout in the same strict manner for 1000BASE-T1 switches and multi-port transceivers as for standalone single channel transceivers.

The pinout of the ICs might be influenced by many parameters and the recommended pin arrangement might not be applicable.

#### 7.4.5 1000BASE-T1 auto polarity detection and correction

It is mandatory to use *Auto Polarity Detection and Polarity Correction* feature defined in [1] for 1000BASE-T1 implementation.

Note:

When using the 100BASE-T1 operation mode of a 1000BASE-T1 device, Auto Polarity correction is only an optional feature at 100BASE-T1 devices and not covered by the IEEE802.3 specification for these devices.

Note:

The device configured as slave device does the polarity correction.

## 8 1000BASE-T1 testing requirements and system requirements

### 8.1 General

A transceiver (PHY or switch port) of a 1000BASE-T1 system implemented according to the requirements defined in chapter 7 shall fulfill the requirements listed in chapters 8.2 and 8.3. All tests shall be fulfilled in an identical configuration.

Note:

This means all the following tests shall be conducted in one configuration, which is according to chapter 7, and with a channel (when needed) according to chapter 9.

All used information for test ECU design (application notes, layout recommendations, configurations etc.) shall be documented in the test reports. There must not be any further undocumented information (e.g. configuration of undocumented registers). The layout and the used configuration shall be reviewed by the semiconductor manufacturer and the review documentation shall be part of the documentation.

### 8.2 Transceiver testing requirements

#### 8.2.1 Configuration for testing

The configuration for all the following tests (chapters 8.2.2 to 8.2.4) shall be identical and according to chapter 7. Additionally, the used CMC in the BIN shall be compliant with [10].

The channel types 1, 2 and 3 as defined in chapter 9 shall be used for testing.

#### 8.2.2 Conformance test requirements

All tests of [3], [4] and [5] shall be conducted. The requirements as defined in [3], [4] and [5] are valid.

#### 8.2.3 Interoperability test requirements

All tests of [6] shall be conducted. The requirements as defined in [6] are valid.

#### 8.2.4 EMC test requirements

All tests of [7] shall be conducted. The requirements as defined in [7] are valid. For the avoidance of doubt all recommended limits shall be met as mandatory.



## 8.3 Qualification of 1000BASE-T1 derivative devices

### 8.3.1 Scope

These definitions shall be used for a harmonized test approach for derivatives of 1000BASE-T1 transceiver devices within the qualification tests according to [3], [4], [5], [6], [7], [8] and [9].

### 8.3.2 General

In general, all 1000BASE-T1 transceiver devices (transceiver block) must fulfill the requirements of the qualification test specifications listed in 8.3.1 and shall be tested completely and separately against the specifications.

In case of different 1000BASE-T1 transceiver devices with common underlying technical implementation and minor differences, the users of this specification may

- define an adoptable 1000BASE-T1 transceiver devices family and device derivatives of this family
- agree upon options for reduction of single qualification test cases.

This specification contains requirements for the qualification test plan definition for family of 1000BASE-T1 transceiver devices.

In order to minimize the required qualification tests for device derivatives, a common practice for “family plan” qualification, including test planning, execution and reporting shall be established.

### 8.3.3 Terms and definitions

In the meaning of the requirements within this document, different transceiver device types may be combined to a 1000BASE-T1 transceiver family only if their dies, circuitries, setting, functionality ranges / feature set and operation parameters are identical. This means, in the context and coverage of these definitions, only the applicable (permitted) differences between transceiver devices within one semiconductor family are different packages and different bonding implementations.

|  |  |
|--|--|
| <b>Transceiver derivatives</b>         | A transceiver type that belongs to a 1000BASE-T1 transceiver family                            |
| <b>Transceiver umbrella derivative</b> | 1000BASE-T1 transceiver which is supposed to cover the maximum critical family implementations |
| <b>Transceiver root derivative</b>     | The chronological first available device derivative  |

Note:

The transceiver root is not necessarily the umbrella device.

### 8.3.4 Qualification test plan

At least root and umbrella devices shall be tested completely against the specifications listed in chapter 8.3.1.

In certain cases, parts of these qualification tests may be transferred for the qualification of family derivatives which offers options to reduce the test scope. However, such reductions will only be valid, if all qualification tests on the umbrella and on the root derivative have been passed completely.

In general, even in case of similarities between 1000BASE-T1 transceiver devices, e.g. of the same semiconductor manufacturer, all have to be tested separately and completely against the specifications listed in chapter 8.3.1.

The adopters of this specification shall agree about the selection of the umbrella devices for establishing the test plans.

If no other definitions are made by the users of these specifications, the device derivatives with the total maximum function / operating range, number of ports and / or pins are defined to be the most critical ones.

Note:

Based on its technical performances, e.g. because of most critical family implementations, the root derivative can also be defined to be the umbrella devices, too. In this case, at least the root derivative and one additional device shall be tested completely against the specifications listed in chapter 8.3.1.

### 8.3.5 Qualification test performance

For the qualification of 1000BASE-T1 transceiver device derivatives, this specification offers the following two options.

#### 8.3.5.1 Case 1: Packaging

- a. Derivate description, compared with umbrella / root derivate:
  - Differences: package type, size and / or pinout,
  - Commonalities: implementation of the transceivers die, xMII, MDI-/supply circuitry / filter and settings as well as functionality ranges / feature set and operation parameters (e.g. temperature and voltage range).
- b. Options for action:
  - Ensure that device derivatives are subsets of umbrella / root derivative in matters of functionality ranges / feature set and hardware,
  - Migration of all root / umbrella derivative results from qualification tests listed in chapter 8.3.1,
  - Revision / re-run and evaluation of EMC and ESD Tests according to [7].

#### 8.3.5.2 Case 2: Bonding

- a. Derivate description, compared with umbrella / root derivate:
  - Differences: reduced bonding, e.g. reduced number of MDI – ports,
  - Commonalities: implementation of the transceivers die, xMII, MDI-/supply circuitry / filter and settings as well as, package type, size, pinout as well as remaining functionality ranges / feature set and operation parameters (e.g. temperature and voltage range).

b. Options for action:

- Ensure that device derivatives are subsets of umbrella / root derivative in matters of functionality ranges / feature set and hardware,
- Migration of all umbrella / root derivative’s results from qualification tests listed in 8.3.1,
- Revision / re-run and evaluation of EMC- / ESD – Tests according to OPEN ALLIANCE: IEEE 100BASE-T1 EMC Test Specification for transceivers.

**8.3.6 Documentation**

For safeguarding and traceability reasons, all documentation within practical usages shall be binding. First of all, this must be applied for the identification of potential derivate options, e.g. by datasheet descriptions.

All affected qualification test reports must document:

- technical commonalities of and differences between 100BASE-T1 transceiver devices (derivatives) under test and root / umbrella devices,
- motivation for selection derivative and umbrella / root devices,
- references to binding documents,
- complete test results of devices (derivatives) under test and umbrella / root devices
- and test setup differences

**8.3.7 Practical usage: PHY, switch and SoC device derivatives**

In the following section there are several basic assumptions on the development of the different devices. Based on these assumptions the approaches for the qualification of device derivatives are different.

**8.3.7.1 PHY device derivatives**

The PHY is in most cases the basic device for any semiconductor vendor of Ethernet related products. Once a PHY is realized and about to be introduced on the market, there are almost no major changes encountered. Thus, following table for reduced test shall be used:

| Differences between DUT and umbrella device | PCS Test | PHY Control Test | PMA Test | EMC ESD | IOP | Switch Test | ECU-Test (applicable for Tier1 suppliers) |  |
|---|----------|------------------|----------|---------|-----|-------------|---|--|
| <b>Package</b>                              |          |                  |          | X       |     | n/a         |   | -No different Feature<br>-No new functionality |
| <b>All other</b>                            | X        | X                | X        | X       | X   | n/a         | X   |  |

**Table 2: PHYs - Tests cases on derivative differences**

Note:

Explicitly: All changes to transceiver block including initialization settings (scripts) need a re-run of all tests. Modifying scripts is seen as a major change which requires complete re-testing against the complete specifications.

### 8.3.7.2 Switch device derivatives

The procedure is most important to switch devices. Switch devices have been seen in the past in the form that basically the same product was put on the market in different packages, with different number of ports.

| Differences between DUT and umbrella device | PCS Test | PHY_Cont-Test | PMA Test | EMC ESD | IOP | Switch Test | ECU-Test (applicable for Tier1 suppliers) |  |
|---|----------|---------------|----------|---------|-----|-------------|---|--|
| Package                                     |          |               |          | X       |     |             |   | -No different feature<br>-No new functionality   |
| PHY-independent switch features             |          |               |          |         |     | X           | X   | Enhancement of networking capabilities, whereas the technology, functionality and IP of the integrated PHYs are the same |
| Reduced number of ports                     |          |               |          | X       |     |             |   | -No different feature<br>-No new functionality   |
| All other                                   | X        | X             | X        | X       | X   | X           | X   |  |

**Table 3: Switches - Tests cases on derivative differences**

Note:

In case of Switch devices having several PHY instances where all of them are identical (except for the PHY address) and have identical BIN, then the conduction of conformance testing as defined in [3], [4] and [5] shall be required only for one PHY.

Note:

The term networking capability summarizes all switch-dependent features like, VLAN handling, QoS-features, filtering-capabilities, speed of the switching fabric (switching-rate), etc. The technology, functionality and IP of the integrated PHY are to be the same.

Changing the switching fabric (higher switching-rate) might affect the EMC performance of the device.

Note:

An example of this might be a family of products based on a single Silicon device and appear on the market as 7 port, 5 port and 3 port devices.

Here the test of the device which allows the test of all features will be sufficient.

Note:

The re-assignment of pins to a different function available in the silicon, but not seen on devices in a previous test will need a complete re-test.

Example: Changing via bond-out or other configuration method other interfaces e.g. MDIO, MII not seen exactly in the same function in a previous test need a complete re-test.

### **8.3.7.3 SoC device derivatives**

SoC derivate may appear in very different forms. If SoC derivatives cannot be handled in the same manner as other 1000BASE-T1 – transceiver devices, e.g. reduced bonding, all SoC derivatives must be tested completely and evaluated separately.

## **8.4 System requirements**

An ECU incorporating one or more 1000BASE-T1 interfaces shall fulfill the requirement listed in chapters 8.4.1 to 8.4.3 in terms of functional behavior and diagnostic functionality.

### **8.4.1 Wake-up requirements**

The system timing requirements provided in [12] are valid.

### **8.4.2 Diagnostic requirements**

The registers defined in [13] shall be accessible and their behavior shall be according to the requirements defined in [13].

### **8.4.3 Evaluation/testing capabilities for ECUs**

To allow evaluation of ECUs, the 1000BASE-T1 Test Mode functionality with Test Modes 0 to 7 shall be implemented for each 1000BASE-T1 interface of the ECU. (Refer to [1] for description of the test modes). See also chapter 7.3.1.3.

The ECU shall be able to deactivate data transmission (“SEND\_Z”, e.g. “TX off” or “Scrambler off”) of each 1000BASE-T1 interface to allow MDI return loss and MDI Mode conversion reflection test with proper termination inside the transceiver (i.e. 100 Ω).

## 8.5 Additional tests required on ECU-level

The following tests from [8] shall be conducted for analysis of the physical Layer behavior (further higher layer test may be required as well):

| Reference    | Test   | Requirement |
|--------------|--|-------------|
| OABR_PMA_TX1 | Check the Transmitter Output Droop                 | Optional    |
| OABR_PMA_TX2 | Check the Transmitter Timing Jitter in MASTER Mode | Mandatory   |
| OABR_PMA_TX3 | Check Master Transmit Clock Frequency              | Mandatory   |
| OABR_PMA_TX4 | Check the Transmitter Power Spectral Density (PSD) | Optional    |
| OABR_PMA_TX5 | Check the MDI Return Loss                          | Mandatory   |
| OABR_PMA_TX6 | Check MDI Mode Conversion                          | Mandatory   |
| OABR_PMA_TX8 | Check the Transmitter Distortion                   | Optional    |

**Table 4: Additional required tests on ECU-level**

## 8.6 Cable harness recommendation for 1000BASE-T1 test links

To allow a proper operation of the implemented interface, all 1000BASE-T1 links within a cable harness assembly implementation should fulfill the channel requirements of [11].

Therefore, all components of the link should be designed and assembled to ensure the required RF parameters.

## 9 System test environment definition

### 9.1 General

This definition shall be used for defining a test wiring harness that simulates various communication channels according to the channel definitions of IEEE Std. 802.3bp [1] for tests of 1000BASE-T1 transceivers according to [3], [4],[5], [6] and [8]. The chapters also contain examples for a practical implementation.

### 9.2 Channel Type A.1

#### 9.2.1 General

The Type A.1 channel is derived from a 15m link segment. The parameters of the type A.1 channel are derived from the limit definition for a communication channel according to IEEE P802.3bp and OPEN Alliance TC9 definitions for a 1 Gig Hz communications channel. For setting up a real test harness upper and lower limits are added for each parameter. The type A.1 channel implementation shall fulfill these limits at  $(23\pm 2)^\circ\text{C}$  ambient temperature (RT = Room Temperature).

**NOTE:** For cable type reference, *within the body* of this document: “Type A” cable refers to Automotive grade unshielded twisted pair (UTP) cable, with jacketing considered a requirement for 1000BASE-T1.

#### 9.2.2 Required parameters

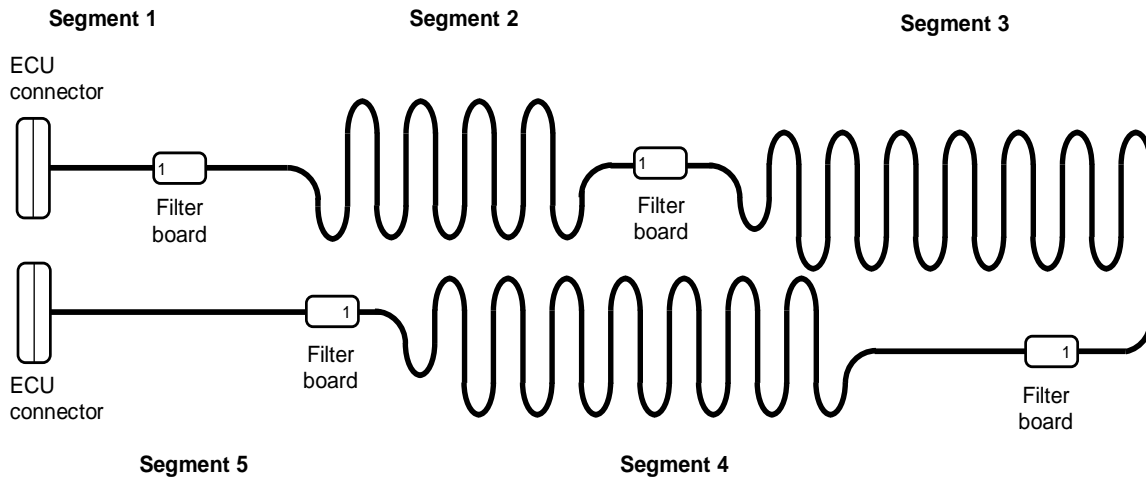
The parameter and limits given in Table 5 are defined for a type A.1 channel implementation.

| Parameter                        | Lower Limit  | Upper Limit  | Comments  |
|----------------------------------|--|--|---|
| CIDM                             | 90 $\Omega$  | 110 $\Omega$   |   |
| IL                               | open   | 1 MHz: 0.66 dB<br>10 MHz: 1.91 dB<br>40 MHz: 3.84 dB<br>140 MHz: 7.32 dB<br>400 MHz: 12.74 dB<br>600 MHz: 15.85 dB |   |
| RL ) <sub>1</sub>                | 1 MHz: 19.0 dB<br>10 MHz: 19.0 dB<br>40 MHz: 16.0 dB<br>130 MHz: 16.0 dB<br>400 MHz: 11.0 dB<br>600 MHz: 11.0 dB | no limit   | ) <sub>1</sub> within the limit relevant frequency range the following requirements are defined: all values of RL must be above the lower limit and in minimum 6 of 9 cable resonant caused local minima should be below to upper limit |
| Propagation delay ) <sub>2</sub> | open   | 2 MHz: 94.0 ns<br>600 MHz: 94.0 ns   | ) <sub>2</sub> measurements of propagation delay according to [11].   |

**Table 5: Required parameter and limits for channel type A.1 implementations according to OPEN Alliance TC9 definitions for a 1 Gig Hz communications channel.**

### 9.2.3 Example for Type A.1 channel implementation

Figure 8 shows the topology of the example type A.1 channel implementation. The description of each part of this implementation is given in Figure 8 and Table 6.



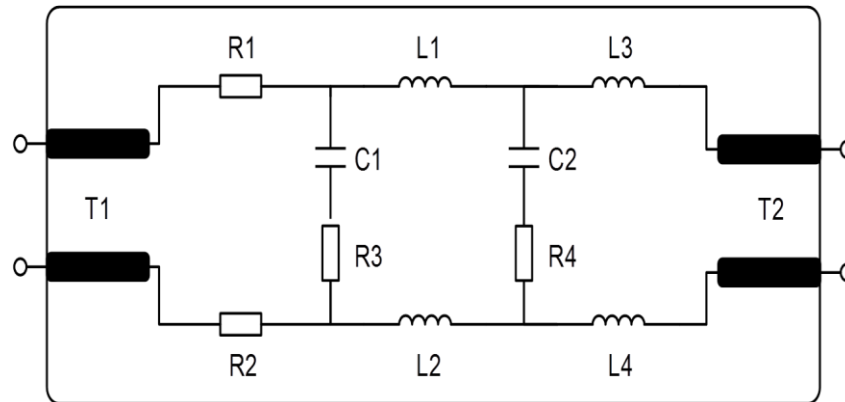
**Figure 8: Example for channel type A.1 implementation – Topology**

| Part            | Description                                       | Type  |
|-----------------|---|---|
| ECU connector 1 | 2 pin connector                                   | shall fulfill TC9 requirements on connectors<br><i>Example: TE 1-Port MATEnet Connector for UTP, COD Z, # 9-2302454-9</i> |
| Segment 1       | 0.5 m cable                                       | shall fulfill TC9 requirements on cables<br><i>Example: LEONI Dacar® 647</i>  |
| Filter board    | RLC filter board with line impedance compensation | see Figure 9  |
| Segment 2       | 3.5 m cable                                       | Same as segment 1   |
| Filter board    | RLC filter board with line impedance compensation | see Figure 9  |
| Segment 3       | 5.0 m cable                                       | Same as segment 1   |
| Filter board    | RLC filter board with line impedance compensation | see Figure 9  |
| Segment 4       | 4.5 m cable                                       | Same as segment 1   |
| Filter board    | RLC filter board with line impedance compensation | see Figure 9  |



| Part            | Description     | Type                    |
|-----------------|-----------------|-------------------------|
| Segment 5       | 1.5 m cable     | Same as segment 1       |
| ECU connector 2 | 2 pin connector | Same as ECU connector 1 |

**Table 6: Example for channel type A.1 implementation – Parts**



**Figure 9: Example for channel type A.1 implementation – Filter board**

| Part   | Description   |  |
|--------|---|--|
| R1, R2 | Thick Film Chip Resistor, 0.5 $\Omega$ , Tol. $\pm$ 1%  |  |
| C1     | Multi-Layer Organic Capacitor, 2.7 pF, Tol. $\pm$ 0.1pF   |  |
| R3     | Thick Film Chip Resistor, 1 k $\Omega$ , Tol. $\pm$ 1%  |  |
| L1, L2 | Chip HF-Inductor, 3.9 nH, Tol. $\pm$ 5%   |  |
| C2     | Multi-Layer Organic Capacitor, 1.6 pF, Tol. $\pm$ 0.1pF   |  |
| R4     | Thick Film Chip Resistor, 17.8 $\Omega$ , Tol. $\pm$ 1%   |  |
| L3, L4 | Chip HF-Inductor, 4.7 nH, Tol. $\pm$ 5%   |  |
| T1     | Edge coupled Microstrip, $Z_{diff} = 93.78 \Omega$<br>25mm (Length) * 1.45mm (Width)* 1mm (Spacing) | PCB Materials<br>– Substrate Thickness: 0.762 mm<br>– Copper Cladding: 35 $\mu$ m<br>– Dielectric Constant: 3.66 |
| T2     | Edge coupled Microstrip, $Z_{diff} = 86.62 \Omega$<br>25mm (Length) * 1.65mm (Width)* 1mm (Spacing) |  |

**Table 7: Example for channel type A.1 implementation – Parts**

**NOTE:** channel type A.1 parameters cannot be discerned by making the channel cable wire longer, or increasing the number of in-lines, beyond what is specified in IEEE 802.3bp document. So 15 meters of cable with 4 in-lines is the *worst case physical limit*. Hence degraded channel conditions are affected by employing filter boards, in place of in-line connectors per Figure 8 and Figure 9, shown above. This allows pushing the channel to the worst case limit lines (per TC9), without physically extending the channel or adding in-line connectors.

## 9.3 Channel Type A.2

### 9.3.1 General

The Type A.2 channel is derived from a 5m link segment scaled from the type A.1 cable.

### 9.3.2 Required parameters

The parameter and limits given in Table 8 are defined for a type A.2 channel implementation.

| Parameter                        | Lower Limit  | Upper Limit  | Comments  |
|----------------------------------|--|--|---|
| CIDM                             | 95 $\Omega$  | 110 $\Omega$   |   |
| IL                               | 1 MHz: 0.08 dB<br>10 MHz: 0.36 dB<br>40 MHz: 0.75 dB<br>140 MHz: 1.55 dB<br>400 MHz: 2.70 dB<br>600 MHz: 3.40 dB | 1 MHz: 0.25 dB<br>10 MHz: 0.65 dB<br>40 MHz: 1.15 dB<br>140 MHz: 2.25 dB<br>400 MHz: 4.10 dB<br>600 MHz: 5.20 dB |   |
| RL ) <sub>1</sub>                | 1 MHz: 25.0 dB<br>66 MHz: 25.0 dB<br>600 MHz: 19.0 dB  | no limit   | ) <sub>1</sub> within the limit relevant frequency range the following requirements are defined: all values of RL must be above the lower limit and in minimum 6 of 9 cable resonant caused local minima should be below to upper limit |
| Propagation delay ) <sub>2</sub> | 2 MHz: 25.0 ns<br>600 MHz: 25.0 ns   | 2 MHz: 30.0 ns<br>10 MHz: 28.5 ns<br>600 MHz: 28.5 ns  | ) <sub>2</sub> measurements of propagation delay according to [11].   |

**Table 8: Required parameter and limits for channel type A.2.**

### 9.3.3 Example for Type A.2 channel implementation

The description of each part of this implementation is given in Table 9.

| Part            | Description     | Type  |
|-----------------|-----------------|---|
| ECU connector 1 | 2 pin connector | shall fulfill TC9 requirements on connectors<br><i>Example: TE 1-Port MATenet Connector for UTP, COD Z, # 9-2302454-9</i> |
| Segment 1       | 5.0 m cable     | shall fulfill TC9 requirements on cables<br><i>Example: LEONI Dacar® 647</i>  |
| ECU connector 2 | 2 pin connector | Same as ECU connector 1   |

**Table 9: Example for channel type A.2 implementation – Parts**

## 9.4 Channel Type A.3

### 9.4.1 General

The Type A.3 channel is derived from a **1.5m** link segment scaled from the type A.1 cable.

### 9.4.2 Required parameters

The parameter and limits given in Table 10 are defined for a type A.3 channel implementation.

| Parameter                        | Lower Limit  | Upper Limit  | Comments  |
|----------------------------------|--|--|---|
| CIDM                             | 95 $\Omega$  | 105 $\Omega$   |   |
| IL                               | 1 MHz: 0.03 dB<br>10 MHz: 0.12 dB<br>40 MHz: 0.24 dB<br>140 MHz: 0.50 dB<br>400 MHz: 0.85 dB<br>600 MHz: 1.10 dB | 1 MHz: 0.10 dB<br>10 MHz: 0.20 dB<br>40 MHz: 0.40 dB<br>140 MHz: 0.80 dB<br>400 MHz: 1.40 dB<br>600 MHz: 1.80 dB |   |
| RL ) <sub>1</sub>                | 1 MHz: 30.0 dB<br>66 MHz: 30.0 dB<br>600 MHz: 19.0 dB  | no limit   | ) <sub>1</sub> within the limit relevant frequency range the following requirements are defined: all values of RL must be above the lower limit and in minimum 6 of 9 cable resonant caused local minima should be below to upper limit |
| Propagation delay ) <sub>2</sub> | 2 MHz: 7.5 ns<br>600 MHz: 7.5 ns   | 2MHz: 10.0 ns<br>10 MHz: 8.5 ns<br>600 MHz: 8.5 ns   | ) <sub>2</sub> measurements of propagation delay according to [11].   |

**Table 10: Required parameter and limits for channel type A.3**

### 9.4.3 Example for Type A.3 channel implementation

The description of each part of this implementation is given in Table 11.

| Part            | Description     | Type  |
|-----------------|-----------------|---|
| ECU connector 1 | 2 pin connector | shall fulfill TC9 requirements on connectors<br><i>Example: TE 1-Port MATenet Connector for UTP, COD Z, # 9-2302454-9</i> |
| Segment 1       | 1.5 m cable     | shall fulfill TC9 requirements on cables<br><i>Example: LEONI Dacar® 647</i>  |
| ECU connector 2 | 2 pin connector | Same as ECU connector 1   |

**Table 11: Example for channel type A.3 implementation - Parts**

## 10 Appendices: Test documentation examples

### 10.1 Test configuration documentation example

| Item        | Type                  | Source                        | Comment  |
|-------------|-----------------------|-------------------------------|--|
| DUT         | PHY -0816 -Test board | Fa. Hell-COM                  |  |
|             |                       |                               |  |
| Cable       | 2*0.14 PP Jacketed    | Longwire&Copper.com           |  |
|             |                       |                               |  |
| Transceiver | 80-0816               | Hell-COM                      | 1000BASE-T1;   |
| Layout      |                       | App-Note AN-12345             | Hell-Com.com\Ap_Note.. 24.12.2017                            |
| Script      | 1000Base Operation    | Script                        | Hell-Com.com\Ap_Note\Sript\1000Base_operation_V.01 22.3.2018 |
| L1          | ABG-8148              | General Inductors             | 80μH   |
| R1, R2      | 1K                    | Best_Ohm AG, Serie 4711, 0805 | 100V   |
| C1, C2      | 100nF                 |                               |  |

**Table 12: Example for test circuitry documentation**

## 10.2 DUT feature documentation example

| DUT Feature                                | YES | NO | Comment   |
|--|-----|----|---|
| TEST Mode 1                                | x   |    |   |
| TEST Mode 2                                | x   |    |   |
| ..   |     | x  | See Deactivated short   |
| TEST Mode 6                                | x   |    |   |
| TEST Mode 7                                | x   |    |   |
|  |     |    |   |
| Deactive signal front end / termination on |     | x  | Allow termination, if..<br>(explain what to do or why there is an exception.. |
| Ready Status Register                      |     | x  | Check ..xyz AND abc instead   |
| ..   |     |    |   |
| Detect short                               |     | x  | Not in this silicon   |
| ..   |     |    |   |
| CRC / symbol failures                      | x   |    |   |
| ..   |     |    |   |
| Polarity detect                            |     | x  | Not in this silicon   |

**Table 13: Example for feature availability documentation**