Advanced diagnostic features for 1000BASE-T1 automotive Ethernet PHYs

TC12 - advanced PHY features

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2 Introduction

This specification describes advanced features of a 1000BASE-T1 automotive Ethernet PHY (often also called transceiver), e.g. for diagnostic purposes for automotive Ethernet PHYs.

3 Normative references

[1] IEEE P802.3bp™ Amendment 4: Physical Layer Specifications and Management Parameters for 1 Gb/s Operation over a Single Twisted-Pair Copper Cable - Clause 97

4 Abbreviation/Symbols

*****	AND
!	NOT
+	OR
COM	Communication ready (status bit)
DCQ	Dynamic Channel Quality
DD	Defect distance
ECU	Electronic Control Unit
FEC	Forward Error Correction
FECC	FEC Event Counter
HDD	Harness defect detection
LL	Link Losses
LP	Link Partner
LQ	Link Quality
LRT	Local Receiver Time
LTT	LinkUp Total Time
MSE	Mean Square Error
MSE_WC	Mean Square Error Worst Case
OS	OPEN/SHORT detection
PHY	PHY is a Physical layer interface device, often called transceiver
POL	Polarity detection and correction
RRT	Remote Receiver Time
SQI	Signal Quality Index
TDR	Time Delay Reflectometry

5 Overview

1000BASE-T1 automotive Ethernet transceivers (PHY or every PHY port of a switch) shall offer the information specified below for diagnostic purposes.

group	group name	parameter	parameter name	description	mandatory /optional	remarks
DCQ	Dynamic Channel Quality	MSE	Mean Square Error	The MSE (Mean Square Error) value of the symbol detection shall be determined in a standardized way	o	1)
		SQI	Signal Quality Index	A classification of the signal quality in 8 stages (3 bit) shall be carried out	m	1), 2)
HDD	Harness defect detection	**OS**	OPEN/SHORT detection	Cable harness errors (short circuit or open line) shall be detected	m	
	TDR based Cable	**TDR**	SHORT/OPEN/NOISE / DISTANCE detection	Cable harness errors detected by TDR-like test approach	m	
LQ	Link Quality	**LTT**	LinkUp Total Time	The time of the last link training shall be stored	m	
		LRT	Local Receiver Time	The timing of the local receiver shall be stored	o	
		RRT	Remote Receiver Time	The timing of the remote receiver shall be stored	o	
		LL	Link Losses	number of link losses since the last power cycle shall be stored	m	
		COM	communication ready	Optimized Link Status information. Signals when communication is possible.	m	
POL	Polarity detection & correction	POL				
FEC	Forward Error Correction	**FECC**	FEC Counter	FEC counter	m	

Table 1: Overview of required PHY parameters.

Remarks to Table 1:

1) The dynamic channel quality shall be determined with a reasonable refresh rate and be stored in the corresponding defined registers. For the evaluation of all registers that represent a dynamic signal quality, there shall be a second register providing the worst value since the last register reading process.

2) The 8 stages shall correlate to the SNR values at the MDI and may represent corresponding bit error rates (in the case of an interference model with white noise).

All optional topics ‘o’ are initial proposals and are only seen as a rough framework. Optional features are not yet fully checked in terms of implementation or feasibility and thus could be changed or even dropped in a future version of this document.

Bold: Features for plant, maintenance and service: Standardized access is required

5.1 Register Size and Register Definitions

IEEE defines for the MDIO Access a standard register size of 16Bit. In order to get an effective register access, registers may contain a group of information when the data are related to the same subject and will be used potentially within the same software entity.

The term register within this document may comprise the access to a single data register in a most basic form as well as the procedural access to a group of single bit and registers or an implemented functional feature of the Ethernet PHY, which process the according data.

The organisation and implementation of registers is vendor specific.

5.2 Clear/Reset Register

All register are set to their default values after Power on Reset and HW Reset. For register within the advanced diagnostic features the SW reset shall be equivalent to a HW-Reset

6 Advanced PHY features

6.1 Dynamic Channel Quality (DCQ)

Dynamic channel quality includes MSE values, SQI values, and peak MSE values.

6.1.1 Mean Square Error (MSE)

Optional or mandatory feature: Optional
Providing Mean Square Error information is optional, if provided it is recommended that the calculation is defined and controlled by the implementer. The MSE information shall not be used for further qualification (e.g. for Interop Testing). For qualification purposes the mandatory SQI information is defined.

The PHY can provide detailed information of the dynamic signal quality by means of a MSE value or comparable information. The MSE value can be determined from the MeanSquareError of the slicer.

The implementation is vendor specific.

The following recommendations can be used as guidance for calculating and presenting the MSE value:

The MSE value for 1000BASE-T1 should be determined across 2^16 (65,536) symbols (summing up and normalization), with a refresh rate in the tolerance range of 80us – 200us. The resulting MSE value shall be linearly scaled to a value in the range of [0…511] and this value shall be placed in the register, DCQ.MSE.

In addition to the current MSE value, the worst case MSE value since the last read should be stored in a second register.

	DCQ.MSE
Name	Mean Square Error
Description	MSE value Vendor specific

Table 2 Definition of DCQ.MSE

	DCQ.MSE_WC
Name	Worst Case Mean Square Error
Description	Max MSE value ; Vendors Specific

Table 3 Definition of DCQ.MSE_WC

6.1.2 Signal Quality Index (SQI)

Optional or mandatory feature: mandatory
The signal quality value (SQI) shall be determined from the determined MSE value or comparable information. The SQI value shall be stored in a register in 8 levels (between “000” = worst value and “111” = 7 = best value).

In addition to the current SQI value, the lowest SQI value calculated since the last register read access shall be stored in the DCQ.SQI register as shown below.

	DCQ.SQI
Name	Signal Quality Index
Description	current SQI value
Description	worst case SQI value since last read

Table 4 Definition of DCQ.SQI

The following features of the SQI value are mandatory:

- When the register value outputs a value of 0 a link loss shall be recorded through the LQ.LFL register.
- The indicated signal quality shall monotonically increase /decrease with noise level.
- It shall be indicated in the datasheet at which level a BER<10^-10 (better than 10^-10) is achieved (e.g. "from SQI=3 to SQI=7 the link has a BER<10^-10 (better than 10^-10)")

During interoperability testing the indicated signal quality shall be monitored and documented for information only.

The recommended correlation between the SQI values stored in the register and an accompanying signal to noise ratio (SNR) based on AWG noise (bandwidth of 550MHz) is shown in Table 5. The bit error rates to be expected in the case of white noise as interference signal are shown in the table as well for information purposes.

SQI value	SNR value @MDI - AWG noise, 550MHz (informative)	recommended BER for AWG noise model (informative)
SQI=0	<18dB	BER>10^-10
SQI=1	18dB=<SNR<19dB	
SQI=2	19dB=<SNR<20dB	
SQI=3	20dB=<SNR<21dB	BER<10^-10
SQI=4	21dB=<SNR<22dB	
SQI=5	22dB=<SNR<23dB	
SQI=6	23dB=<SNR<24dB	
SQI=7	24dB=<SNR	

Table 5 Recommended correlation from SQI to SNR under AWG assumption.

6.2 Harness Defect Detection (HDD)

6.2.1 OPEN and SHORT detection (OS)

Optional or mandatory feature: Mandatory

There shall be a possibility to detect harness defects. This can either be done during normal operation (as long as possible) or after a failure event e.g. an established link is interrupted is signalled or in a specific host-triggered diagnostic mode. With this functionality a PHY shall reliably detect the following error situations as long as the channel is properly terminated (link partner termination is connected to the channel):

- OPEN of one bus wire
- OPEN of both bus wires
- SHORT of both conductors (to ground or supply line)
- SHORT between both bus wires
- (OPTIONAL) SHORT of one conductor (to ground or supply line)*

(OPEN = open circuit, SHORT = short circuit)

It is not needed to distinguish all of the above error situations individually.

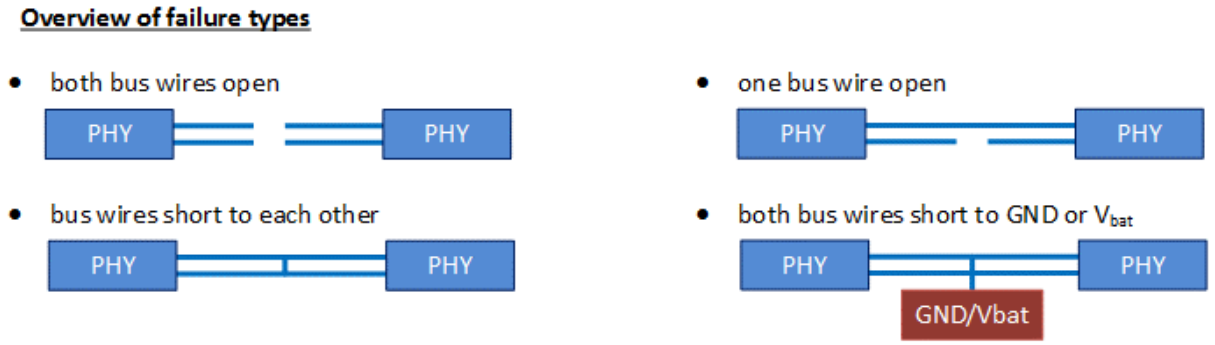

Figure 1 Overview of error situations to be detected.

It is mandatory to detect all these failures when the LP is not transmitting any signal (typically “SEND_Z” for 1000BASE-T1 or as SLAVE). Optionally these failures are also detected when the LP is MASTER and transmitting e.g. TRAINING pattern.*) REMARK: The condition of short circuit of one bus wire to GND or VBAT is not reliably detectable with today’s technology. The detection of short circuit of one wire to GND or VBAT is therefore an optional feature. If no link loss is occurring, this only may be identified by higher layers due to significantly decreased signal quality. An indication for such a failure may be a significantly reduced SQI or sporadic link losses, which can be detected by higher layers (e.g. by SQI register or Link Losses register).

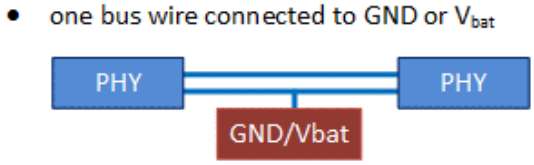

Figure 2 Overview of error situation optionally to be detected.

Error! Reference source not found. Table 7 is showing the Bus Failure Matrix, indicating which combinations of f ailures and environmental conditions are mandatory to detect and which combinations are optional.

	HDD.OS
Name	OS
Description	Cable OK OPEN detect (one or both bus wires) SHORT detect (of bus wires; of one or both bus wires to GND or VBAT)

Table 6 Open / Short detection

Bus Failure Matrix	LP is SLAVE	LP is MASTER
cable OK	mandatory	optional
OPEN detect	mandatory	optional
SHORT detect	mandatory	optional
one bus wires SHORT to GND/VBAT	optional	optional

Table 7 Bus failure matrix

6.2.2 Time Delay Reflection (TDR)

Optional or mandatory feature: mandatory

There shall be the possibility to use a TDR based diagnostic feature for cable diagnostic. This feature is applicable only in diagnostic mode of the PHY device and shall not be activated during normal operation. The TDR diagnostic feature shall be available in both PHY modes: Master or Slave. This diagnostic mode shall be available on a 1000BASE-T1 device independent if operating in 100BASE-T1 or 1000BASE-T1 mode.

Distances to fault above 15m are optional as the channel definition with the OpenAlliance is limited to 15m. The TDR results above the working area of the specific device, the result shall be indicated as “resolution not possible / out of distance”

Activating the TDR feature shall deliver the following information:

	HDD.TDR (only 1000BASE-T1 devices)
Name	TDR
Description	TDR activation
Description	Short Open Noise Cable O.K Test in progress; initial value with TDR ON Test not possible (e.g. active link/communication)

Description	1Bit = Distance to 1st / main fault 000000 = no error 000001 = error about 0-1m away 000010 = error between 1-2m away … 011111= error about 30-31m away 111111 = resolution not possible / out of distance	1Bit approx. 1m	approx. 1… 31m

Table 8 Definition of **HDD.TDR**

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6.3 Link quality – start-up time and link losses (LQ)

6.3.1 Linkup Total Time (LTT)

Optional or mandatory feature: mandatory

Figure 3 and Figure 4 Definition of the start and end times for a determination of the start-up times of a 1000BASE-T1 link.

The transceiver shall provide the time required from enabling the PHY to establish a link. In this context, the following time definitions apply:

- 1000BASE-T1
  Linkup_Total_Time (LU) = t_stop – t_start

  The Link Up Counter is an internal 11 bit counter; with an bit increment each 1ms.

  - For Link Synchronization mode, the counter starts when the PHY transits from SYNC_DISABLE state or LINK_GOOD_state.
  - For AutoNegotiation mode, the counter starts when PHY transits from AutoNegotiation_Enable state or AN_GOOD state to TRANSMIT_DISABLE state.
  - Counter stops when the Link is Up (Link_status_changes fail to OK) and it will be reset to 0 after its value is recorded by the Linkup_Total_Time Register.

t_start = Start of Linkup_Total_Time Counter -- Link Sync State Machine

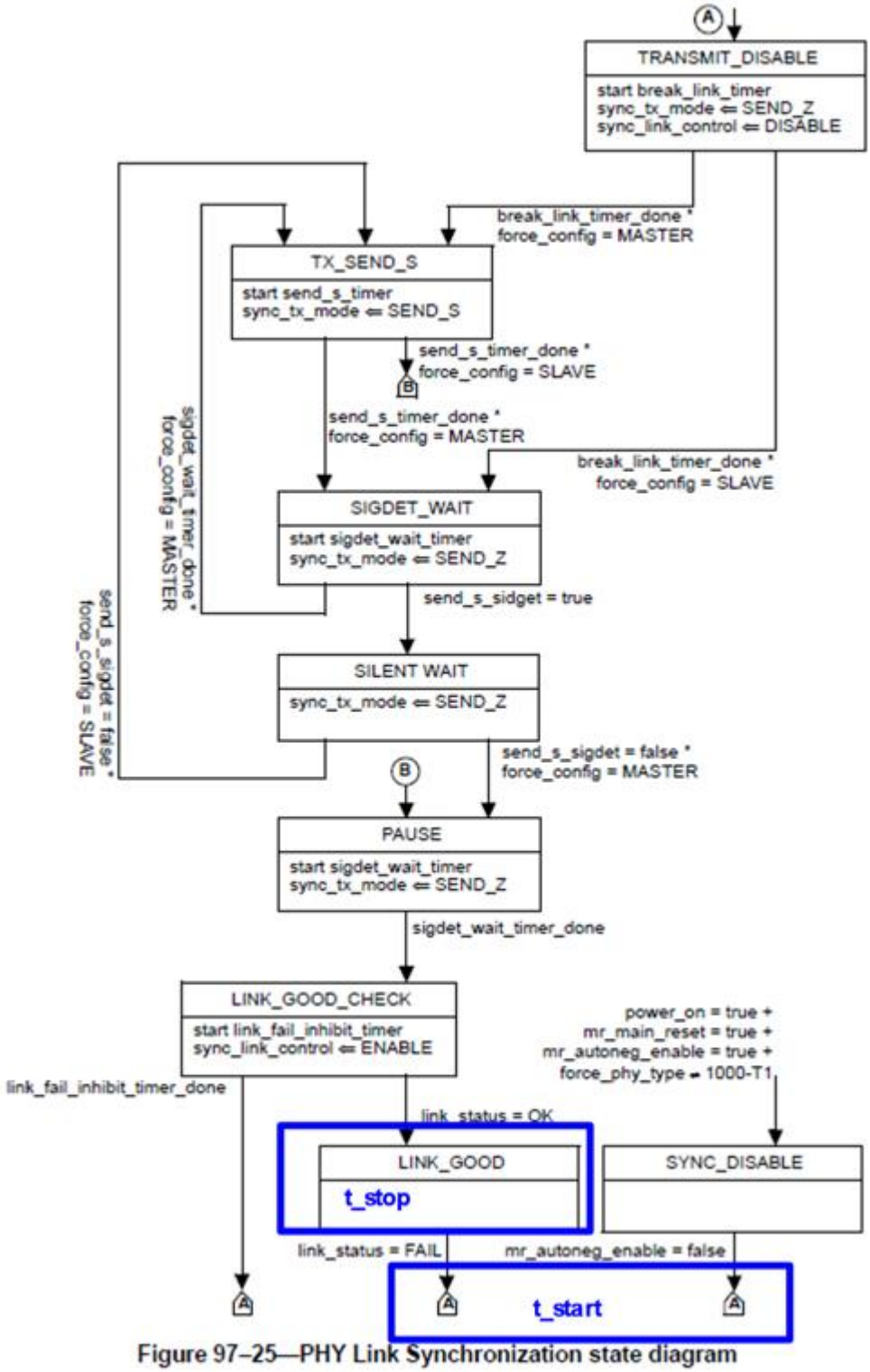

Figure 97–25—PHY Link Synchronization state diagram

Figure 3 Linkup_Total_Time Start and stop condition for timing measurement at 1000BASE-T1 with Link Synchronization

t_start Start of Linkup_Total_Time Counter -- AutoNegotiation State Machine

98.5.5 State diagrams

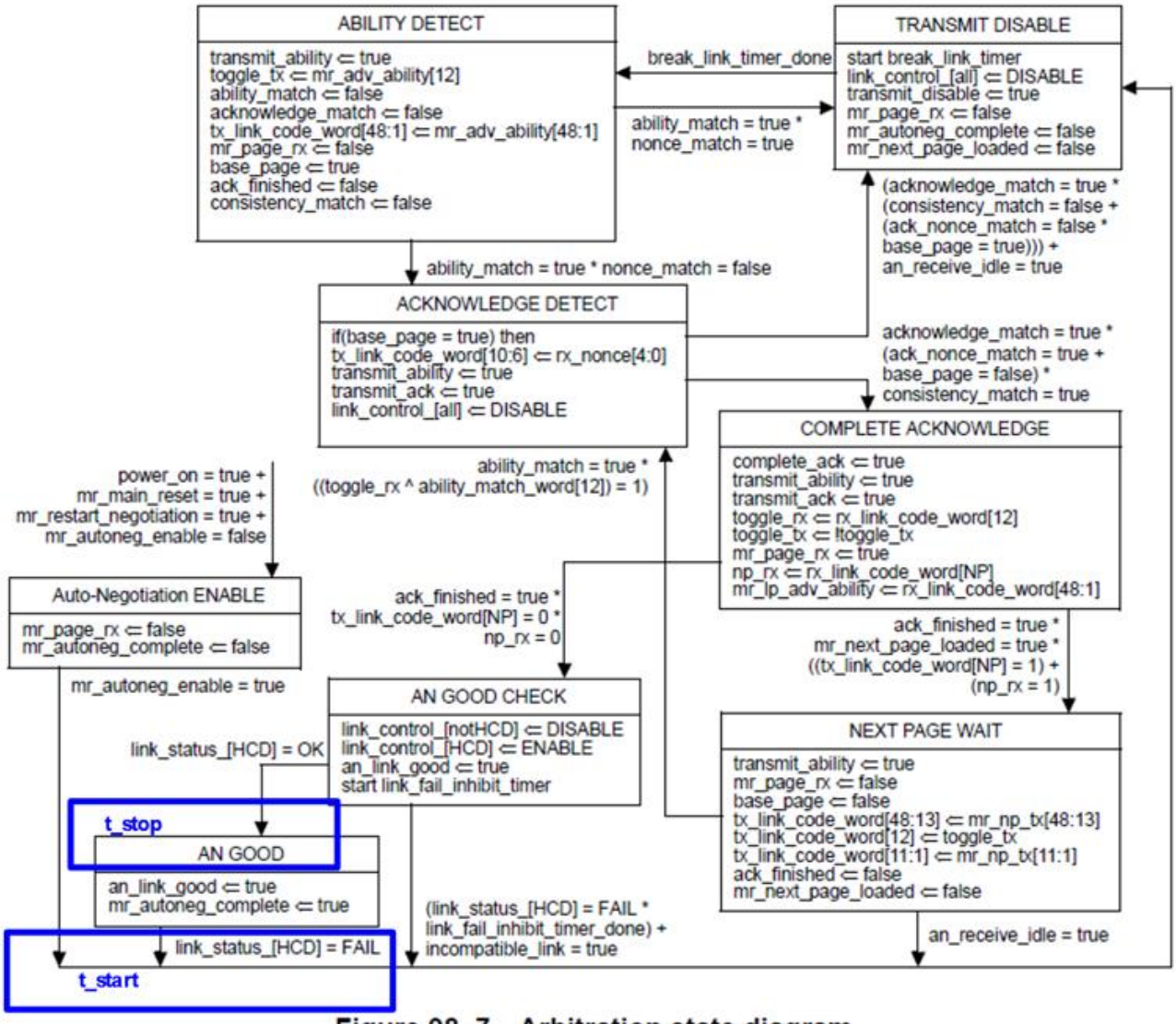

Figure 98–7—Arbitration state diagram

Figure 4 Linkup_Total_Time Start and stop condition for timing measurement at 1000BASE-T1 with Auto-Negotiation

	LQ.LTT
Name	Linkup_Total_Time
Description	) Information about the total link up time from enabling the PHY until the link is established.
Explanation	1 Bit == 1ms; max range 2047ms

Table 9 Definition of LQ.LTT

6.3.2 Local receiver time (LRT)

Optional or mandatory feature: optional

For the last successful training, the transceiver shall provide the time required from PHYC control INIT_MAXWAIT_TIMER state until the loc_phy_ready = OK. In this context, the following time definitions apply (Tstart_RT is defined by Figure 5):

- 1000BASE-T1
  Local Receiver Time (LRT)
  Tstop_RT =>loc_phy_ready=OK
  LQ.LRT= Tstop_RT – Tstart_RT

	LQ.LRT
Name	Local Receiver Time
Description	Time until loc_phy_ready = OK

register value	Explanation
Explanation	1 Bit == 1ms; max range 250ms

Table 10 Definition of LQ.LRT register

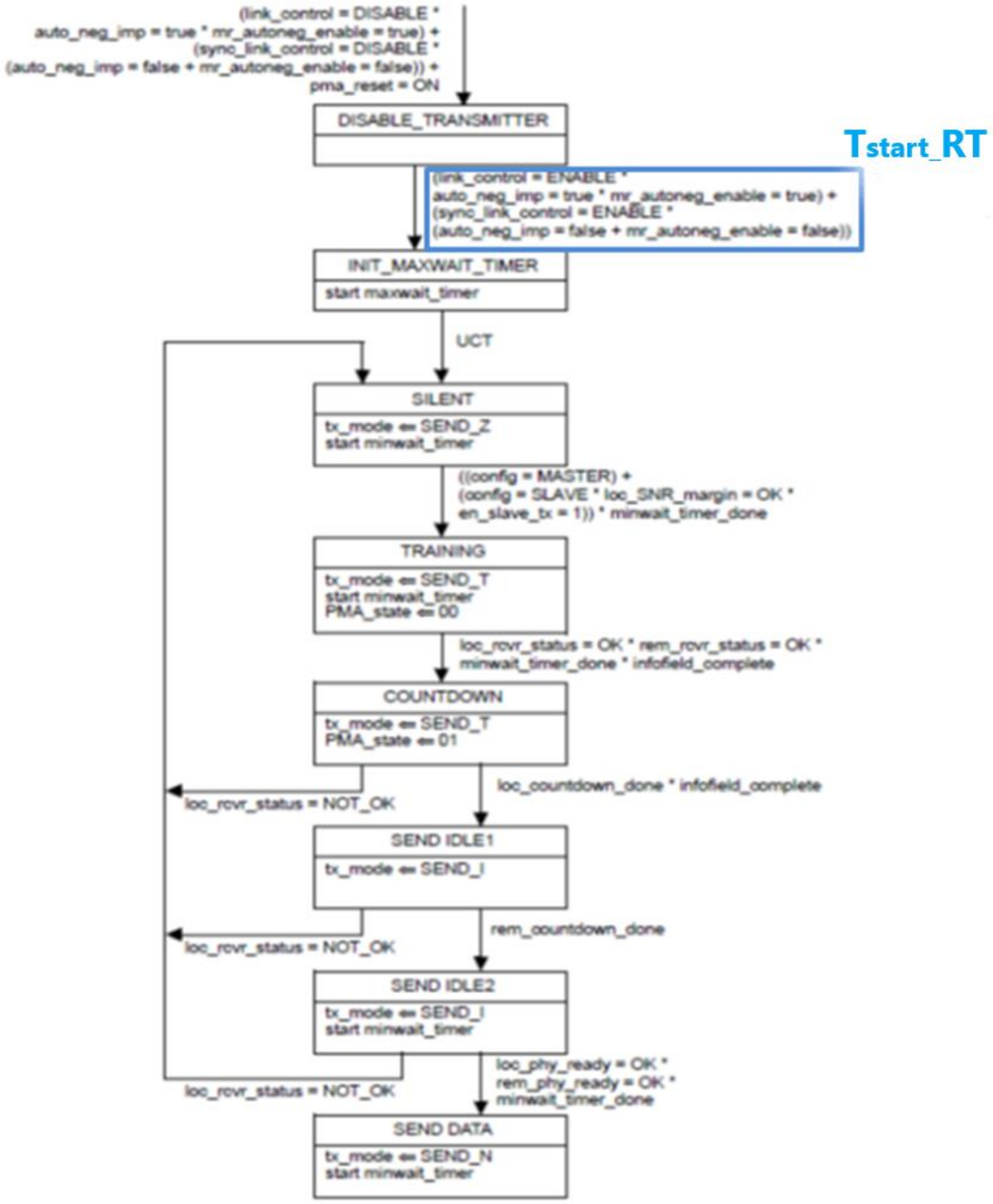

Figure 97–26—PHY Control state diagram

Figure 5 LQ.LRT and LQ.LTT Start condition for timing measurement at 1000BASE-T1

6.3.3 Remote receiver time (RRT)

Optional or mandatory feature: optional

For the last successful training, the transceiver shall provide the time required from PHYC control INIT_MAXWAIT_TIMER state until the local PHY is signalling that rem_phy_ready = OK. In this context, the following time definitions apply (Tstart_RT as in Subclause 6.3.2):

- 1000BASE-T1
  Remote Receiver Time (RRT)
  Tstop_RT=> rem_phy_ready=OK
  LQ.RRT= Tstop_RT- Tstart_RT

	LQ.RRT
Name	Remote Receiver Time
Description	Time until rem_phy_ready = OK

register value	Explanation
Explanation	1 Bit == 1ms; max range 250ms

Table 11 Definition of LQ.RRT register

6.3.4 Link Losses (LL)

Optional or mandatory feature: mandatory

The PHY shall store the number of link failures which occurred since the last power cycle in a register.

	LQ.LFL
Name	Link Losses
Description	number of Link Losses which occurred since last power cycle (0…63)
Explanation	0 …63 link losses occurred

Table 12 Definition of LQ.LFL register

6.3.5 Communication ready status (COM)

Optional or mandatory feature: mandatory

The Communication_ready (Comm_ready) status is an optimized Link_Status information which shall be provided via the extended status register as information for higher layers to signal that from now on communication via the link is possible.

The optimized link status shall be defined by the Comm ready status, when this meets the system will be confirmed as capable of communicating.

- 1000BASE-T1
  Comm_ready = link status

	LQ.COM
Name	Communication Ready Status
Description	information on communication ready

	Explanation
Explanation	False If !(loc_phy_ready = OK * rem_phy_ready = OK * link_status = OK)
	True If (loc_phy_ready = OK * rem_phy_ready = OK * link_status = OK)

Table 13 Definition of LQ.COM

6.4 Polarity Detection and Correction (POL)

In accordance with the specifications (1000BASE-T1). No specific diagnostic feature.

6.5 Forward Error Correction Counter

6.5.1 FEC Counter (FECC)

Optional or mandatory feature: mandatory

The transceiver shall store the number of frames with correctable FEC errors, which occurred since the last power cycle or reset.

	FEC.FECC
Name	Forward Error Correction Counter
Description	Number of Frames captured (0…1023) with symbols corrected by FEC. Note – Up to 22 symbols could be corrected by FEC without an error / data loss in the received data.
Explanation	0…1023 frames corrected

Table 14 Definition of FEC.FECC

=== End of Document===