10BASE-T1S PLCA Management Registers

TC14 – MDIO registers for PLCA

Author & Company	Piergiorgio Beruto (Canova Tech)
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Contents

Introduction

In addition to the 10BASE-T1S PHY, IEEE802.3cg Clause 148 defines the optional PLCA Reconciliation Sublayer for achieving deterministic performance on a shared media (multidrop) network.

Although the RS is defined above the MII from a layering perspective, some 10BASE-T1S implementations embed PLCA in the PHY IC. This allows to add PLCA functionalities connecting to existing MCUs / Ethernet switches that provide an exposed MII interface to the PHY.
For such implementations, the PLCA management objects defined in Clause 30 can be mapped to the vendor-defined address space of Clause 45 registers.

In such a way, PLCA can be managed using the same standard MDIO interface already defined for Ethernet PHYs.

Abbreviation/Symbols

*****	*AND*
!	*NOT*
+	*OR*
0x	*prefix for numbers represented in hexadecimal notation*

1 Scope

The objective of this document is to provide a standard set of management registers for 10BASE-T1S implementations embedding the PLCA Reconciliation Sublayer functions.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

[1] IEEE Computer Society, "IEEE Std 802.3cg™-2019, Amendment 5: Physical Layer Specifications and Management Parameters for 10 Mb/s Operation and Associated Power Delivery over a Single Balanced Pair of Conductors," IEEE Standards Association, New York, 2019.

[2] IEEE Computer Society, "IEEE Standard for Ethernet," IEEE Standards Association, New York, 2018.

3 Terms and Definitions

For the purposes of this document, the terms and definitions given in [1] and [2] apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

— ISO Online browsing platform: available at https://www.iso.org/obp

— IEC Electropedia: available at http://www.electropedia.org/

4 Register map

PLCA management registers are defined in MMD 31 (Vendor Specific 2) of the Clause 45 address space.

Table A.1 — PLCA registers

MMD	Address	Name	Description
31	0xCA00	IDVER	ID and version register
31	0xCA01	CTRL0	control register #0
31	0xCA02	CTRL1	control register #1
31	0xCA03	STATUS	status register
31	0XCA04	TOTMR	to_timer configuration
31	0xCA05	BURST	burst mode configuration

4.1 IDVER - ID and Version register (31.CA00)

The assignment of bits in the PLCA ID and version register is shown in Table A.1.0

Table A.1.0 — IDVER bits assignment

Bit(s)	Name	Description	R/W [a]	Default/Value
15:8	IDM	register map ID	RO	0x0A
7:0	VER	register map version	RO	0x11

NOTE

[a] RO = read-only, RW = read-write, SC = self-clearing

4.1.1 IDM

Constant field indicating that the address space is defined by this document. These bits shall read as 0x0A (Open Alliance).

4.1.2 VER

Constant field indicating the version of this document the register map conforms to. Some registers/bits defined herein may not be available in all revisions. The management entity can read this register to provide backward compatibility. For the present revision of this specification, these bits shall read as indicated in Table A.1.0/Value.

4.2 CTRL0 – Control Register #0 (31.CA01)

The assignment of bits in the PLCA control register 0 is shown in Table A.1.1

Table A.1.1 — CTRL0 bits assignment

Bit(s)	Name	Description	R/W [a]	Default/Value
15	EN	PLCA enable	RW	0
14	RST	PLCA reset	RW,SC	0
13:0	-	Reserved	RO	0
NOTE [a] RO = read-only, RW = read-write, SC = self-clearing				

4.2.1 EN

When this bit is set to a logical 1, the PLCA RS functions are enabled. Otherwise, the PHY operates in plain CSMA/CD mode, without the performance enhancement provided by PLCA. This is the default condition.

This bit maps to the *aPLCAAdminState* and *acPLCAAdminControl* objects in [1] Clause 30.

4.2.2 RST

When this bit is set to a logical 1, the PLCA RS functions are reset. This bit is self-clearing and shall read as 1 while PLCA reset is in progress, otherwise it shall read as 0.

This bit maps to the *acPLCAReset* object in [1] Clause 30.

4.3 CTRL1 – Control Register #1 (31.CA02)

The assignment of bits in the PLCA control register 1 is shown in Table A.1.2

Table A.1.2 — CTRL1 bits assignment

Bit(s)	Name	Description	R/W [a]	Default/Value
15:8	NCNT	Node count	RW	8
7:0	ID	PLCA ID	RW	255
NOTE [a] RO = read-only, RW = read-write, SC = self-clearing				

4.3.1 NCNT

This field sets the maximum number of PLCA nodes supported on the multidrop network. On the node with PLCA ID = 0 (see 4.3.2), this value must be set at least to the number of nodes that may be plugged to the network in order for PLCA to operate properly.

This bit maps to the *aPLCANodeCount* object in [1] Clause 30.

4.3.2 ID

This field sets the PLCA ID of the node. User should ensure this ID is unique across the multidrop network to achieve collision-free operation. The special value 255 causes PLCA functions to be suspended. The special value 0 is used to configure the node as the PLCA coordinator.

This bit maps to the *aPLCALocalNodeID* object in [1] Clause 30.

4.4 STATUS – Status register (31.CA03)

The assignment of bits in the PLCA status register is shown in Table A.1.3

Table A.1.3 — STATUS bits assignment

Bit(s)	Name	Description	R/W [a]	Default/Value
15	PST	Node status	RO	-
14:0	-	Reserved	RO	0
NOTE [a] RO = read-only, RW = read-write, SC = self-clearing				

4.4.1 PST

This field reads as 1 when the node is either

- configured as coordinator (ID = 0) and the BEACON signal is being transmitted regularly
- configured as a follower (ID > 0) and the BEACON signal is being received regularly

It reads 0 otherwise.

This bit maps to the *aPLCAStatus* object in [1] Clause 30.

4.5 TOTMR – Transmit opportunity timer register (31.CA04)

The assignment of bits in the PLCA transmit opportunity timer register is shown in Table A.1.4

Table A.1.4 — TOTMR bits assignment

Bit(s)	Name	Description	R/W [a]	Default/Value
15:8	-	Reserved	RO	0
7:0	TOT	to_timer value	RW	32
NOTE [a] RO = read-only, RW = read-write, SC = self-clearing				

4.5.1 TOT

This field sets the value of the PLCA to_timer in bit-times, which determines the PLCA transmit opportunity window opening. For a discussion on how this timer relates to the network and PHY parameters, please consult [1].
For achieving collision-free operation, the to_timer must be set equally across all the nodes on the multidrop network. The default value guarantees proper operation of a network featuring IEEE conformant PLCA enabled nodes communicating over a 25 m twisted-pair cable in line topology.

This bit maps to the *aPLCATransmitOpportunityTimer* object in [1] Clause 30.

4.6 BURST – Burst mode configuration register (31.CA05)

The assignment of bits in the PLCA burst mode register is shown in Table A.1.5

Table A.1.5 — BURST bits assignment

Bit(s)	Name	Description	R/W [a]	Default/Value
15:8	MAXBC	Max burst count	RW	0
7:0	BTMR	Burst Timer	RW	128
NOTE [a] RO = read-only, RW = read-write, SC = self-clearing				

4.6.1 MAXBC

This field sets the maximum number of additional packets the node is allowed to send during its own transmit opportunity. When set to 0, PLCA burst mode is turned off. This is the default condition. Refer to [1] for a discussion about burst mode and its purpose.

This bit maps to the *aPLCAMaxBurstCount* object in [1] Clause 30.

4.6.2 BTMR

This field sets the value of the PLCA burst_timer in bit-times. When burst mode is enabled by setting MAXBC to a non-zero value (see 4.6.1), these bits configure the amount of time to wait for the MAC to deliver a new packet before yielding the current transmit opportunity. To ensure proper operation of PLCA burst mode, this field must be set greater than the local MAC IPG duration, including any additional MAC TX latency. The default value is enough for typical MAC implementations. If PLCA burst mode is not used, the value of this field is ignored by the PLCA RS.

This bit maps to the *aPLCABurstTimer* object in [1] Clause 30.