IEEE 10BASE-T1S Implementation Specification

TC14 – System Implementation

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Contents

Introduction

This specification describes the system implementation of 10BASE-T1S interfaces, used in automotive applications.

Abbreviation/Symbols

BIN	Bus Interface Network
CD	Collision Detection
CRC	Cyclic Redundancy Check
CM	Common Mode
CMC	Common Mode Choke
CMT	Common Mode Termination
CSMA/CD	Carrier Sense Multiple Access / Collision Detection
DC	Direct Current
DET	Differential End Termination
DGND	Digital Ground
DME	Differential Manchester Encoding
DUT	Device under Test
ECU	Electronic Control Unit
ED	Energy Detect
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
ET	End Termination
GND	Ground connection in electrical circuits
IC	Integrated Circuit
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IL	Insertion Loss
IP	Intellectual Property
IOP	Interoperability
ISO	International Organization for Standardization
LPF	Low Pass Filter
MAC	Media Access Control

MACPHY	A MACPHY solution integrates an IEEE Clause 4 MAC and a 10BASE-T1x PHY exposing a low pin count Serial Peripheral Interface (SPI) to the host microcontroller.
MCU	Micro Controller Unit
MDI	Medium Dependent Interface
MDIO	Management Data Input/Output
MII	Media Independent Interface
MQS	Micro Quadlock System
OEM	Vehicle Manufacturer / Original Equipment Manufacturer
OSC	Oscillator/Cristal
PCS	Physical Coding Sublayer
PCB	Printed Circuit Board
PSD	Power Spectral Density
PGND	Power Ground
PHY	Interface semiconductor circuit for implementation of the functions of the Ethernet physical layer
PLCA	Physical Layer Collision Avoidance
PMA	Physical Medium Attachment
PMD	Physical Medium Device
PoDL	Power over Data Line
P2P	Point-to-point
QoS	Quality of Service
RF	Radio Frequency
RGMII	Reduced Gigabit Media Independent Interface
RL	Return Loss
RS	Reconciliation Sublayer
RT	Room Temperature
Rx	Receive
SCC	Standalone Communication Channel
SGMII	Serial Gigabit Media Independent Interface
SNR	Signal to Noise Ratio
SOC	System on Chip
SPI	Serial Peripheral Interface
S-Parameter	Scattering Parameter
SQI	Signal Quality Index
Switch	A device that interconnects the nodes with the Ethernet physical layer in a network
TDR	Time Domain Reflectometry
Tx	Transmit

UTP	Unshielded Twisted Pair
VCC	Pin for IC voltage supply
VDD	Pin for IC voltage supply
VLAN	Virtual local area network

1 Scope

The purpose of this document is to provide general definitions and requirements for 10BASE-T1S interfaces, which are intended to be used on automotive applications.

The main focus of this document is to define a general set of requirements for qualification and testing purposes following the OPEN Alliance generated test specifications. The implementation of 10BASE-T1S interface shall be applicable with the application notes of the semiconductor manufacturer of the specific PHY as DUT.

If a semiconductor manufacturer makes use of different approach for the implementation of 10BASE-T1S interfaces, the semiconductor manufacturer must address this to their customers and find an appropriate alternative test approach. It is still recommended to use the same definitions for all tests. Some or even all OPEN Alliance tests specifications might be not applicable.

The same Bus Interface Network (BIN) shall be used for all tests of Transceiver/integrated circuits:

- EMC [7],
- Interoperability [6],
- Conformance (PMA [4], PCS [5] and PLCA Test [3]).

10BASE-T1S System Implementation Specification shall be applied for 10BASE-T1S PHYs operation at 10Mb/s with PLCA enabled.

Operation with PLCA disabled is not in the scope of this specification.

Within the conformance tests there may be tests where the implementation of the BIN is not relevant. The specified implementation shall be used where necessary.

Communication systems using Power over data line (PoDL) are not covered by this specification.

Topics related to transmission speed changes from 100Mb/s to 10Mb/s or vice versa are out of the scope of this document

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

[1] IEEE Std 802.3cg™-2019, IEEE Standard for Ethernet - Amendment 5: Physical Layer Specifications and Management Parameters for 10 Mb/s Operation and Associated Power Delivery over a Single Balanced Pair of Conductors.

[2] IEEE P802.3-2018 IEEE Standard for Ethernet

[3] OPEN ALLIANCE: 10BASE-T1S PLCA Test Suite

[4] OPEN ALLIANCE: 10BASE-T1S Physical Media Attachment Test Suite

[5] OPEN ALLIANCE: 10BASE-T1S Physical Coding Sublayer Test Suite

[6] OPEN ALLIANCE: 10BASE-T1S Interoperability Test Suite

[7] OPEN ALLIANCE: 10BASE-T1S Transceiver EMC Specification

[8] OPEN ALLIANCE: Automotive Ethernet ECU Test Specification

[9] OPEN ALLIANCE: Switch Semiconductor Test Specification

[10] OPEN ALLIANCE: 10BASE-T1S Common Mode Choke Test Specification

[11] OPEN ALLIANCE: 10BASE-T1S Definitions for Communication Channel

[12] OPEN ALLIANCE: Sleep/Wake-up Specification for Automotive Ethernet – Revision 1.0

[13] OPEN ALLIANCE: Advanced diagnostic features for automotive Ethernet PHYs

[14] OPEN ALLIANCE: 10BASE-T1S EMC Test Specification for ESD suppression devices

[15] ISO / IEC 11801:2002 Information technology — Generic cabling for customer premises

[16] OPEN ALLIANCE: 10BASE-T1S Link Segment Channel and Components

[17] OPEN ALLIANCE: 10BASE-T1S PLCA Management Registers – Revision 1.2

[18] OPEN ALLIANCE: 10BASE-T1S PMD Transceiver Interface – Revision 1.5

3 Terms and Definitions

For the purposes of this document, the terms and definitions given in [1] - [18] apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

— ISO Online browsing platform: available at https://www.iso.org/obp

— IEC Electropedia: available at http://www.electropedia.org/

— Node term definition

End Node	A node that is at either end of a mixing segment. There are no other nodes between the End Node and the 100Ω end termination. The End Node may contain the 100Ω end termination.
Drop Node	Any node that is located between the two end nodes
Coordinator	This is the node configured as aPLCALocalNodeID=0 that is responsible for the periodic transmission of the BEACON and configuring the number of transmit opportunities between each BEACON.
Follower	Followers are any nodes configured as aPLCALocalNodeID=1..254. They synchronize their transmit opportunity counter with the reception of the periodic BEACON transmitted by the coordinator
Head Node	This is the highest-level application node on the mixing segment. It typically implements a Switch or gateway access to the core network beyond the bus segment.

Note: It is expected that each segment includes two end nodes, one coordinator and one head node.

— Transceiver: General term used for PHYs, MACPHYs, PMD Transceiver, PHY integrated in a Switch**.**

4 Overview

This document includes three main Chapters:

- Implementation for 10BASE-T1S, Chapter 5
  This Chapter defines the interface implementation for automotive applications together with requirements on components used to realize the Bus Interface Network (BIN).

- 10BASE-T1S testing requirements and system requirements, Chapter 6
  This Chapter defines further system requirements for systems implemented according to the system implementation.

- System test environment definition, Chapter 7
  This Chapter defines the system test environment, in which the Transceiver as implemented system requirements shall be evaluated.

5 Implementation for 10BASE-T1S

5.1 General

For 10BASE-T1S automotive Ethernet the physical layer implementation of a BIN shall be implemented according to this chapter of the specification.

Component ratings listed in this document shall be valid within the specified temperature range (e.g. -40°C … +85°C / 105°C / 125°C) of the implemented system.

5.2 Collision Detection (CD) / Handling

The automotive EMC immunity requirements exceeds the alien crosstalk noise levels defined in IEEE 802.3cg™-2019 [1]. Therefore, in such environment the CD mechanism of the PHY may not be able to distinguish noise from collisions, limiting the achievable level of immunity.

However, the PLCA feature provides collision-free operation over 10BASE-T1S multi-drop networks. Therefore, if all nodes support PLCA, the additional SNR margin required for CD can be spent to further improve alien noise immunity.

For the above reasons, only “pure” PLCA networks are in scope of this specification. That is, networks where all nodes have PLCA enabled.

Note:
System designers and PHY designers can still use/implement collision detection for other (non-automotive) use cases, however this could lead to different trade-offs between system robustness / noise tolerance which is not discussed in this specification.

5.2.1 PHY with PLCA enabled and with only logical CD reporting to the MAC

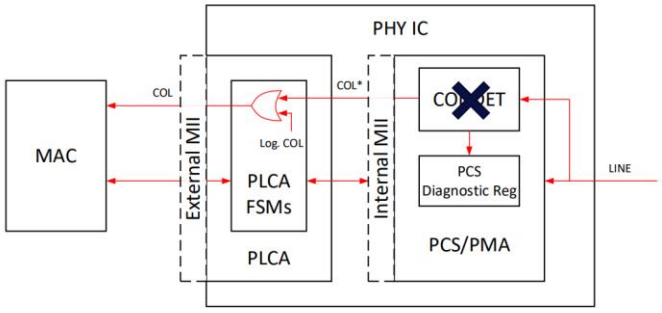


Figure 1: The PHY reports only logical collisions to the MAC. Physical collisions are not detected.

A logical collision it is a signaling on the COL pin triggered by the PLCA RS, according to [1], to align the transmissions from the MAC to the node´s transmit opportunity.

5.2.2 PHY with PLCA enabled and with both logical and physical CD reporting to the MAC (Option)

Physical collisions are reported to the MAC as well as the logical collisions that are generated by the PLCA RS. In this scenario, additional noise margin may be required, leading to different compromises in terms of system robustness / noise tolerance.

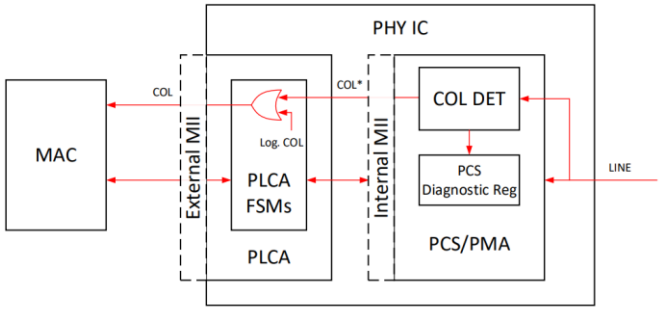


Figure 2: The PHY reports both logical and physical collisions to the MAC (not recommended for automotive usage).

5.2.3 PHY with PLCA enabled and with only logical CD reporting to the MAC and physical CD for diagnostic purpose (Option)

This option is similar to the one in section 5.2.1 but physical collisions are detected for the sole purpose of diagnostic. The upper layers can read this information via a management interface such as MDIO or SPI**.**

Depending on the PHY architecture and the noise conditions, the diagnostic collision counter may report inaccurate information.

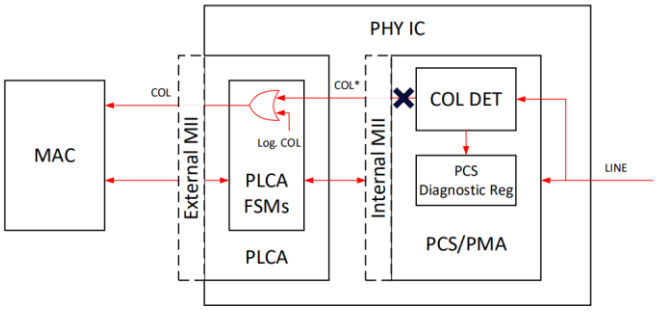


Figure 3: The PHY reports only logical collisions to the MAC. Physical collisions are still detected only for diagnostic purpose.

5.3 Interface circuitry definition

A 10BASE-T1S interface shall be implemented according to the requirements defined in IEEE P802.3cg™ [1] and as shown in this Chapter, including Figure 4 and Table 1.

The interface consists of the transceiver block with transceiver supply decoupling and filtering, optional data-line filter and optional ESD protection and the Bus Interface Network (BIN) consisting of:

Common mode choke (CMC)
DC block capacitors
Common mode termination network
Optional bus end termination network
Optional ESD protection device

The ECU connector is also a part of the interface

All interface components shall be selected in accordance with the data sheets and application notes of the semiconductor manufacturer, as well as OEM´s qualification requirements. The optimized BIN circuit is defined by the semiconductor manufacturer, and in accordance with the IEEE and other application specific requirements, which includes e.g. OEMs qualification requirements.

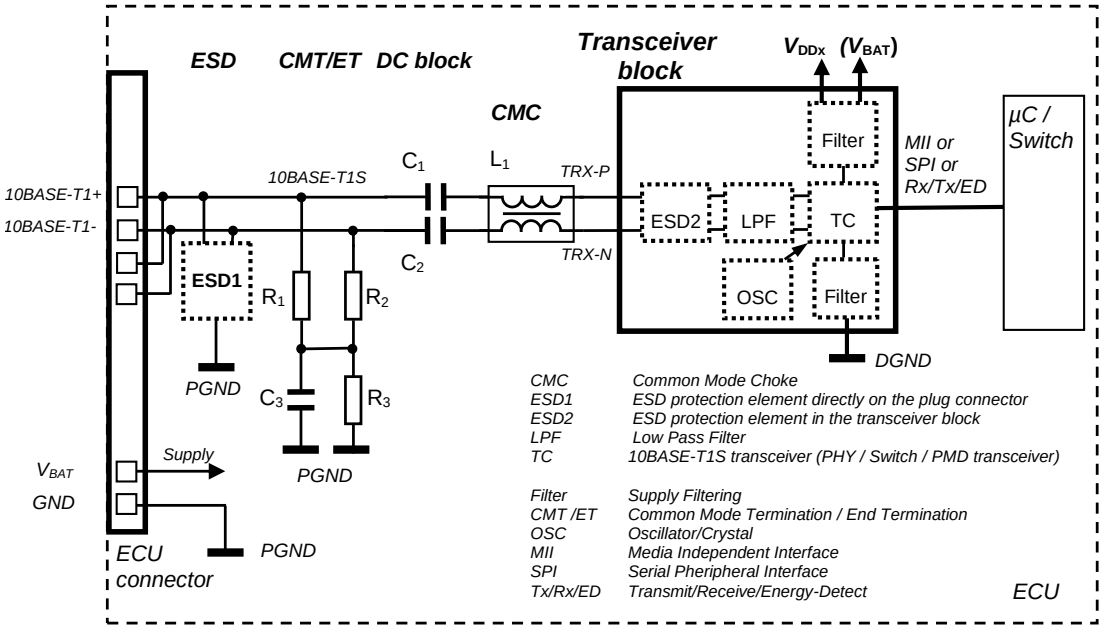
All components of the 10BASE-T1S interface shall be implemented as required in this Chapter and in Chapter 5.4.

The layout and the configuration, including the schematic, of the transceiver interface shall be reviewed by the semiconductor manufacturer.

For layout design information of a specific system implementation the application notes of semiconductor manufacturers shall be considered.

If configuration of the transceiver by software is necessary (i.e. configuration script), this shall also be implemented according to the application notes of the semiconductor manufacturers. The layout and the configuration of the transceiver shall be reviewed by the semiconductor manufacturer.

An exemplary documentation for the used circuitry in a test documentation is provided in appendix Chapter 8.1.



PGND is defined as direct connected to external GND connection.
DGND is defined as internal GND for Transceiver and/or other digital ICs (e.g. micro controller). It can be decoupled by an inductor from external GND connection.

Figure 4: Interface circuitry / schematic for 10BASE-T1S

Figure 4 can be used as reference and guideline for the ECU developments. Deviations from the schematic in Figure 4 are allowed, in particular for grounding concepts, for example, other grounding concepts might be required in case of shielding.

Ref.	Part	Remarks
	Transceiver block	The Transceiver block (Transceiver including ESD protection device (ESD_2) and LPF according to application notes) has to fulfill the requirements of the OPEN Alliance specifications (refer to [IEEE802.3cg™] [1]))1. If the transceiver block is a PMD transceiver it has to fulfill the requirements of the OPEN Alliance specification (refer to OPEN Alliance specification [18].
L_1	**Common mode choke**	Shall fulfill the requirements according to [10].
C_1, C_2	**Capacitor**)1,2 100 nF **Tolerance** ≤ 10% **Voltage range** ≥ 50 V)2	

Ref.	Part	Remarks
R_1, R_2	**Resistor**)2 1.5 kΩ ; 1.5 kΩ (CM) 50 Ω (DET) **Tolerance** ≤ 1 % (even after ESD test) **Nominal power** ≥ 0.4 W for 50 Ω)3 ≥ 0.1 W for 1.5 kΩ)3	CM: optional Common mode termination only for Drop Nodes DET: Differential end termination only for End Nodes The resistors need sufficient ratings. The specified minimum power rating of R1 and R2 is a recommended target value for the typical usage in an automotive area. In the case of more favorable boundary and test conditions, this value can be correspondingly adjusted.
R_3	**Resistor**)2 100 kΩ **Tolerance** ≤ 10% **Nominal power** ≥ 0.1 W	To avoid static charge of the cable harness.
C_3	**Capacitor**)2 4.7 .. 100nF **Tolerance** ≤ 10% **Voltage range** ≥ 50 V)1	100nF)3 The capacitor need sufficient electrical strength.
ESD1		Optional. The ESD protection device in accordance to semiconductor manufacturers´ application notes.
	ECU connector	Shall fulfill the requirements according to [16]. Further requirements and information can be found in Chapter 5.4.3 ECU Connectors for 10BASE-T1S Interfaces (MDI Interface).
C_{MDI}	**C_{MDI} ≤ 25 pF** **Combined capacitive load** (valid for mixed segment with ≤ 8 nodes and ≤ 25m)	Combined capacitive load is the sum of all individually capacitive loads of - transceiver block (10pF)3) - CMC (10pF)3) - rest (5pF)3), consisting e.g. of ECU- connector, ESD1 protection element, 10BASE-T1S signal traces on the PCB. C_{MDI} ≤ 25 pF is valid for a 10BASE-T1S topology with 8 nodes and 25m. For a higher number of nodes, this value has to be reduced or an impedance matching (not specified here), which can reduce the C_{MDI}, seen into the ECU, must be performed.

)1 According to car manufacture specifications for supply voltages ≥ 56V voltage range for 48V electrical systems, typically 100V min. electric strength recommended for ceramic caps. For 12V systems typ. 50V electrical strength is sufficient.

)2 It is required to follow the definitions of semiconductor manufacturer for external passive components and circuit, software configuration (script) and software flow definitions, which are defined in datasheet and application notes.

)3 Recommended target values.

Table 1: Interface component requirements

5.4 Requirements for 10BASE-T1S ECU Interface components

The components used in a 10BASE-T1S interface implementation shall fulfill the following requirements. The testing requirements are described in Chapter 6.2.

5.4.1 10BASE-T1S Transceivers (standalone or integrated in Switch)

All Transceivers (PHYs; MACPHYs, PMD transceivers, PHY integrated in a Switch) used in a 10BASE-T1S interface shall comply with IEEE P802.3cg™ [1] and OPEN Alliance 10BASE-T1S Transceiver Interface [18].

5.4.1.1 Transceiver functional requirements

All Transceivers (PHYs or Switches) used in a 10BASE-T1S interface shall be tested according to the following requirements:

- The PHY/Switch shall support test modes according to [1].
- The PHY/Switch shall provide PLCA status information via a register, according to [1] and [17].
- The PHY/Switch shall be able to detect a short between bus lines and provide this information via a register according to [13].
- The PHY/Switch shall be able to detect interruptions of bus lines and provide this information via a register according to [13].
- The PHY/Switch (optional for PMD-Transceiver) shall provide signal quality information (e.g. SQI) via a status register according to [13].
- The PHY/Switch shall provide unexpected Beacon detection information via a status register according to [13].

If one of the above is not fulfilled a reason/substitution for this shall be documented. An exemplary documentation is provided in appendix Chapter 8.2.

5.4.1.2 Transceiver conformance, EMC and Interoperability requirements

All Transceivers (PHYs or Switches) used in a 10BASE-T1S interface shall be conformant to 10BASE-T1S according to the following test specifications:

- OPEN ALLIANCE: 10BASE-T1S PLCA Test Suite [3]
- OPEN ALLIANCE: 10BASE-T1S Physical Media Attachment Test Suite [4]
- OPEN ALLIANCE: 10BASE-T1S Physical Coding Sublayer Test Suite [5]
- OPEN ALLIANCE: 10BASE-T1S Interoperability Test Suite [6]
- OPEN ALLIANCE: 10BASE-T1S Transceiver EMC Specification [7]

Further details of these tests are described in Chapter 6.2.

5.4.1.3 Evaluation/testing capabilities for integrated circuits

To allow evaluation, 10BASE-T1S Test Mode functionality with Test Modes 1 to 4 (refer to [1]) shall be implemented for each 10BASE-T1S interface of the tested integrated circuit.

5.4.1.4 Further transceiver requirements

Further qualification of Transceivers on system level shall be done according to Chapters [7] and [8].

5.4.2 Common mode choke for 10BASE-T1S interfaces

All common mode chokes used in a 10BASE-T1S interface shall be tested according to [10].
The requirements of the CMC Test Specification [8] are mandatory.

5.4.3 ECU connectors for 10BASE-T1S interfaces (MDI interface)

The complete 10BASE-T1S channel (P2P- as well as the Mixing Segment Channel) as well as all individual components (cables and connectors as well as assembled cable harness) shall fulfill the requirements according to [11]. Therefore all components of the 10BASE-T1S channel shall be designed and assembled to ensure the required RF parameters.

The ECU connector implementation as well as the MDI Test Head shall fulfill the connector requirements of [11].

5.4.4 ESD elements

A landing pad according to the Transceiver's application note for an optional ESD element shall be on the interface layout.

The ESD element can either be placed in the transceiver block or directly in front of the common mode choke as shown in Figure 4.

An ESD element placed between connector and CMC has to fulfill the requirements defined in [14].

5.4.5 Clock tolerance requirements

A typical clock source with 25MHz is used for clock generation, its tolerance shall be less than ±100ppm (±0.01%). For details refer to the Transceiver`s application notes.

The clock tolerance requirement ≤ ±100ppm shall be fulfilled including aging and temperature effects.

6 10BASE-T1S testing requirements and system requirements

6.1 General

A Transceiver of a 10BASE-T1S system implemented according to Chapter 5 shall satisfy the requirements listed in this Chapter. All tests have to be fulfilled in an identical configuration.

Note:

This means all the following tests have to be conducted in one configuration, which is according to Chapter 5, and with a channel (when needed) according to Chapter 7.

All information used for test ECU design (App Notes, Layout recommendation, configuration, etc.) shall be documented in the test reports. There must not be any further undocumented information used (e.g. configuration of undocumented registers). The layout and the used configuration shall be reviewed by the semiconductor manufacturer and the review documentation shall be part of the documentation.

6.2 Transceiver testing requirements

6.2.1 Configuration for testing

The configuration for all the following tests (Chapters 6.2.2 to 6.2.4) shall be identical and according to Chapter 5. Additionally, the CMC used in the BIN shall be compliant with [10].

The channel types 1 and 2 as defined in Chapter 7.2 and 7.3 shall be used for testing.

6.2.2 Conformance test requirements

All tests of [3], [4] and [5] shall be conducted. The requirements as defined in [3], [4] and [5] must be met.

6.2.3 Interoperability test requirements

All tests of [6] shall be conducted. The requirements as defined in [6] must be met.

6.2.4 EMC test requirements

All tests of [7] shall be conducted. The requirements as defined in [7] must be met. For the avoidance of doubt all limits shall be met as mandatory.

6.2.5 Qualification of 10BASE-T1S derivative devices

6.2.5.1 Scope

These definitions shall be used for a harmonized test approach for derivatives of 10BASE-T1S Transceiver devices within the qualification tests according to [3], [4], [5], [6], [7], [8] and [9].

6.2.5.2 General

In general, all 10BASE-T1S Transceiver devices (transceiver block) must fulfill the requirements of the qualification test specifications listed in 6.2.5.1 and have to be tested completely and separately against the specifications.

In case of different 10BASE-T1S Transceiver devices with common underlying technical implementation and minor differences, the users of this specification may

- define an adoptable 10BASE-T1S transceiver devices family and device derivatives of this family
- agree upon options for reduction of single qualification test cases.

This specification contains requirements for the qualification test plan definition for family of 10BASE-T1S Transceiver devices.

In order to minimize the required qualification tests for device derivatives, a common practice for “family plan” qualification, including test planning, execution and reporting may be established.

6.2.5.3 Terms and definitions

In meeting of the requirements within this document, different Transceiver device types may be combined into a 10BASE-T1S Transceiver family only if their dies, circuitries, setting, functionality ranges / feature set and operation parameters are identical. This means, in the context and coverage of these definitions, the only applicable (permitted) differences between Transceiver devices within one semiconductor family are different packages and different bonding implementations.

Transceiver derivatives	A Transceiver type that belongs to a 10BASE-T1S Transceiver family
Transceiver umbrella derivative	10BASE-T1S Transceiver which contains the maximum critical family functionality
Transceiver root derivative	The chronological first available device derivative

Note:
The transceiver root is not necessarily the umbrella device.

6.2.5.4 Qualification test plan

Constant test coverage is required for all devices. However, test scope and effort may be reduced for devices of the same family if it is agreed that test results from previously qualified devices may be transferred.

At least two devices must be included within a family in order to reduce testing. These two devices are usually the *initial silicon* and the *umbrella silicon*. The umbrella silicon device contains the superset of all functionality, complexity, and blocks within a family. The number of ports in a device plays a minor role as they are typically identical. Initial silicon is the first chronological device in the family.

The initial silicon may be the same as the umbrella silicon. In this case, an additional device must be identified to create a device family.

Example:
This example consists of a family of two devices with the same number of pins. The first device contains fewer Ethernet ports than the second device. However, the first device contains additional interfaces (e.g., SGMII,

RGMII, etc.) that do not exist on the second device. In this case, the first device has greater complexity because it contains additional function blocks not present on the second device. The first device may therefore be considered the umbrella device. While the second device contains more Ethernet ports than the first device, it contains no additional function blocks and is therefore less complex. All blocks that would be tested on the second device can be tested on the first device alone.

Note:
Based on its technical performances, e.g. because of most critical family implementations, the root derivative can also be defined to be the umbrella device, too. In this case, at least the root derivative and one additional device shall be tested completely against the specifications listed in 6.2.5.1.

6.2.5.5 Qualification test performance

For the qualification of 10BASE-T1S Transceiver device derivatives, this specification offers the following two options.

6.2.5.5.1 Case 1: Packaging

a. Derivate description, compared with umbrella / root derivate:
- Differences: package type, size and / or pinout,
- Commonalities: implementation of the Transceiver die, MII, MDI-/supply circuitry / filter and settings as well as functionality ranges / feature set and operation parameters (e.g. temperature and voltage range).

b. Options for action:
- Ensure that device derivatives are subsets of umbrella / root derivative in matters of functionality ranges / feature set and hardware,
- Migration of all root / umbrella derivative qualification test results listed in 6.2.5.1,
- Re-evaluate performance of EMC- / ESD – Tests according to [7] OPEN ALLIANCE: IEEE 10BASE-T1S Transceiver EMC Specification.

6.2.5.5.2 Case 2: Bonding

a. Derivate description, compared with umbrella / root derivate:
- Differences: reduced bonding, e.g. reduced number of MDI – ports,
- Commonalities: implementation of the Transceiver die, MII, MDI-/supply circuitry / filter and settings as well as, package type, size, pinout as well as remaining functionality ranges / feature set and operation parameters (e.g. temperature and voltage range).

b. Options for action:
- Ensure that device derivatives are subsets of umbrella / root derivative in matters of functionality ranges / feature set and hardware,
- Migration of all umbrella / root derivative´s result from qualification tests listed in 6.2.5.1,
- Re-evaluate performance of EMC- / ESD Tests according to [7] OPEN ALLIANCE: IEEE 10BASE-T1S Transceiver EMC Specification.

6.2.5.6 Documentation

For safeguarding and traceability reasons, all documentation within practical usages shall be binding. First of all, this must be applied for the identification of potential derivate options e.g. by datasheet descriptions.

All affected qualification test reports must document:

- technical commonalities of and differences between 10BASE-T1S Transceiver devices (derivatives) under test and root / umbrella devices,
- motivation for selection derivative and umbrella / root devices,
- references to binding documents,
- complete test results of devices (derivatives) under test and umbrella / root devices
- and test setup differences

6.2.5.7 Practical usage: PHY, Switch and SoC device derivatives

In the following section there are several basic assumptions on the development of the different devices. Based on these assumptions the approaches for the qualification of device derivatives are different.

6.2.5.7.1 PHY device derivatives

The PHY is in most cases the basic device for any semiconductor vendor of Ethernet related products. Once a PHY is realized and about to be introduced on the market, there are almost no major changes encountered.

Thus, following Table 2 for reduced testing shall be used:

Differences between DUT and umbrella device	**PCS Test**	**PLCA-Test**	**PMA Test**	**EMC ESD**	**IOP**	**Switch Test**	**ECU-Test (applicable for Tier1 suppliers)**	
Package				X		n/a		-No different Feature -No new functionality
All other	X	X	X	X	X	n/a	X	

Table 2: PHYs - Test cases on derivative differences

Note:
Explicitly: All changes to transceiver block including initialization settings (scripts) need a re-run of all tests. Modifying scripts is seen as a major change which requires complete re-testing against the complete specifications.

6.2.5.7.2 Switch device derivatives

The procedure is most important to Switch devices. Switch devices have been seen in the past in the form that basically the same product was put on the market in different packages, with different number of ports.

Differences between DUT and umbrella device	PCS Test	PLCA-Test	PMA Test	EMC ESD	IOP	Switch Test	ECU-Test (applicable for Tier1 suppliers)	
Package				X				-No different Feature -No new functionality
PHY-independent Switch features						X	X	Enhancement of networking capabilities, whereas the technology, functionality and IP of the integrated PHYs are the same
Reduced number of ports				X				-No different feature -No new functionality
All other	X	X	X	X	X	X	X	

Table 3: Switches - Test cases on derivative differences

Note:
In case of Switch devices having several identical PHY instances (except for the PHY address) and identical BIN, then the conduction of conformance testing as defined in [3], [4] and [5] shall be required only for one PHY.

Note:
The term networking capability summarizes all switch-dependent features like, VLAN handling, QoS-features, filtering-capabilities, speed of the switching fabric (switching-rate), etc. The technology, functionality and IP of the integrated PHY are to be the same.
Changing the switching fabric (higher switching-rate) might affect the EMC performance of the die.

Note:
An example for this approach might be a family of Switch products based on a single silicon device and appear on the market as 7 port, 5 port and 3 port devices.

Here the testing of the device which allows the tests of all features will be sufficient.

Note:
The re-assignment of pins to a different function available in the silicon, but not seen on devices in a previous test will need a complete re-test.

Example: Changing via bond-out or other configuration method other interfaces e.g. MDIO, MII not seen exactly in the same function in a previous test need a complete re-test.

6.2.5.7.3 SoC device derivatives

Systems on Chip (SOC) derivates may appear in very different forms. If SOC derivatives cannot be handled in the same manner as other 10BASE-T1S – Transceiver devices, e.g. reduced bonding, all SOC derivatives must be tested completely and evaluated separately.

6.3 ECU requirements

6.3.1 Functional implementation requirements

An ECU incorporating one or more 10BASE-T1S interfaces shall satisfy the requirements listed in Chapters 6.3.1.1 to 6.3.1.3 in terms of functional behaviour and diagnostic functionality.

6.3.1.1 Wake-up requirements

The system timing requirements provided in [12] (OPEN ALLIANCE: Sleep/Wake-up Specification for Automotive Ethernet) are valid.

6.3.1.2 Diagnostic requirements

The registers defined in [13] shall be accessible and their behaviour shall be according to the requirements defined in [13] (OPEN ALLIANCE: 10BASE-T1S Advanced diagnostic features for automotive Ethernet PHYs.

6.3.1.3 Evaluation/testing capabilities for ECUs

To allow evaluation of ECUs, the 10BASE-T1S Test Mode functionality with Test Modes 1 to 4 shall be implemented for each 10BASE-T1S interface of the ECU. (Refer to [1] for description of the test modes). See also Chapter 5.4.1.3 Evaluation/testing capabilities for integrated circuits.

6.3.2 Additional tests requirements

The following tests from [8] (OPEN ALLIANCE: Automotive Ethernet ECU Test Specification) shall be conducted for analysis of the physical layer behaviour (Further higher layer test may be required as well):

Reference	Test	Requirement	Remarks
[8] ; [1] subclause 147.5.2 ; 147.5.4.1	Check the Transmitter Output Voltage.	Mandatory	--
[8] ; [1] subclause 147.5.2; 147.5.4.2	Check the Transmitter Output Droop	Mandatory	--
[8] ; [1] subclause 147.5.2; 147.5.4.3	Check the Transmitter Timing Jitter	Mandatory	--
[8] ; [1] subclause 147.5.2; 147.5.4.4	Check the Transmitter Power Spectral Density (PSD) up to 250 MHz.	Mandatory	See Chapter 6.3.2.1 Extended Transmitter PSD Mask (Multidrop)
[8] ; [1] subclause 147.5.4.5; 147.9.2	Check the Transmitter High Impedance	Mandatory	The impedance at MDI must be higher than the parallel combination of [2*R_{CMT} ; 10 kΩ ; 25 pF].
[8]	Check the Transmitter rise/fall timing	Mandatory	see Chapter 6.3.2.2 Transmitter rise/fall time slope at MDI (send mode)

Table 4: Additional required tests on ECU-level

6.3.2.1 Extended Transmitter PSD Mask (Multidrop)

In contrast to the IEEE, an extension for the upper limit of the PSD mask from 40-250 MHz is specified. See Figure 5 Extended Transmitter PSD Mask (Multidrop).

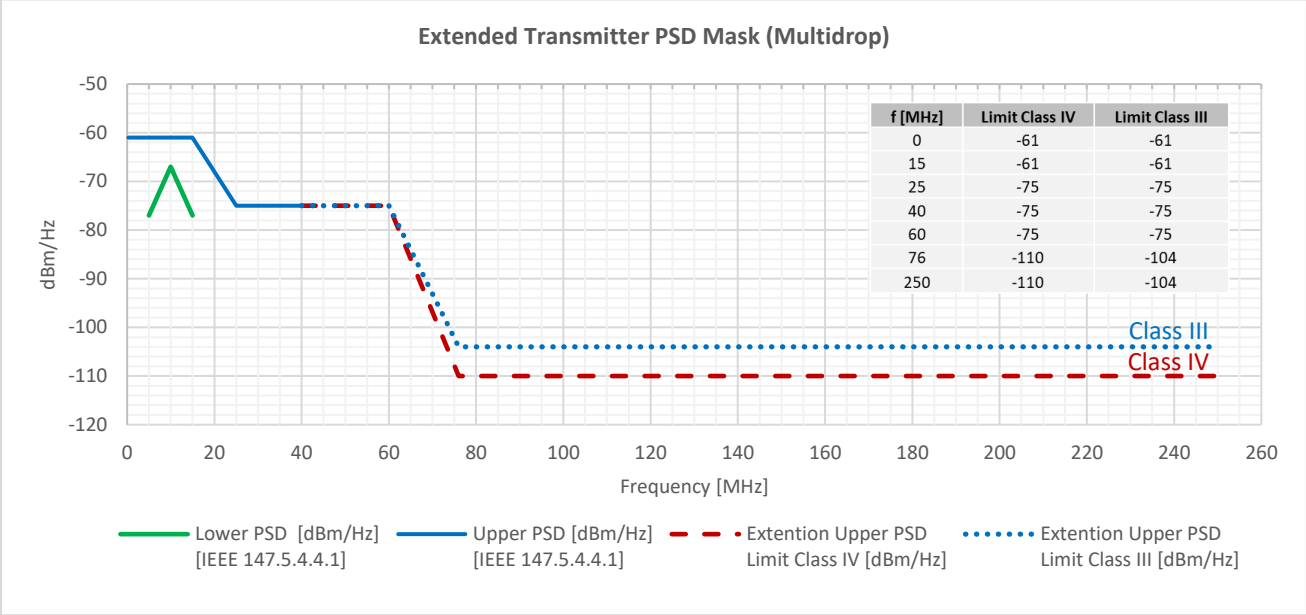


Figure 5: Extended Transmitter PSD Mask (Multidrop]

6.3.2.2 Transmitter rise/fall time slope at MDI (send mode)

Valid for PHYs and Switches. For PMD-Transceiver t_{rise}/t_{fall} time is specified in the transceiver interface specification [18].

6.3.2.2.1 Rise/fall time for transmitter (send mode)

		MIN	MAX
t_{rise}/t_{fall}	20% - 80%	7.5 ns	15 ns

Table 5: Rise/fall time for transmitter at MDI

6.3.2.2.2 Test conditions

Load	50 Ω || 15 pF

Table 6: Test conditions at MDI

6.3.2.3 V_{LINE}-R_{SE} specification

6.3.2.3.1 General

Due to resonance effects, with some specific combinations of component parameters, the common mode voltage at PHY transceiver pins may get higher than the one applied at MDI interface for certain frequency range (specifically: 1 to 5 MHz). On Figure 6, the relevant parameters are depicted as part of the equivalent circuit.

It was projected, that when the resonant voltages get higher than the operating common-mode range (or also when operated in OFF/Power down state) of a specific compromised transceiver mode conversion can be generated, due to non-linearity (asymmetric clipping) effects.
The mode conversion leads to significant differential noise contribution that can spread on the bus and impair communication not only on compromised device, but also on the rest of the bus.

System designer can apply analytic (based on theoretical assessment) and/or empirical (based on actual measurement) approach to address this issue.

The following sections describe the analytical method with its intended application scenario, as well as two related measurement methods. Those can also be used not only as means of empirically evaluating the effects of the mode conversion under CM stress, but also as example how to obtain the important R_{SE} parameters.

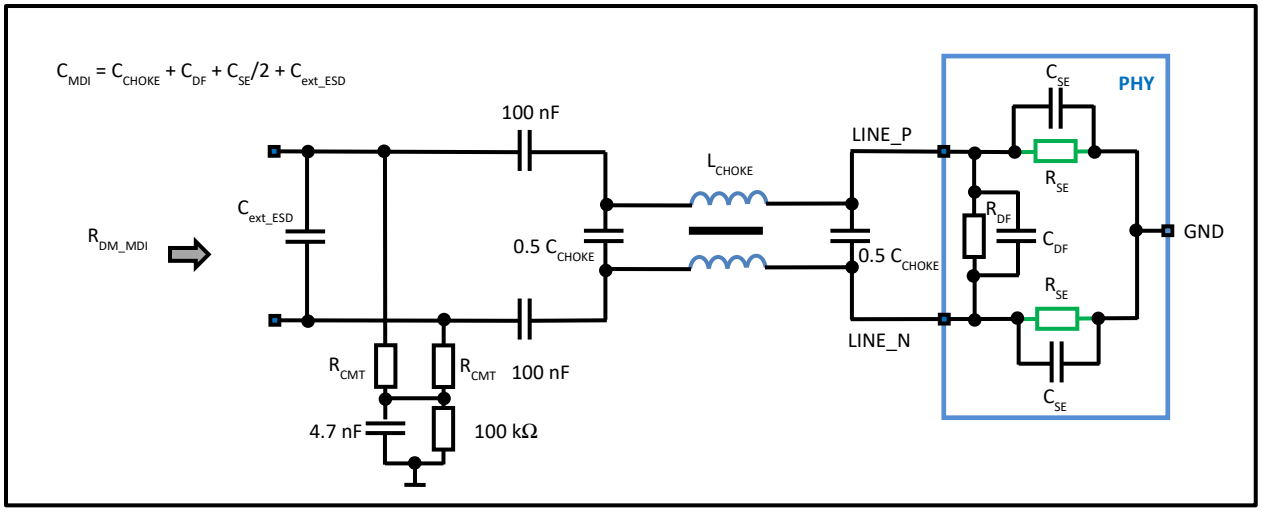


Figure 6: Principle of a node circuit

6.3.2.3.2 Analytical methods

This method utilizes limits, extracted from theoretical assessment of the magnitude of the resonances. It calls for using transceiver with linear operating range that is aligned to (i.e. wider than the limit set for) its specific single-ended input impedance.

Figure 7 depicts the dependency of the required linear common mode-operating range (V_{LINE}) vs. single ended resistive component (R_{SE}) and contains the respective formulas.

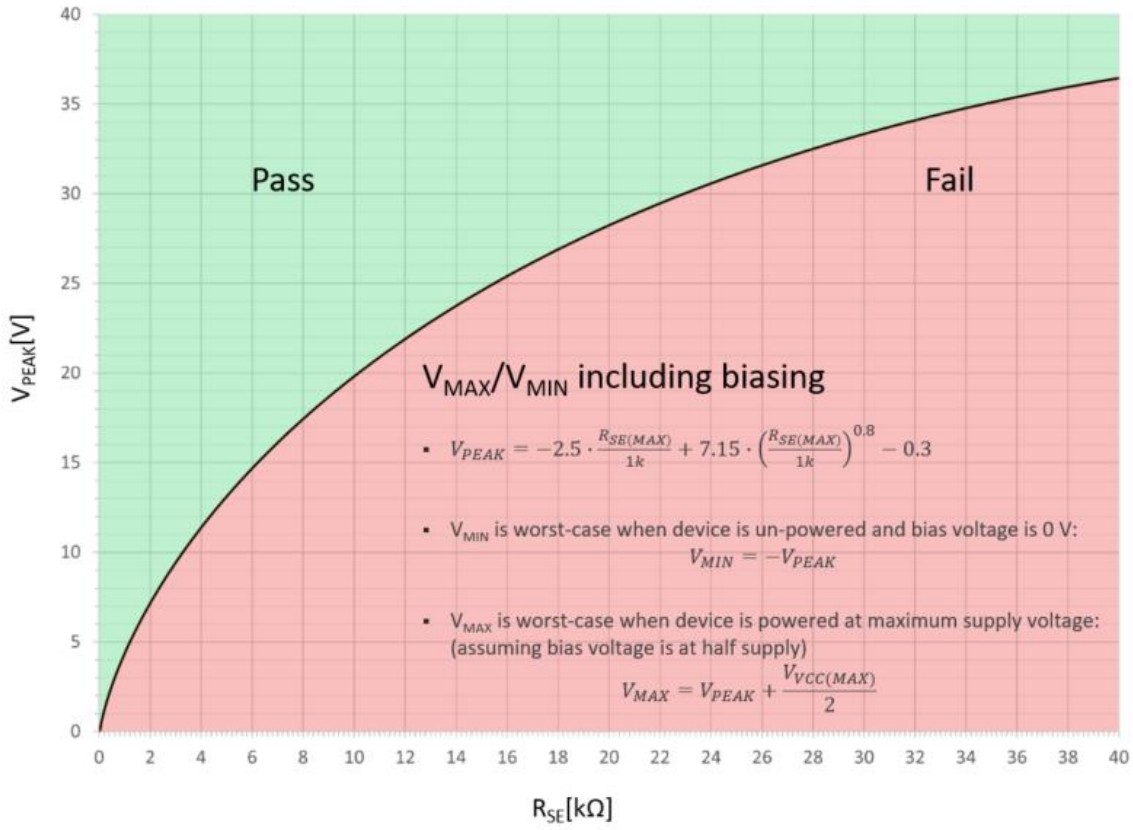


Figure 7: V_{PEAK}/R_{SE} specification 200µH / Class III CMC

A system designer should look for the following definitions in transceiver section of the datasheet of the selected line interface IC (PMD Transceiver/PHY/MACPHY/Switch):

- Single Ended Impedance (R_{SE}) – max value (must be valid at least in the frequency range 1-5 MHz)
- Operating CM Range – min and max value

This statement mentioned above does not preclude any technology even if there is clipping as long as the distortion test is satisfied.

Regardless of the technologies that are used in the implementation, the PHYs have to pass the distortion tests that will be defined in the EMC specification [7].

6.3.2.3.3 Practical methods

See appendix Chapter 9.3

6.4 Differential end termination

The differential end termination is seen as an element, which has an influence on the communication channel and is specified in more detail in this section.

Differential end termination can be executed in following ways:

a) Electrical termination circuit included in a single stand-alone termination unit at the mixed segment end in a harness.
b) Like the termination unit mentioned in a) but the termination circuit is integrated in any already available ECU for avoiding that additional stand-alone unit.
c) Electrical termination circuit as a part of a 10BASE-T1S End Node interface as shown in Figure 8 and Figure 4 Interface circuitry/schematic for 10BASE-T1S.

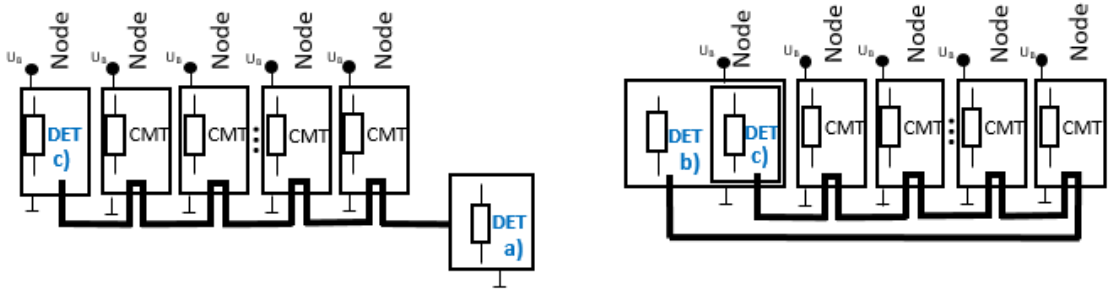


Figure 8: Variants of differential end termination execution

The differential end termination shall fulfill following requirements.

6.4.1 Differential end termination component requirements

R_1, R_2	**Resistor**)[2;5] 50 Ω (DET) **Tolerance** ≤ 1 % (even after ESD test) **Nominal power** ≥ 0.4 W)[4]	DET: Differential end termination The resistors need sufficient ratings. The specified minimum power rating of R1 and R2 is a recommended target value for the typical usage in an automotive area. In the case of more favorable boundary and test conditions, this value can be correspondingly adjusted.
R_3	**Resistor**)[2;3;5] 100 kΩ **Tolerance** ≤ 10% **Nominal power** ≥ 0.1 W	To avoid static charge of the cable harness.

C_3	**Capacitor**)[2;3;5] 4.7 .. 100nF **Tolerance** ≤ 10% **Voltage range** ≥ 50 V)[1]	100nF)[4] The capacitor need sufficient electrical strength.

)[1] According to car manufacture specifications for supply voltages ≥56V voltage range for 48V electrical systems, typically 100V min. electric strength recommended for ceramic caps. For 12V systems typ. 50V electrical strength is sufficient.

)[2] It is required to follow the definitions of semiconductor manufacturer for external passive components and circuit, software configuration (script) and software flow definitions, which are defined in datasheet and application notes.

)[3] Optional if included in the harness.

)[4] Recommended target value

)[5] Schematic see Figure 4

Table 7: Differential end termination component requirements

6.4.2 Requirements for mode conversion loss

The mode conversion loss requirements are specified in this section because the differential end termination is seen as an element, which has an influence on the communication channel.

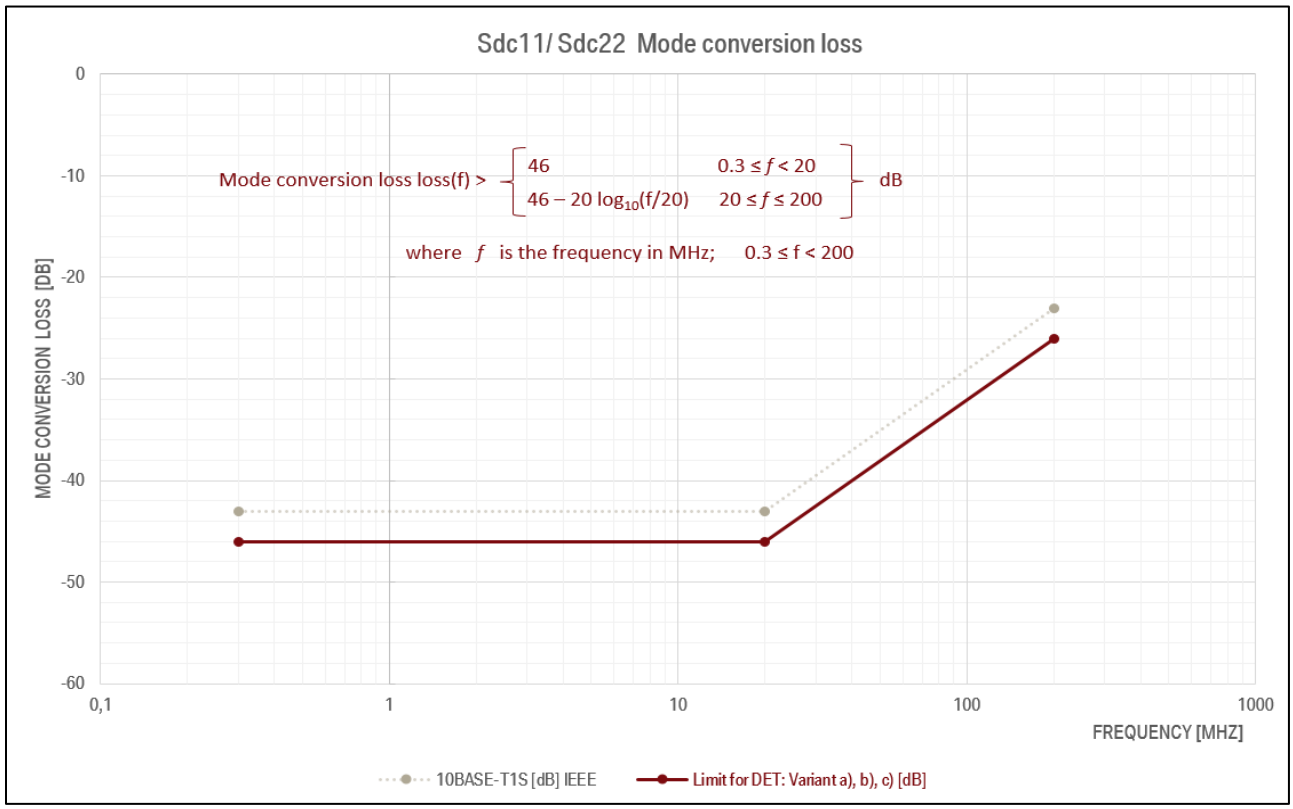


Figure 9: Mode conversion loss

6.4.3 Requirements for return loss

The return loss requirements are specified in this section because the differential end termination is seen as an element, which has an influence on the communication channel.

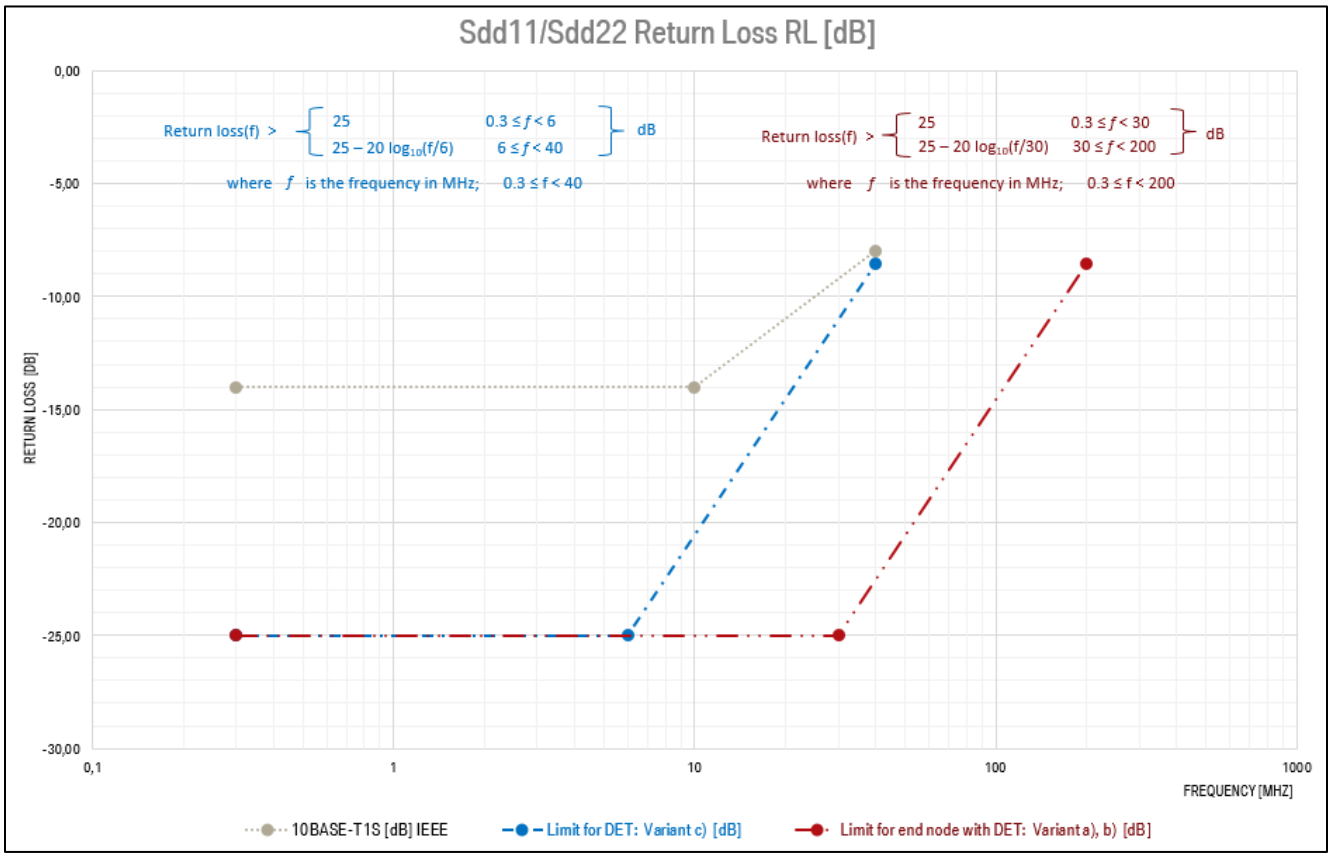


Figure 10: Return loss

6.5 Cable harness and connector recommendations for 10BASE-T1S

To allow a proper operation of the implemented interface, all 10BASE-T1S parts within a cable harness assembly implementation shall fulfill the channel requirements of [11].

Therefore all components of the channel shall be designed and assembled to ensure the required RF parameters.

7 System test environment definition

7.1 General

This definition shall be used for defining a test wiring harness that simulates various communication channels according to the channel definitions of IEEE Std. 802.3cg™ [11] for tests of 10BASE-T1S transceivers according to [3], [4],[5], [6] and [8]. These Chapters also contain examples for a practical implementation.

7.2 Channel Type 1 P2P

7.2.1 General

The Type 1 channel is derived from a **25m** mixing segment without stubs. The parameters of the type 1 channel are derived from the limit definition for a communication channel according to IEEE P802.3cg™ [1] and [11] OPEN Alliance TC9 definitions for 10BASE-T1S communications channel. For setting up a real test harness upper and lower limits are added for each parameter. The type 1 channel implementation shall fulfill these limits at (23±2)°C ambient temperature (RT = Room Temperature).

NOTE: For cable type reference, within the body of this document: "Type 1" cable refers to automotive grade jacked unshielded twisted pair (UTP) cable 10BASE-T1S.

7.2.2 Required parameters

The parameter and limits given in
Table 8 are defined for a type 1 channel implementation.

7.2.3 Example for Type 1 channel implementation

Figure 11 shows the topology of the example type 1 channel implementation. The description of each part of this implementation is given in Figure 11, Figure 12 and Table 8.

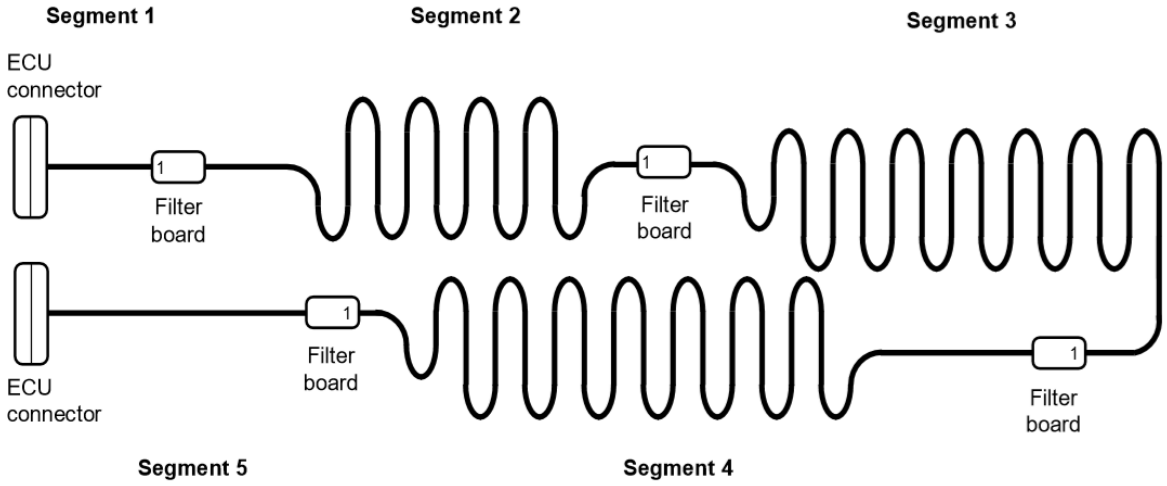
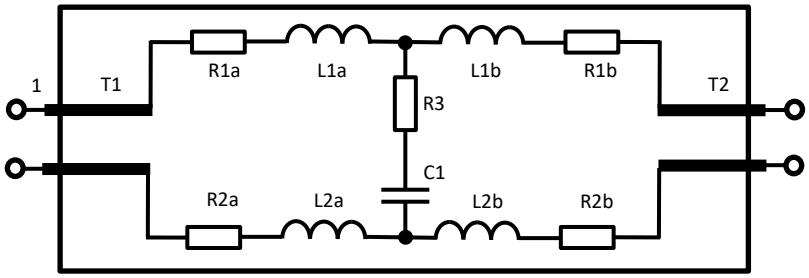


Figure 11: Example for channel type 1 implementation - P2P

Part	Description	Type
ECU connector 1	2 pin MQS connector or equivalent	MQS or equivalent see Figure 11 and Chapter 5.4.3
Segment 1	3.5 m cable	FLKCUMGU9Y-9Y 2x0.13QMM-T105 / Krocar 64996795 or equivalent jacketed cable
Filter board	RLC filter board with line impedance compensation	see Figure 12
Segment 2	0.75 m cable	Same as segment 1
Filter board	RLC filter board with line impedance compensation	see Figure 12
Segment 3	13.0 m cable	Same as segment 1
Filter board	RLC filter board with line impedance compensation	see Figure 12
Segment 4	0.75 m cable	Same as segment 1
Filter board	RLC filter board with line impedance compensation	see Figure 12
Segment 5	3.5 m cable	Same as segment 1
ECU connector 2	2 pin connector	Same as ECU connector 1

Table 8: Example for channel type 1 implementation – Parts



Legend:

R1a; R1b, R2a, R2b:	0,5 Ω (± 1%)
L1a, L1b, L2a, L2b:	30 nH (Coilcraft 0603CS-30NXGLW)
C1:	4.7 pF (± 5%)
R3:	10 Ω (± 1%)
T1, T2:	matched line 25mm length, $Z_{differential}$ = 120 Ω (±5%)

Figure 12: Example for channel type 1 implementation - Filter board

7.3 Channel Type 2 (mixing segment)

7.3.1 General

The Type 2 channel is derived from a **25m** mixing segment. The parameters of the type 2 channel are derived from the limit definition for a communication channel according to IEEE P802.3cg™ [1] and [11] OPEN Alliance TC9 definitions for 10BASE-T1S communications channel. For setting up a real test harness upper and lower limits are added for each parameter. The type 2 channel implementation shall satisfy these limits at (23±2)°C ambient temperature (RT = Room Temperature).

NOTE: For cable type reference, within the body of this document: "Type 2" cable refers to automotive grade unshielded twisted pair (UTP) cable for 10BASE-T1S.

7.3.2 Required parameters

The parameter and limits given in [16] are defined for a type 2 channel implementation.

7.3.3 Example for Type 2 channel implementation (8 nodes)

Figure 13 shows the topology of the example type 2 channel implementation.
The description of each part of this implementation is given in Figure 13 and Table 9.

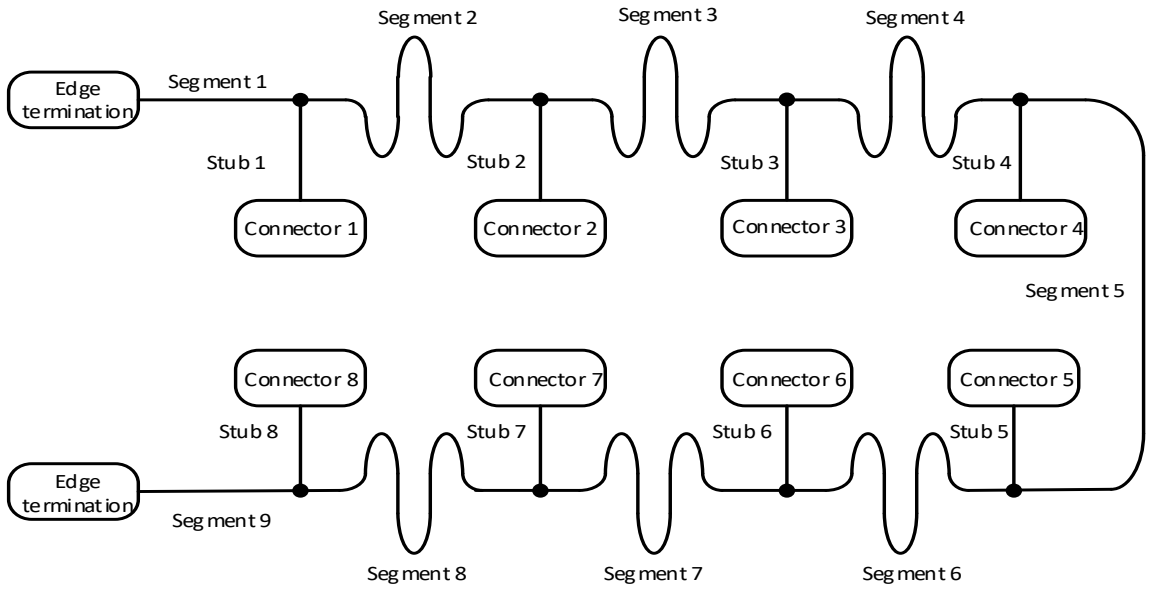


Figure 13: Example for channel type 2 implementation - Topology

Part	Description	Type
Termination	Differential end termination (100Ohm±1%)	see Figure 4 and Chapter 6.4
Segment 1; 9	<0,3 m cable	FLR9Y 2*0,35 QMM-SN SL13 KroSchu 64996567 or equivalent
Segment 2	4 m cable	same as segment 1
Segment 3	2 m cable	same as segment 1
Segment 4	4 m cable	same as segment 1
Segment 5	0.5 m cable	same as segment 1
Segment 6	0.5 m cable	same as segment 1
Segment 7	13.5 m cable	same as segment 1
Segment 8	0.5 m cable	same as segment 1
Stub1-8	0,1m cable	same as segment 1
Connector 1- 8	Connector	MQS or equivalent see Figure 13 and Chapter 5.4.3

Table 9: Example for channel type 2 implementation - Parts

8 Appendix 1: Test documentation examples

8.1 DUT configuration documentation example

Item	Type	Source	Comment
DUT	PHY -0816 -Test board	Fa. Hell-COM	
Cable	0.35 PP	Longwire&Copper.com	
Transceiver	80-0815	Hell-COM	10BaseT1S;
Layout		App-Note AN-12345	Hell-Com.com\Ap_Note.. 24.12.2021
Script	10Base Operation	Script	Hell-Com.com\Ap_Note\Script\10Base_operation_V.01 xx.xx.2020
L1	ABG-8147	General Inductors	100µH
R1, R2	1K	Best_Ohm AG, Serie 4711, 0805	100V
C1, C2	100nF		

Table 10: Example for test circuitry documentation

8.2 DUT feature documentation example

DUT Feature	YES	NO	Comment
TEST Mode 1	x		
TEST Mode 2	x		
..			See deactivated short
TEST Mode 4			
Deactive signal front end / termination on		x	Allow termination, if.. (explain what to do or why there is an exception..
Ready Status Register		x	Check ..xyz AND abc instead
Detect short		x	Not in this silicon
..			
CRC / symbol failures	x		
..			
End Termination detection		x	Not in this silicon

Table 11: Example for feature availability documentation

9 Appendix 2: Evaluation of a 10BASE-T1S system, based on signal criteria at ECU bus pins

9.1 Eye mask criteria of 10BASE-T1S

One of the first practical criteria for 10BASE-T1S system evaluation is to check the bus signal eye diagram at every 10BASE-T1S nodes by using the eye mask criteria which is shown in Figure 14 and Table 12.

Eye mask criteria	Parameter value	Comment
Eye-height	-30mV and +30mV	Measured at MDI
Eye-width	≥ 25 ns	Measured at MDI
Jitter	≤15 ns	Measured at MDI Depending on rise/fall time of transmitters and mixed segment (i.e. reflexions superposition)

Table 12: Eye mask criteria

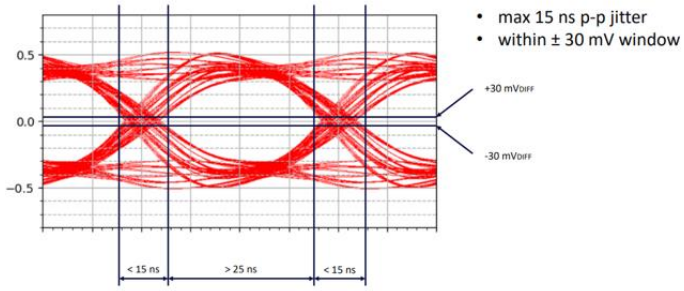


Figure 14: Eye mask criteria

A method to estimate the max. possible EMC induced (Differential / Alien) noise, the 10BASE-T1S system can handle, can be estimated by comparing the minimal p-p height distance of eye diagram of the unstressed signal subtracted by the p-p eye-width window.

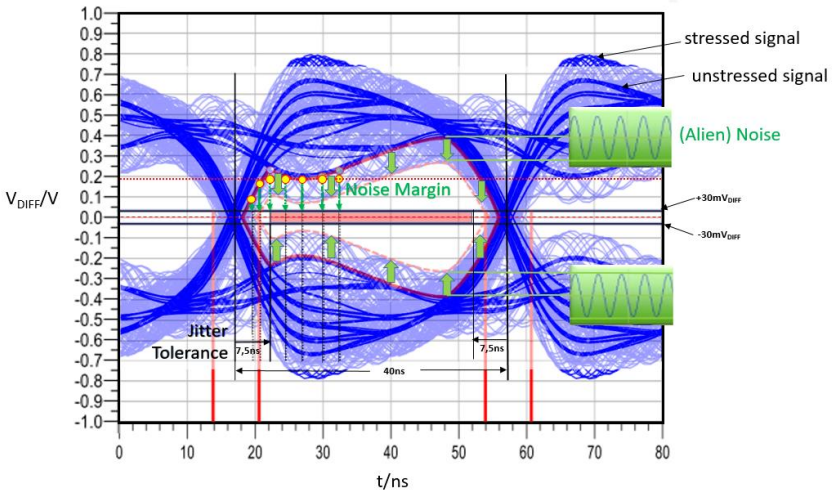


Figure 15: Noise margin

For automotive system, an experience value is to have at least more than 200mVpp as a Differential / Alien noise margin.

9.2 No carrier / idle detect window criteria of 10BASE-T1S

No Collision detect criteria	Parameter value	Comment
No carrier / idle detect inside window	300mV$_{pp_diff}$ for longer than 300ns	Measured at MDI

Table 13: No carrier / idle detect criteria

9.3 Transceiver common-mode range

9.3.1.1 Method #1

This method utilizes bridge-type architecture. The bridge is formed by two external measurement resistors and the two equivalent IC level impedances, as shown on Figure 16.

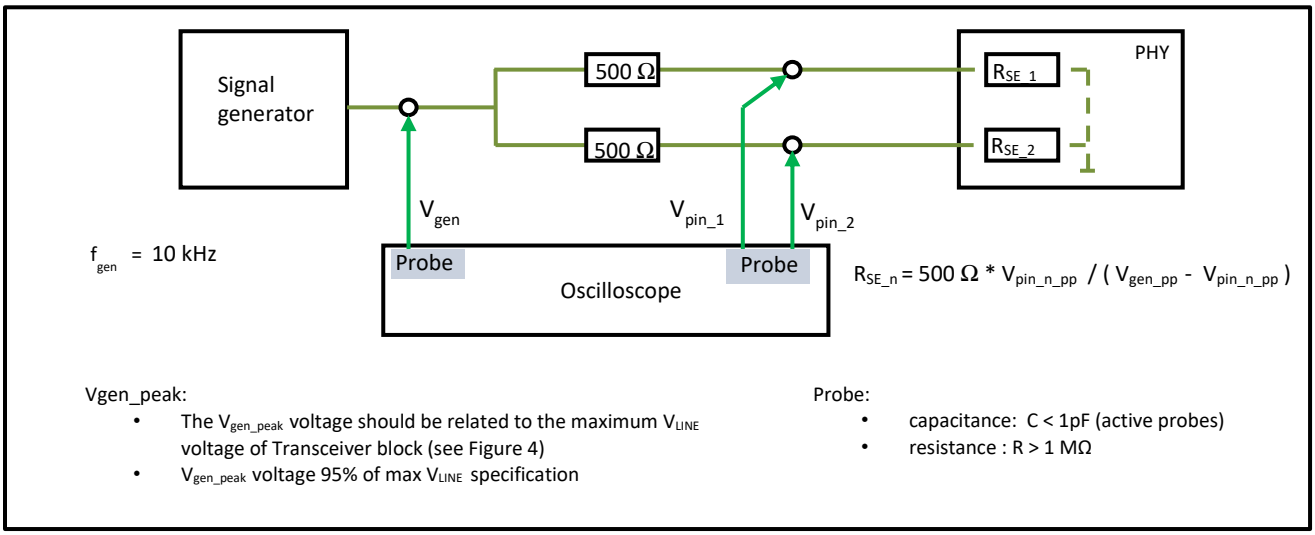


Figure 16: Measurement setup method #1

This method can be used either to determine the resistive single ended component of the impedance of the Transceiver IC or to evaluate the (presence or absence of) mode conversion effect.

The measurement resistors used must be of measurement grade (i.e. matched to 0.1%) and the setup shall be built under of the directive of matching parasitic components. That includes careful test PCB design, as well as selection of well-matched probes and oscilloscope channel matching (skew, level, offset) adjustments.

All voltages (applied and measured), used in the formulas are peak-to-peak values. R_{SE} can be calculated using the formula shown in Figure 16.

Additionally, mode conversion generation can be evaluated by this setup – in this case
Vdiff = Vpin_1 – Vpin_2.

9.3.1.2 Method #2

This method utilizes BALUN/Transformer to provide common/differential-mode separation, as shown on Figure 17.

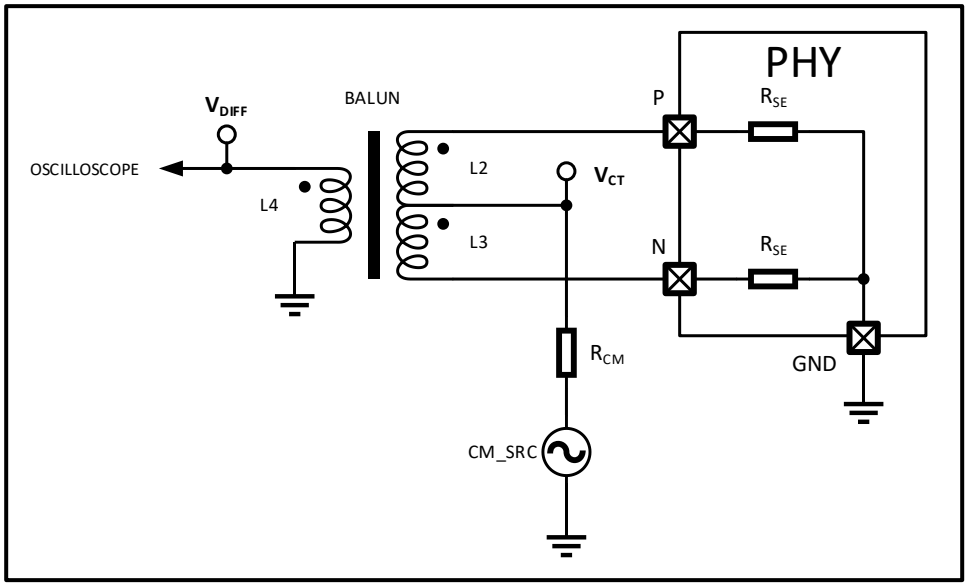


Figure 17: Measurement setup method #2

This alternative method can equivalently be either used to determine the resistive single ended component of the impedance of the Transceiver IC or to evaluate the (presence or absence of) mode conversion effect.

The center-tap of the transformer/BALUN provide the common mode connection to the PHY line interface. The common mode impedance of the PHY is split (i.e. parallel combination) through the P and N connection to GND. The current flowing through both on-chip R_{SE} impedances is causing voltage drop over the measurement resistance R_{CM}. Thus:

$$R_{SE} = 2 * R_{CM} * V_{CT\_PHY} / (V_{CT\_OPEN} - V_{CT\_PHY}),$$

where:

- R_{CM} is the measurement resistance (including the generator/source internal resistance), typically 250 Ohm (200 Ohm external resistor + 50 Ohm generator source impedance)
- V_{CT_OPEN} is the amplitude measured at the center-tap of the transformer/BALUN, with no PHY (i.e. open)
- V_{CT_PHY} is the amplitude measured at the center-tap of the transformer/BALUN, with PHY connected

Presence of mode conversion effects can be detected/measured at the DIFF side of the Transformer/BALUN. It must be considered that the setup will have its own small mode conversion contribution, due to non-ideal balancing, which must be minimized and considered when evaluating the PHY contribution.

Expected is that within the operating range (V_{CM_OP}) of the PHY there will be no significant V_{DIFF} contribution from it.