IEEE 10BASE-T1S EMC Test Specification for Common Mode Chokes

Version 1.0

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This EMC measurement specification shall be used as a standardized common scale for EMC evaluation of common mode chokes for 10BASE-T1S applications.

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Introduction

The IEEE 802.3cg standard defines a 10 Mbit/s Ethernet communication over an unshielded single pair of conductors and separate the two systems 10BASE-T1S and 10BASE-T1L. The 10BASE-T1S implementation covers a half duplex communication using a CSMA/CD for point to point channel and the optional functionalities full duplex communication for a point to point channel and a half duplex communication for a so called mixing segment (or multidrop mode) with at least 8 nodes and 25 m length of bus lines. In any case, the bus cable is terminated with the line impedance of 100 Ω at both ends of the channel. As an optional feature to enable a deterministic access time for each bus node in a mixing segment the new access method PLCA is overlaid to the CSMA/CD system.

Due to the high communication rate of 10BASE-T1 and the intended use of unshielded twisted pair cable, a high risk of EMC problems is expected. For this reason, an EMC optimization of all components of the Ethernet physical layer is required.

A CMC is used as part of a 10BASE-T1S MDI interface circuit and has a strong impact to the functional and EMC behavior of the complete system. This EMC measurement specification is focused on evaluation of the CMC characteristics related to high frequency and functional aspects as well as ESD.

Abbreviation/Symbols

CDMR	*Common to Differential Mode Rejection, common mode single ended measured*
CMC	*Common Mode Choke*
DCMR	*Differential to Common Mode Rejection, common mode single ended measured*
IL	*Insertion Loss*
RF	*Radio Frequency*
RL	*Return Loss*
S-Parameter	*Scattering Parameter*
VNA	*Vector Network Analyzer*
TLP	*Transmission Line Pulse*

1 Scope

This document specifies test and measurement methods for characterization of CMCs intended to be used for Ethernet interfaces for 10BASE-T1S. It contains definitions for test methods, test conditions, performance criteria, test procedures, test setups, test boards and recommended limits and covers

- parasitic capacitance;
- S-parameter measurement mixed mode;
- ESD damage test;
- saturation test at RF disturbances;
- saturation test at ESD.

This document does not cover devices that are intended for use in power over data line applications.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

[1] IEEE P802.3cg™: Physical Layer Specifications and Management Parameters for 10 Mb/s Operation and Associated Power Delivery over a Single Balanced Pair of Conductors

[2] IEC 62615, Electrostatic discharge sensitivity testing – Transmission line pulse (TLP) – Component level

[3] ISO 10605, Road vehicles – Test methods for electrical disturbances from electrostatic discharge

3 Terms and Definitions

For the purposes of this document, the terms and definitions given in 2 and following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- ISO Online browsing platform: available at https://www.iso.org/obp;
- IEC Electropedia: available at http://www.electropedia.org.

4 General

The intention of this document is to evaluate the EMC performance of CMCs intended to use for 10BASE-T1S Ethernet interfaces. The final judgment of the tested device is left to the customer.

5 Test and measurement

5.1 General definitions

All tests are performed for standard room temperature (23 °C +/- 3 K).

In general, a printed circuit board with RF board-to-coax connectors should be used for all tests. To ensure reliable RF parameters, a test board with at least two layers with enlarged GND reference plane is required. The traces on the test board should be designed as 50 (± 5) Ω single ended transmission lines with a length as short as possible. For design of CMC footprint and the definition of minimal distance of CMC housing and CMC terminals to the GND plane the related specification of CMC manufacturer should be used, if not otherwise specified in the specific tests.

The test board design and the method of connecting the CMC with the test board is intended to provide high accuracy and reproducible test results and is with more details described in the respective measurement chapters.

A general electrical drawing with winding and pin definitions of a CMC is shown in Figure 5-1.

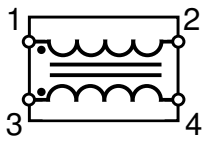


Figure 5-1: General electrical drawing of a CMC

For the measurements described below the CMC line 1 is defined as the CMC winding between pin 1 and pin 2 and line 2 is defined as the winding between pin 3 and pin 4.

5.2 Measurement of parasitic capacitance

5.2.1 VNA measurement method

5.2.1.1 Test setup

The test setup for measuring the parasitic capacitance consists of a VNA in combination with a special test board (adapter test board). The test board is included into the test setup during VNA calibration. The reference points for calibration are defined to the pads of CMC pins 1 and 3 at the test board.

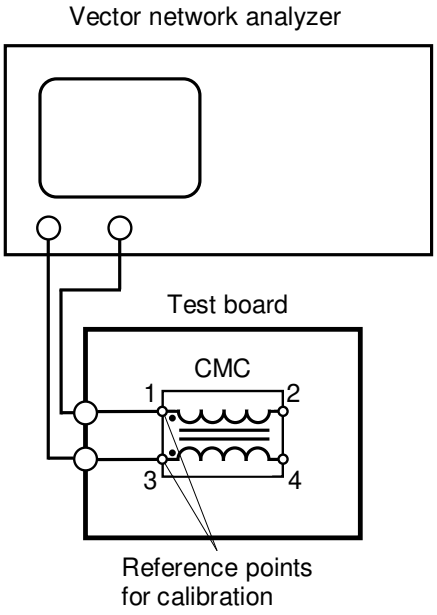


Figure 5-2: Test setup for parasitic capacitance measurement for VNA method

The test equipment definitions are the following:

- vector network analyzer;
- test board parasitic capacitance .

The connecting traces of the test board from RF connectors to CMC pins 1 and 3 should be routed symmetrically at 45° to decrease parasitic inductive coupling. The CMC pins 2 and 4 are unconnected. An example for test board is given in Figure 5-3 .

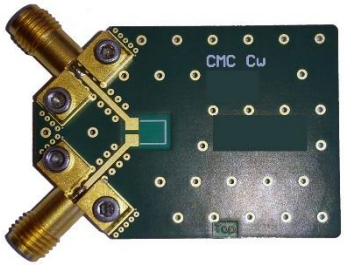
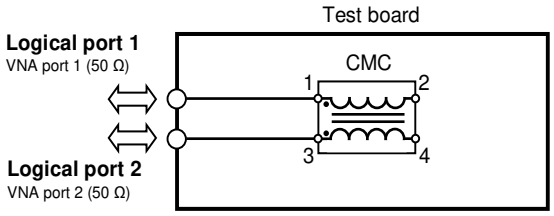


Figure 5-3: Example of test board parasitic capacitance measurement for VNA method, top layer

The test board symmetry and calibration accuracy should be validated with measurement of an open-circuit (without DUT). The remaining open-circuit capacitance should not exceed 500 fF.

5.2.1.2 Test procedure and parameters

The test procedure and parameters are defined in Table 5-6.

Item	Parameter
Frequency range:	1 MHz to 100 MHz
S-parameter per single path:	S_{11}, Re + j Im / CMC pin 1 S_{22}, Re + j Im / CMC pin 3 S_{21}, Re + j Im / CMC pin 1 to pin 3 S_{12}, Re + j Im / CMC pin 3 to pin 1
VNA measurement circuit:	port definitions: logic port 1: physical port 1 / CMC pin 1 logic port 2: physical port 2 / CMC pin 3 

Calculation method:	1. Calculate Y-Parameters from S-Parameters: $[S] = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \Longrightarrow [Y] = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}$ NOTE All calculations should be performed using raw or linearly interpolated data, to avoid inaccuracy introduced by e.g. spline interpolation or rational fitting. 2. Calculate the mean transfer Y-Parameter Y_T: $Y_T = \frac{(Y_{21} + Y_{12})}{2} = \frac{S_{12} + S_{21}}{50 \cdot (1 + S_{11} - S_{12} \cdot S_{21} + S_{22} + S_{11} \cdot S_{22})}$ 3. Calculate the parasitic capacitance C_{para}(f) while extracting the negative imaginary part of Y_T: $C_{para}(f) \approx \frac{Im(-Y_T)}{2\pi f}$ 4. The resulting value C_{para_max} is the maximum value of C_{para} (f) in the frequency range from f = 5 MHz to f = 15 MHz.

Table 5-1: Test procedure and parameters for parasitic capacitance measurements at CMC using VNA method

The tests should be performed at 10 samples and documented in a diagram with C_{para} (f) and C_{para_max} according to the scheme given in Table 5-2. Recommended limits for evaluation are given in A.1.

Test	Item	Sample
CP1	C_{para_max}	10 samples

Table 5-2: Required parasitic capacitance measurements for CMC

5.2.2 LCR meter or impedance analyzer measurement method

5.2.2.1 Test setup

The test setup for measuring the parasitic capacitance consists of a LCR meter or an impedance analyzer in combination with a special test fixture extension, direct mounted to the measuring device. The reference points for calibration are defined to the pads of CMC pins 1 and 3 at the test board.

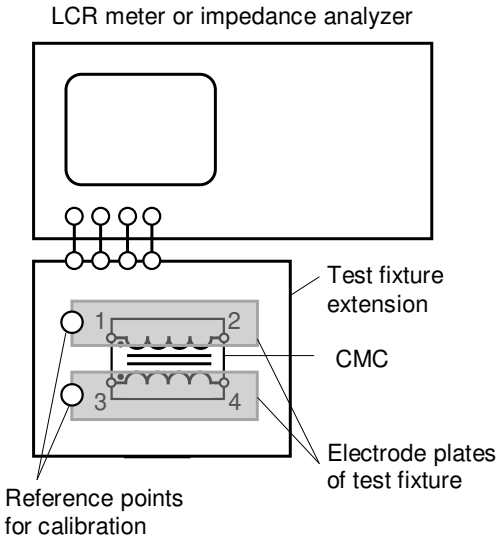


Figure 5-4: Test setup for parasitic capacitance measurement for LCR meter or impedance analyzer method

The test equipment definitions are the following:

- LCR meter or impedance analyzer;
- test fixture extension, direct mounted to the measuring device .

5.2.2.2 Test procedure and parameters

The test procedure and parameters are defined in Table 5-6.

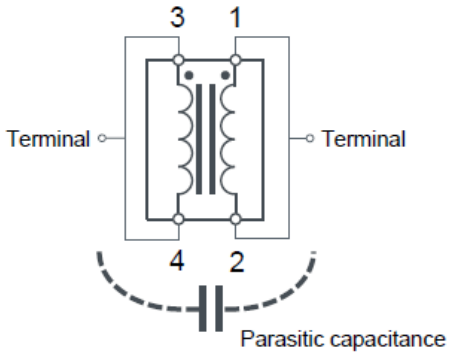
Item	Parameter
Test frequency:	5 MHz
LCR meter or impedance analyzer setting:	C_s
LCR or impedance analyzer measurement circuit:	

Table 5-3: Test procedure and parameters for parasitic capacitance measurements at CMC using LCR meter or impedance analyzer method

The tests should be performed at 10 samples and documented. Recommended limits for evaluation are given in A.1.

Test	Item	Sample
CP1	C_{para_max}	10 samples

Table 5-4: Required parasitic capacitance measurements for CMC

5.3 S-parameter measurement mixed mode

5.3.1 Test setup

The test setup for measuring the mixed mode *S*-parameters consists of a 4-port VNA in combination with a special test board (adapter test board). The test board is included into the test setup during VNA calibration. The reference points for calibration are defined to the pads of the CMC at the test board.

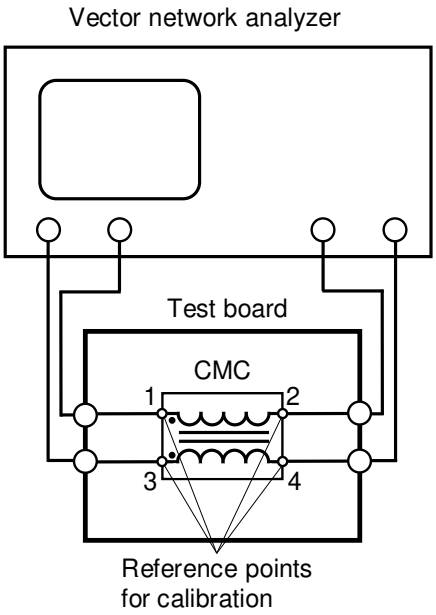


Figure 5-5: Test setup for S-parameter measurements

The test equipment definitions are the following:

- 4-port vector network analyzer;
- test board *S*-parameter mixed mode (4-port);
- test board *S*-parameter single ended (3-port).

For the *S*-parameter 3-port test board, additional specific requirements are defined. The 3-port test board with soldered RF connectors used for balance measurement should have a very high grade of self-balance. To ensure the test board self-balance characteristic of symmetrical network at logical port 2 (common mode), the traces between the DUT and all resistors (R1, R2 and R3) must be kept highly symmetric and as short as possible. To verify the test board self-balance characteristic, the test parameter and requirements given in Table 5-5are defined.

Examples for test boards are given in Figure 5-6 and Figure 5-7.

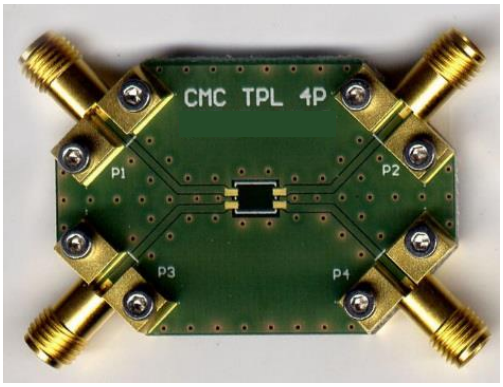


Figure 5-6: Example of test board 4-port S-parameter measurement at CMC – mixed mode, top layer

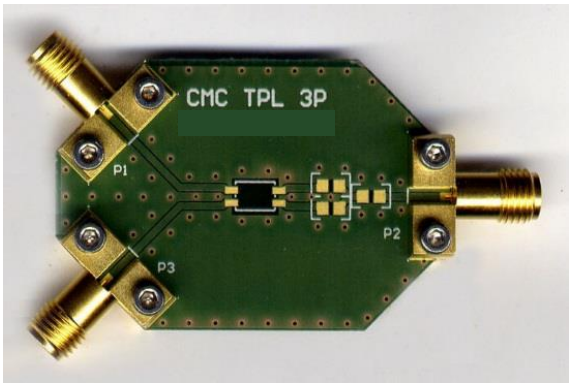


Figure 5-7: Example of test board 3-port S-parameter measurement at CMC – single ended, top layer

The reference points for calibration are the pads of the CMC footprint at the test board.

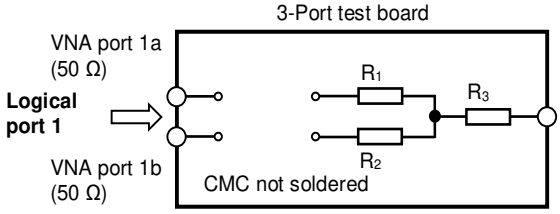
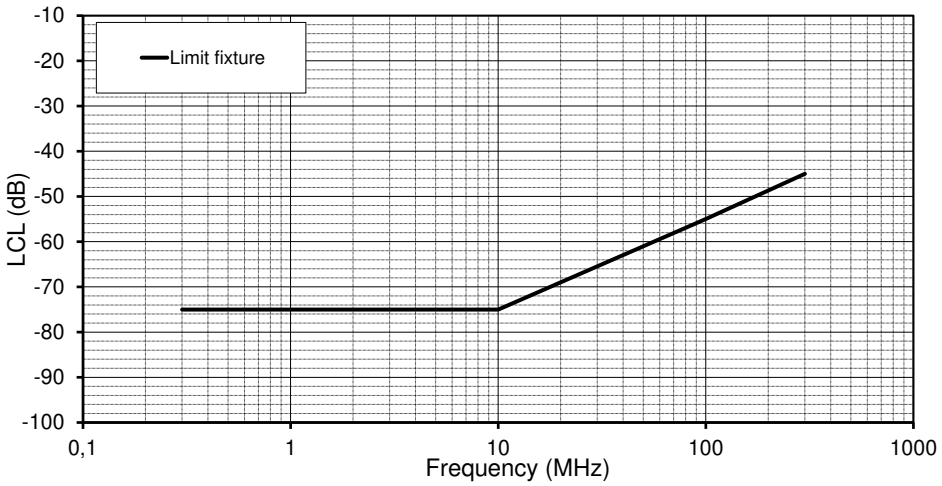
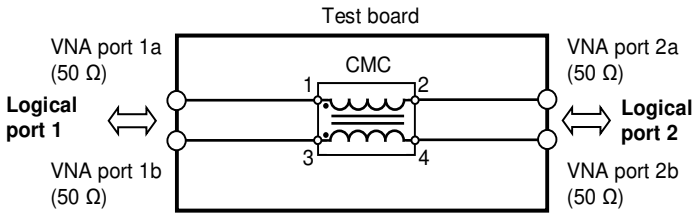
Parameter	Description
Frequency range:	0.3 MHz to 1 GHz
S-parameter:	S_{dc11} (LCL), logarithmic magnitude in dB / differential port side of 3-port test board.
VNA measurement circuit:	port definitions: mixed mode logic port 1: physical port 1a and port 1b differential mode input (logical port 1): 50 Ω impedance each  R = 49,9 Ω for R_1 and R_2 R = 124 Ω for R_3 The CMC should not be populated at the test board for self-balance measurement.
Requirement for 3-port CMC fixture:	**S - Parameter / CMC for Ethernet 10BASE-T1S** Item: Self-balance requirement for 3-Port test fixture Longitudinal Conversion Loss / LCL (S_{cd11}) [MHz] / Limit fixture: 0,3 / -75; 10 / -75; 100 / -55; 300 / -45 

Table 5-5: Test procedure and parameters for 3-port test board characterization for CMC

5.3.2 Test procedure and parameters

The test procedure and parameters are defined in Table 5-6.

Item	Parameter
Frequency range:	0.3 MHz to 1 GHz
S-parameter per single path:	4-port parameters S_{dd11} (RL), logarithmic magnitude in dB / CMC orientation 1 S_{dd22} (RL), logarithmic magnitude in dB / CMC orientation 2 S_{dd21} (IL), logarithmic magnitude in dB S_{cc21} (CMR), logarithmic in dB 3-port parameters S_{sd21} (DCMR), logarithmic magnitude in dB / CMC orientation 1 S_{sd12} (DCMR), logarithmic magnitude in dB / CMC orientation 2 S_{ds21} (CDMR), logarithmic magnitude in dB / CMC orientation 1 S_{ds12} (CDMR), logarithmic magnitude in dB / CMC orientation 2 For S_{sd12} and S_{ds12} measurement the terminal orientation of the CMC is rotated by 180° on the test board.
VNA measurement circuit:	port definitions: mixed mode logic port 1: physical port 1a and port 1b mixed mode logic port 2: physical port 2a and port 2b pin 1 of CMC is placed on logic port 1. 4-port measurements / S_{dd11}, S_{dd22}, S_{dd21} and S_{cc21} mixed mode: 50 Ω input impedance at each measurement port 

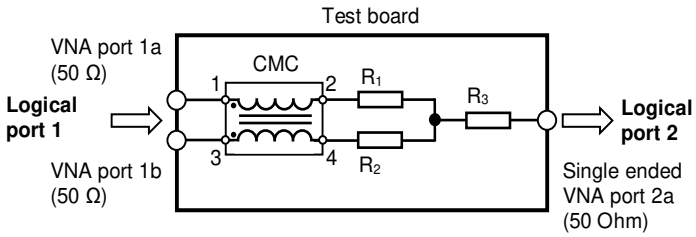
VNA measurement circuit (continue):	3-port measurements / S_{sd21}, S_{ds21}, S_{ds12} and S_{ds12} single ended: differential mode input (logical port 1): 50 Ω impedance each common mode output (logical port 2): single ended network with 200 Ω impedance $R = (R_1 \,||\, R_2) + R_3 + R_{\text{VNA port 2a}}$  R = 49,9 Ω for R_1 and R_2 R = 124 Ω for R_3 The accuracy of resistor values should be ≤ 1 %. The difference between matching resistors should be ≤ 0.1 %.

Table 5-6: Test procedure and parameters for S-parameter measurements at CMC

The measurements should be performed and documented according to the scheme given in Table 5-7.

Test	S-parameter	Reference impedance differential mode [a]	Reference impedance common mode [a]	Sample
S1a	S_{dd11} (RL)	100 Ohm	25 Ohm	10 samples each
S1b [b]	S_{dd11} (RL)	50 Ohm	12.5 Ohm	
S2a	S_{dd22} (RL)	100 Ohm	25 Ohm	
S2b [b]	S_{dd22} (RL)	50 Ohm	12.5 Ohm	
S3	S_{dd21} (IL)	100 Ohm	25 Ohm	
S4	S_{cc21} (CMR)	100 Ohm	25 Ohm	
S7	S_{sd21} (DCMR)	100 Ohm	25 Ohm	
S8	S_{sd12} (DCMR)	100 Ohm	25 Ohm	
S9	S_{ds21} (CDMR)	100 Ohm	25 Ohm	
S10	S_{ds12} (CDMR)	100 Ohm	25 Ohm	

[a] for S1 to S4: definition valid for physical port 1a, 1b, 2a and 2b
for S7 to S10: definition valid for physical port 1a, 1b, physical port 2a is defined to 50 Ohm for single ended

[b] renormalization of measured results for 100 Ohm differential mode and 25 Ohm common mode impedance condition into 50 Ohm differential mode and 12.5 Ohm common mode impedance condition

Table 5-7: Required S-parameter measurements for CMC

For each test case, the results for all 10 samples should be documented as diagram in the CMC characterization report. Recommended limits for evaluation are given in Annex A.2.

5.4 ESD damage

5.4.1 Test setup

The test setup given in Figure 5-8 is used for testing the ESD robustness of CMC.

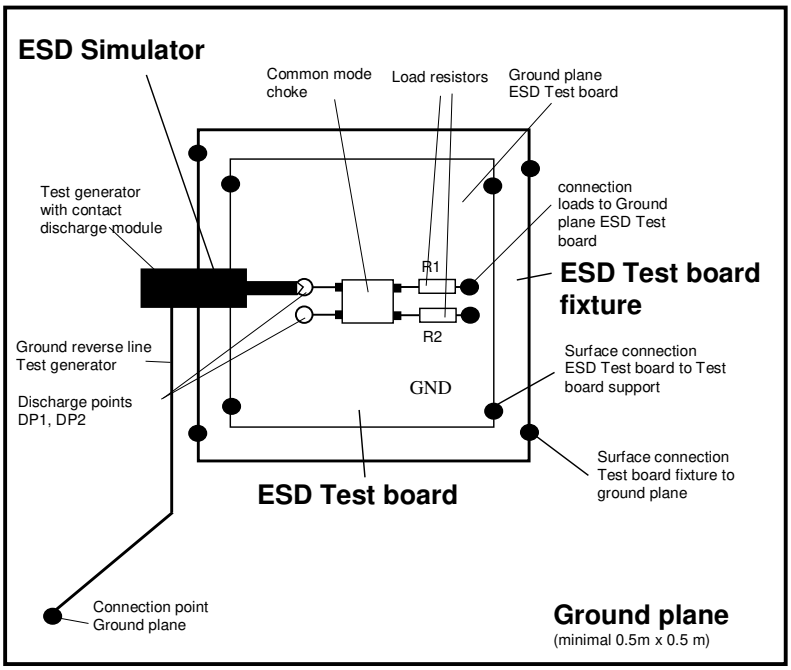


Figure 5-8: Test setup for ESD damage tests at CMC

The test equipment definitions are the following:

- ESD generator (according to ISO 10605, discharge storage capacitor C = 150 pF and discharge resistor *R* = 330 Ω);
- ESD test board;
- ground plane;
- test board fixture.

The ground plane with a minimum size of 0.5 m × 0.5 m is connected to protective earth of the electrical grounding system of the test laboratory. The ESD generator ground return cable is directly connected to this ground plane.

The metallic test fixture positions the ESD test board and directly connects the ESD test board ground plane to the reference ground plane. The ground connection of the test fixture is connected to ground plane with low impedance and low inductance. This surface connection should have a contact area of at least 4 cm^2. Copper tapes can be used in addition.

For testing the tip of the ESD generator is directly contacted with one of the discharge points DP1 and DP2 of the ESD test board. For this purpose, the discharge points are implemented as rounded vias in the layout of the ESD test board and are directly connected by a trace 15 (±5) mm with the respective pin of the CMC.

To achieve a high grade of accuracy of required S-parameter measurements for damage evaluation, it is recommended to use the same test board for S-parameter and ESD tests without re-soldering the DUT. For check of damage evaluation criteria (S-parameter), the reference points for calibration are the input of RF connector (SMA) at the test board.

An example for ESD test board is given in Figure 5-9.

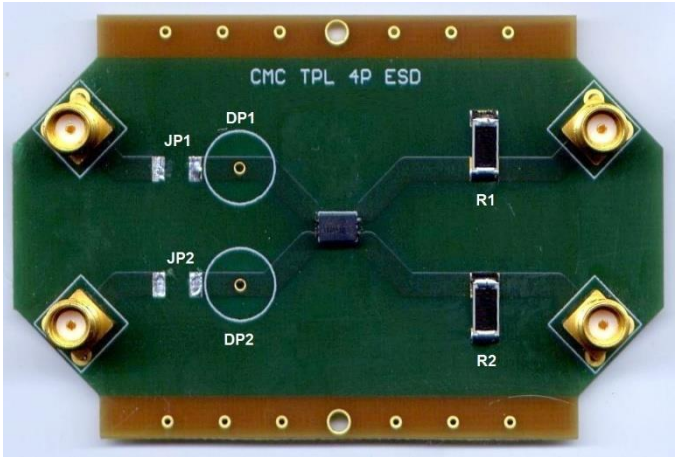


Figure 5-9: Example of ESD test board for CMC, top layer

NOTE While using the ESD test board example given in Figure 5-9 the serial jumpers JP1 and JP2 are left open and the resistors R1 and R2 are populated for ESD tests itself. For S-parameter measurement, the jumpers JP1 and JP2 are closed and the resistors R1 and R2 are not populated. The purpose of using jumpers JP1 and JP2 is to avoid parasitic discharge (ESD spark over event) from discharge points DP1 and DP2 to the ground plane of the ESD test board that can occur at the RF connector (SMA) because of the small dimensions at the connector contacts.

Other test board implementations without using jumpers to disconnect the discharge points from the RF connector terminal can be used as well (e.g. de-soldering the RF connector from ESD test board for ESD test itself). However, in all cases, the avoidance of parasitic discharge from discharge points DP1 and DP2 to the ground plane needs to be checked before testing for unpopulated CMC with a maximum ESD test voltage of +/- 8 kV.

5.4.2 Test procedure and parameters

The required tests and procedure are defined in Table 5-8 and should be done on one sample.

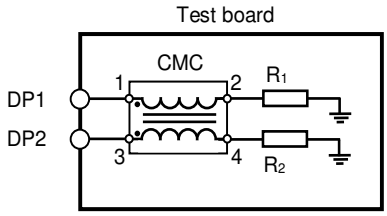
Item	Parameter
Coupling of ESD:	Direct discharge method according to ISO 10605 (discharge storage capacitor C = 150 pF and discharge resistor R = 330 Ω)
Test circuit:	 R = 2 Ω for R_1 and R_2 All resistors have SMD design 1206 or larger with a maximum tolerance of 2 %. The exact type and manufacturer of the used resistors should be documented in the test report.
ESD test voltage:	± 8 kV
Number of discharges:	10 per polarity
Time between discharges:	5 s
Damage evaluation criteria:	– degrade by more than 0,1 dB from the initial value after performing the tests for S-parameter S_{dd21} for frequencies $f \leq 200$ MHz – degrade by more than 1 dB from the initial value after performing the tests for S-parameter S_{dd11}, S_{dd22} and S_{cd21} for frequencies $f \leq 200$ MHz The S-parameter measurements should be done according to 5.3. Frequency ranges or frequency spots with a level at noise floor or below the related limits of 5.3 should not be weighted for applying the damage evaluation criteria. For simplification of measurement for check of mode conversion loss the S-parameter S_{cd21} is used instead of S_{sd21}. The setup for S-parameter S_{cd21} is same as used for the other required S-parameter. Because of different test circuitry for S-parameter S_{cd21} and S_{sd21} the related limit for S-parameter S_{cd21} is corrected by + 10 dB.
Test procedure:	1. *S*-parameter reference measurement before ESD test 2. apply ESD discharges at DP1 (± 8 kV, 10 per polarity, 5 s delay) 3. apply ESD discharges at DP2 (± 8 kV, 10 per polarity, 5 s delay) 4. demagnetization of CMC (if needed) 5. evaluate damage using damage evaluation criteria If a damage occurs at ± 8 kV the test should be repeated with a reduced ESD test voltage to find out the immunity threshold of the DUT. Nevertheless, applying an ESD test voltage of ± 8 kV without damage for DUT is required to pass the test.

Table 5-8: Test parameters for ESD damage tests at CMC

The measurements should be performed and documented according to the scheme given in Table 5-9.

Test	Discharge point	Comment	Sample
E1	DP1	Line 1	1 sample
E2	DP2	Line 2	

Table 5-9: Required ESD tests for damage for CMC

The CMC should withstand the ESD discharge without damage according to the damage evaluation criteria. Recommended limits are given in Annex A.3.

5.5 Saturation test at RF disturbances

5.5.1 Test setup

The test setup for measuring the saturation effect at RF immunity tests consists of a 4-port VNA or 2-port VNA in combination with a RF amplifier, RF attenuator and a special test board. The test setup is given in Figure 5-10.

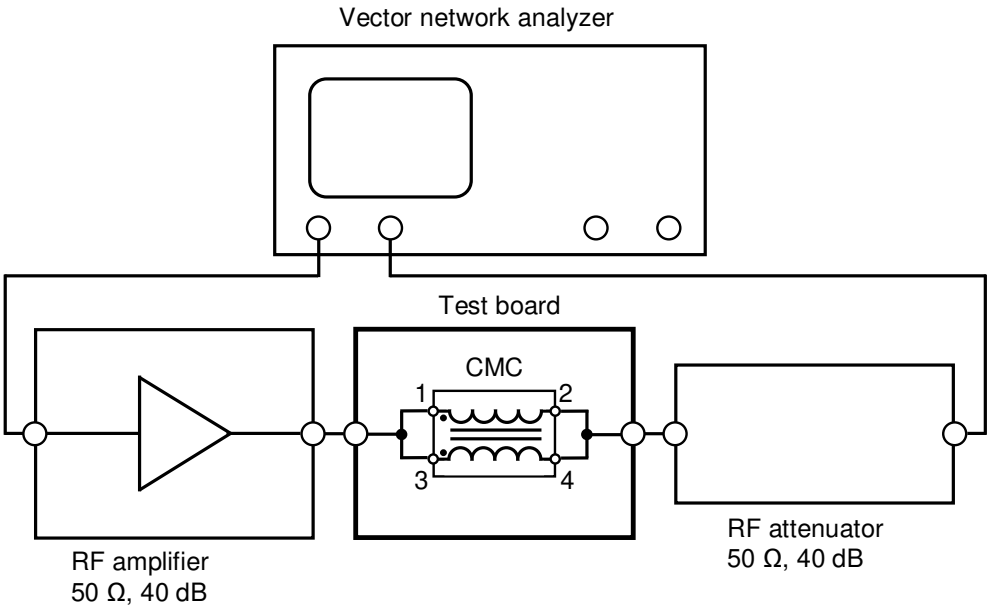


Figure 5-10: Test setup for RF saturation measurements at CMC

The test equipment definitions are the following:

- 4-port or 2-port vector network analyzer;
- RF amplifier (impedance 50 Ω, gain app. 40 dB, PCW ≥ 10 W);
- RF attenuator (impedance 50 Ω, attenuation 40 dB), and
- test board RF saturation / S-parameter (2-port).

An example for RF saturation / S-parameter test board is given in Figure 5-11.

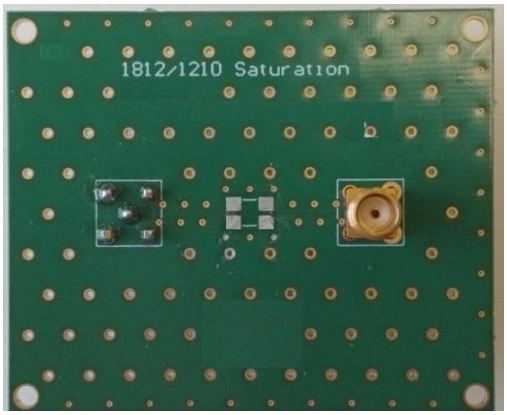


Figure 5-11: Example of RF saturation / S-parameter test board for CMC, top layer

5.5.2 Test procedure and parameters

The required test procedure and parameters are defined in Table 5-10.

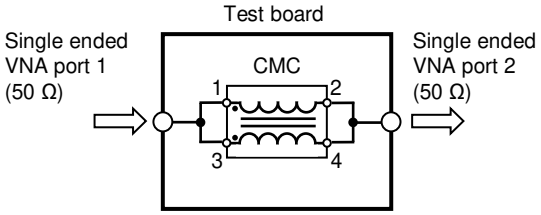
Item	Parameter
Frequency range:	1 MHz to 1 GHz
S-parameter power level:	S_{21} (CMR), logarithmic magnitude in dB
Measurement test circuit:	port definitions: logic port 1: physical port 1 logic port 2: physical port 2 line 1 of CMC is placed on transceiver side (logic port 1) S_{21} measurement: 50 Ω input impedance at each measurement port 
Test power level:	forward power: 24 dBm, 30 dBm, 33 dBm, 36 dBm These test levels are obtained from test level measurement into a 50 Ohm load.
Dwell time per power level:	≥ 60 s
Evaluation of saturation effect:	maximum deviation of 1 dB from the CMR reference value at 24 dBm for power level 30 dBm maximum deviation of 1 dB from the CMR reference value at 24 dBm for power level 33 dBm above 5 MHz maximum deviation of 1 dB from the CMR reference value at 24 dBm for power level 36 dBm above 7 MHz
Test procedure:	1. define the test equipment settings for test power levels 24 dBm, 30 dBm, 33 dBm and 36 dBm with replacement of DUT by short connections on the test board 2. test with power level 24 dBm for setting the reference value 3. test with power level 30 dBm and evaluation 4. test with power level 33 dBm and evaluation 5. test with power level 36 dBm and evaluation

Table 5-10: Test procedure and parameters for RF saturation tests at CMC

The tests should be performed at one sample and documented according to the scheme given in Table 5-11.

Test	S-parameter	Sample
RFS1	S_{21} (CMR)	1 sample

Table 5-11: Required RF saturation tests for CMC

The CMC should withstand the RF power saturation test according to the evaluation criteria. Recommended limits are given in Annex A.4.

5.6 Saturation test at ESD

5.6.1 Test setup

The test setup for measuring the saturation effect at ESD tests consists of a TLP test system, digital storage oscilloscope and a special test board. The test setup is given in Figure 5-12.

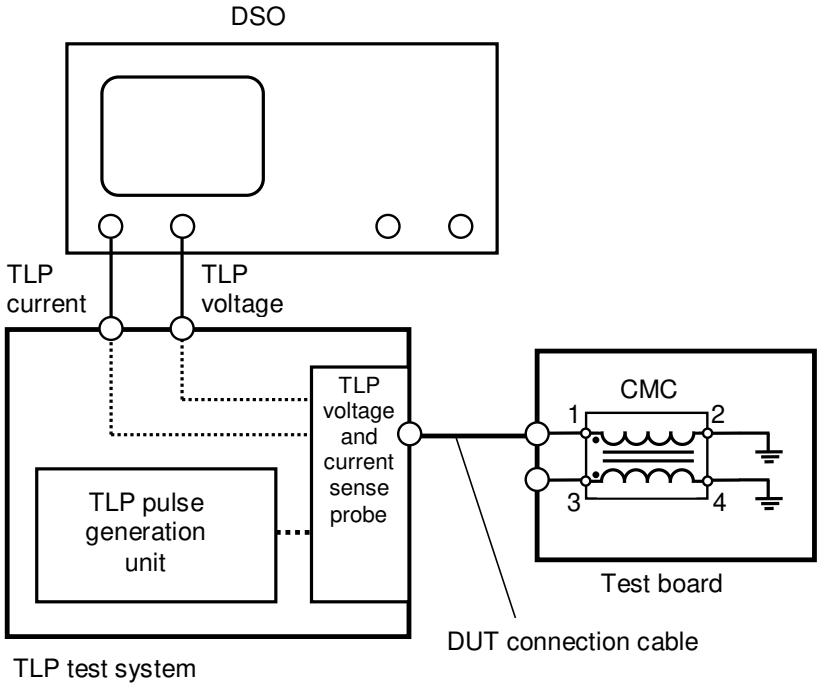


Figure 5-12: Test setup for ESD saturation measurements at CMC

The test equipment definitions are the following:

- TLP test system according to IEC 62615, including TLP generator, current probe and voltage probe;
- DUT connection cable with length ≤ 0.1 m between the test board and the TLP voltage / current sense probes;
- digital storage oscilloscope (DSO, 50 Ω input impedance, minimum 4 GHz analog input bandwidth);
- test board CMC ESD saturation.

NOTE It is recommended to use a DUT connection cable with a maximum length of 0.1 m for lowering the parasitic impact of signal propagation delay to the definition of the reference time for the TLP measuring window t_0 that can cause uncertainty in measuring results. If a DUT connection cable is used with more than 0.1 m length, the signal propagation delay on this cable needs to be considered for definition of the starting time for the TLP measuring window t_0. For this purpose a procedure is given in Annex B.

The TLP test system (including software for post procession, if available) shall be configured according to the definitions of TLP test system manufacturer. To ensure a correct implementation of all connection cables inside the TLP test system and to the DSO as well as the voltage and current probes, the complete system needs to be verified using calibration fixtures according to the definitions of IEC 62615 and the TLP test system manufacturer.

An example for CMC ESD saturation test board is given in Figure 5-13.

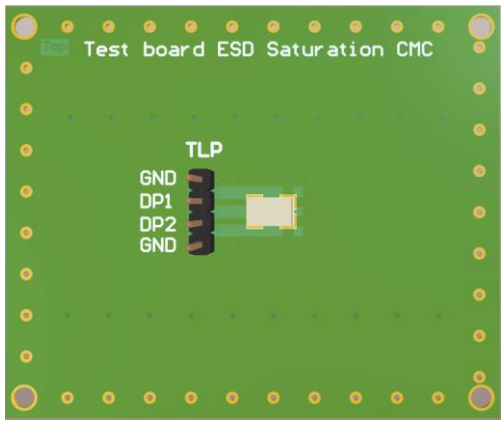


Figure 5-13: Example of ESD saturation test board for CMC, top layer

5.6.2 Test procedure and parameters

The required test procedure and parameters are defined in Table 5-12.

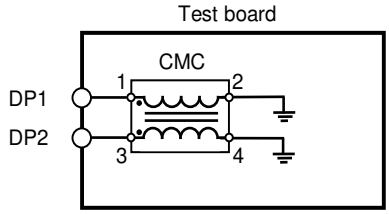
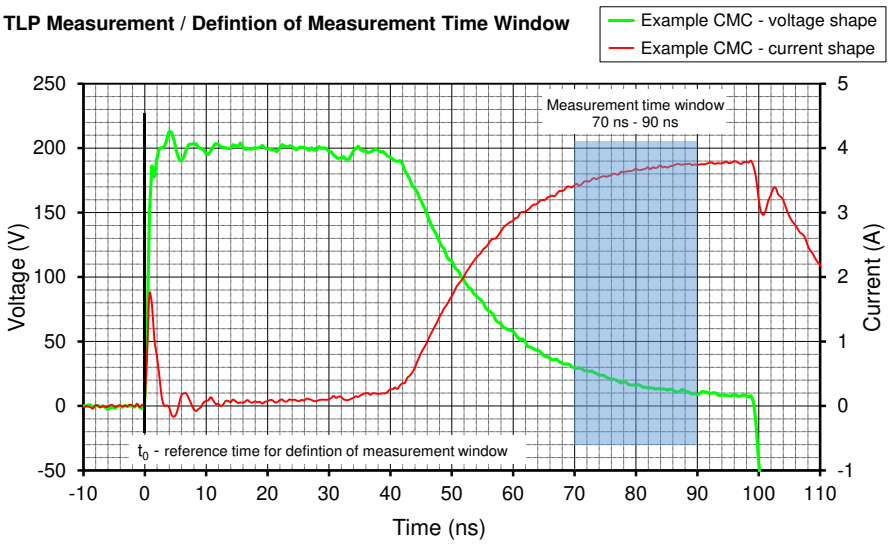
Item	Parameter
Coupling of ESD:	TLP test system according to IEC 62615
Test circuit:	
TLP test parameter:	TLP pulse width: 100 ns TLP pulse rise time: ≤ 1 ns Measurement time window: 70 ns to 90 ns referenced to TLP pulse starting time, defined as reference time t_0 Maximum test voltage: 500 V Test voltage step size: ≤ 2 V Maximum test current: 15 A Definition for TLP pulse reference time t_0 
Evaluation of saturation effect:	CMC ESD saturation break down voltage V_{ESD_br} derived from measured TLP I/V characteristic and limits according to Annex A.5.

Table 5-12: Test procedure and parameters for ESD saturation tests at CMC

The tests should be performed and documented according to the scheme given in Table 5-13.

Test	Discharge point	Comment	Parameter	Sample
ES1	DP1	Line 1	CMC ESD saturation break down voltage	1 sample
ES2	DP2	Line 2		

Table 5-13: Required ESD saturation tests for CMC

For each test case, the TLP I/V characteristic should be recorded and documented in a diagram in the test report. The derived CMC ESD saturation break down voltage should be below the recommended limits given in Annex A.5.

Annex A

Recommended limits for tests

A.1 Parasitic capacitance

Based on measurement result of parasitic capacitance C_{para_max} the CMC shall be classified using the definition of Table A-1.

Class	C_{para_max}
I	13 pF < C_{para_max} ≤ 17 pF
II	10 pF < C_{para_max} ≤ 13 pF
III	7 pF < C_{para_max} ≤ 10 pF
IV	C_{para_max} ≤ 7 pF

Table A-1: Parasitic capacitance classes for CMC

An example of measurement results for typical CMCs using the VNA measurement method is shown in Figure A-1.

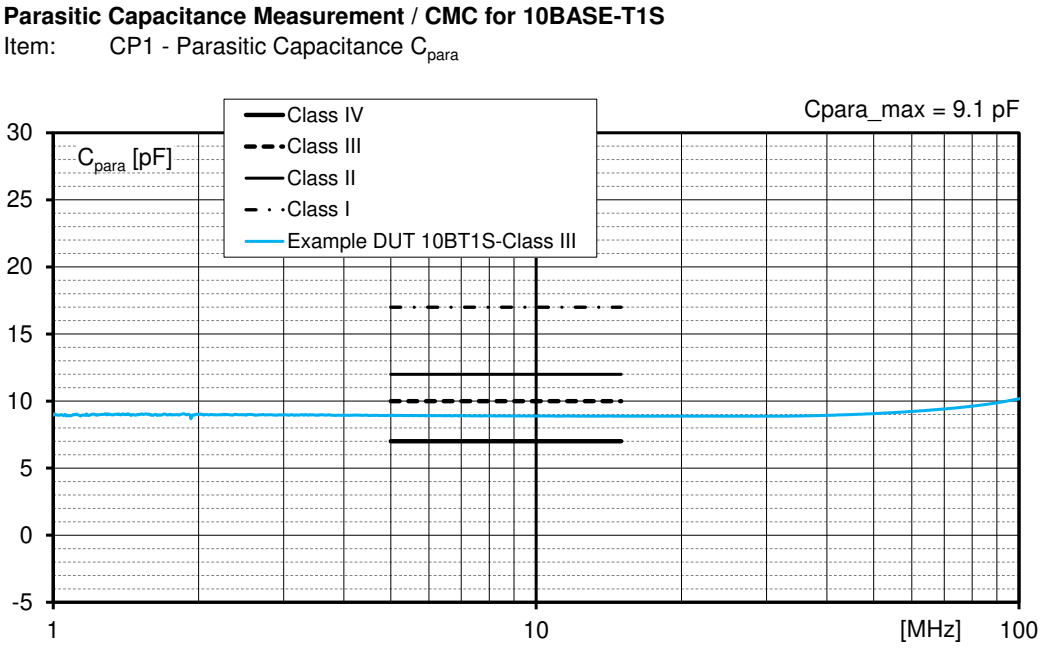


Figure A-1: Example of parasitic capacitance measurement results for CMC

A.2 S-parameter measurement mixed mode

For evaluation of mixed mode S-Parameters the limits given in Figure A-2 to Figure A-5 are recommended. The required limit class depend on the application conditions and will be defined by the customer.

S - Parameter / CMC for Ethernet 10BASE-T1S
Item: Return Loss (RL) / S_{dd11}, S_{dd22}

[MHz]	Limit Class - 100 Ohm DM reference impedance	[MHz]	Limit Class - 50 Ohm DM reference impedance
0,3	-27	0,3	-20
10	-27	6	-20
40	-21	40	-9

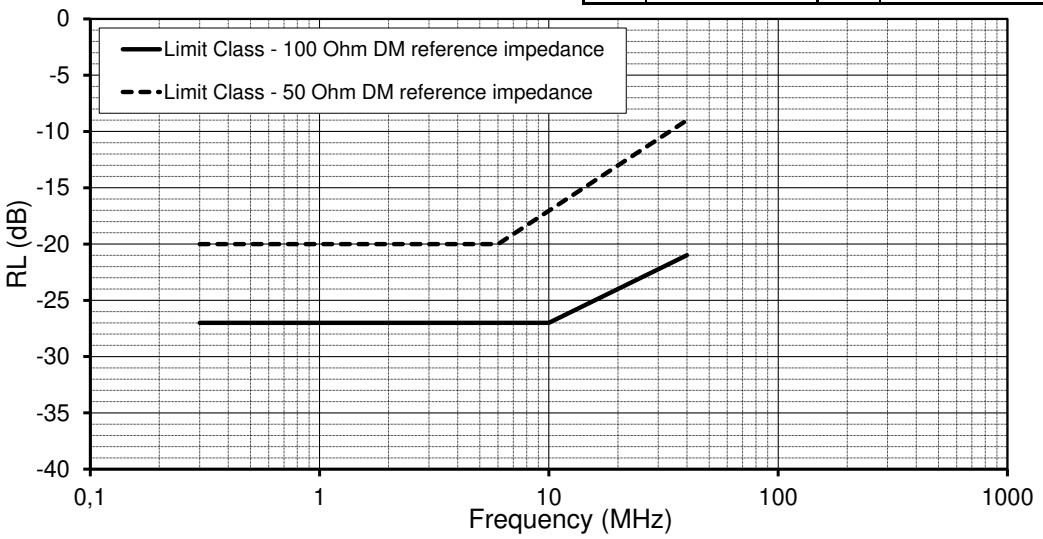


Figure A-2: Recommended characteristics for Sdd11, Sdd22 (RL) for CMC

S - Parameter / CMC for Ethernet 10BASE-T1S
Item: Insertion Loss (IL) / S_{dd21}

[MHz]	Limit Class I
0,3	-0,5
10	-0,5
33	-0,7
40	-0,8

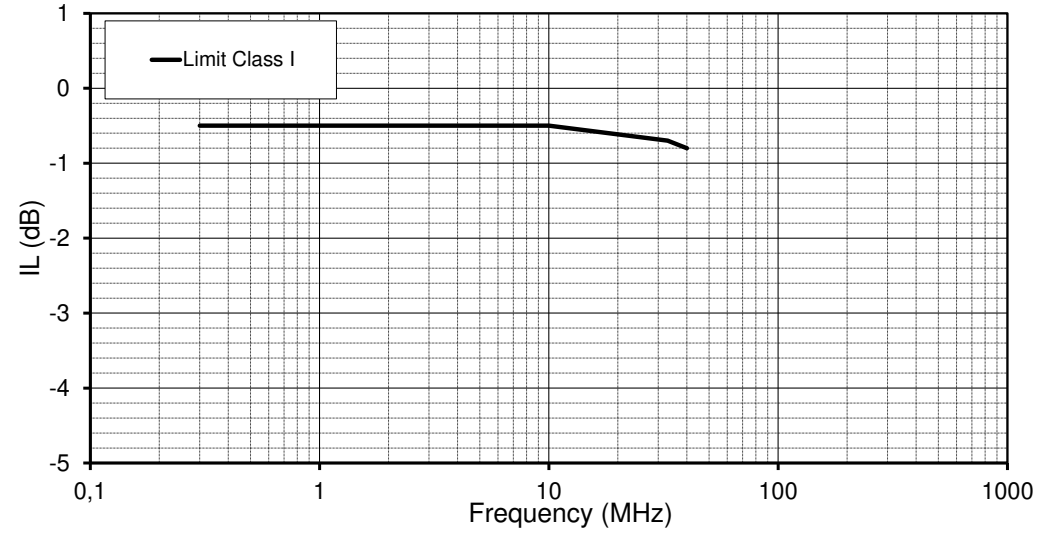


Figure A-3: Recommended characteristics for *S*dd21 (IL) for CMC

S - Parameter / CMC for Ethernet 10BASE-T1S
Item: Common Mode Rejection (CMR) / S_{cc21}

[MHz]	Limit Class III	[MHz]	Limit Class II	[MHz]	Limit Class I
0,3	-15	0,3	-12	0,3	-9
10	-45	10	-42	10	-39
80	-45	112	-42	160	-39
200	-37	200	-37	200	-37
300	-33,5	300	-33,5	300	-33,5

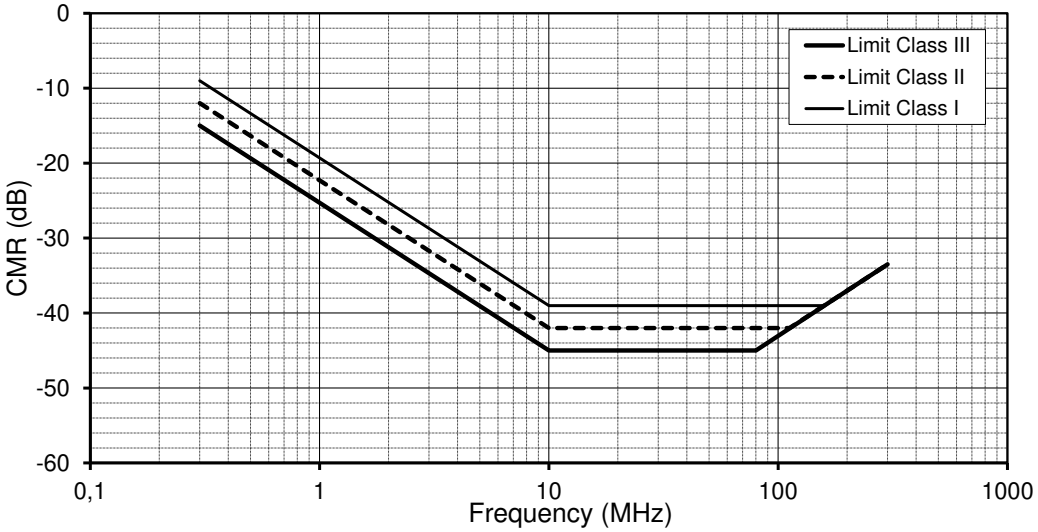


Figure A-4: Recommended characteristics for *S*cc21 (CMR) for CMC

S - Parameter / CMC for Ethernet 10BASE-T1S
Item: Common to Differential Mode conversion Ratio (CDMR) / S_{ds21},S_{ds12}
Differential to Common Mode conversion Ratio (DCMR) / S_{sd21},S_{sd12}

[MHz]	Limit Class III	[MHz]	Limit Class II	[MHz]	Limit Class I
0,3	-70	0,3	-64	0,3	-58
10	-70	10	-64	10	-58
100	-50	100	-44	100	-38
300	-40	300	-34	300	-28

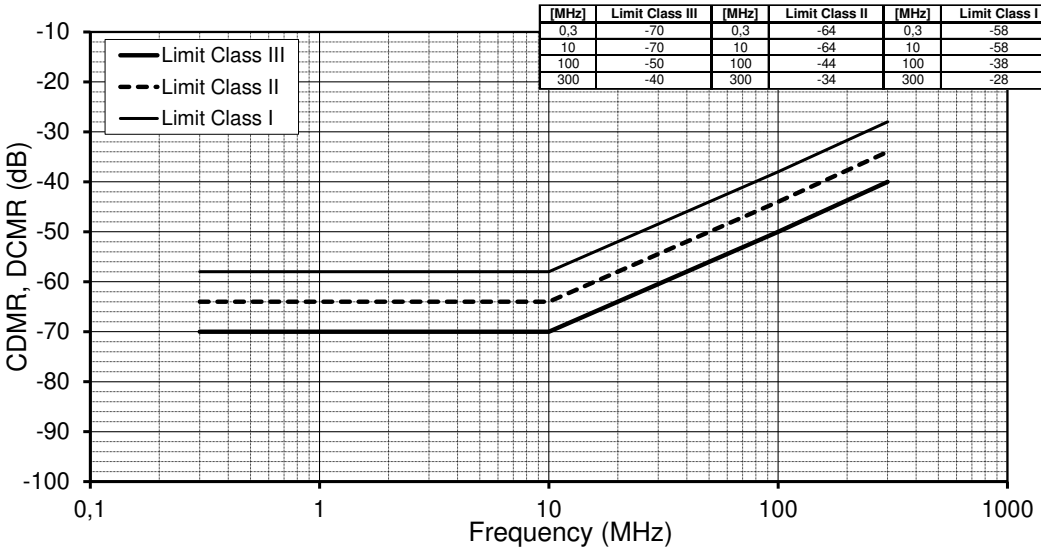


Figure A-5: Recommended characteristics for Ssd21, Ssd12 (DCMR) and Sds21, Sds12 (CDMR) for CMC

A.3 ESD damage

It is recommended that the CMC must withstand the ESD discharge with discharge voltage amplitude of +/- 8 kV without damage.

A.4 Saturation test at RF disturbances

It is recommended that the CMC must withstand the RF power saturation test according to the evaluation criteria up to power amplitude of 36 dBm.

A.5 Saturation test at ESD

Based on measurement result of TLP I/V characteristic the CMC shall be classified using the definition of Table A-2 and Figure A-14.

Class	V_{ESD_br}
I	50 V to 125 V
II	≥ 125 V

Table A-2: ESD saturation break down voltage classes for CMC

An example of measurement results for typical CMCs is shown in Figure A-14.

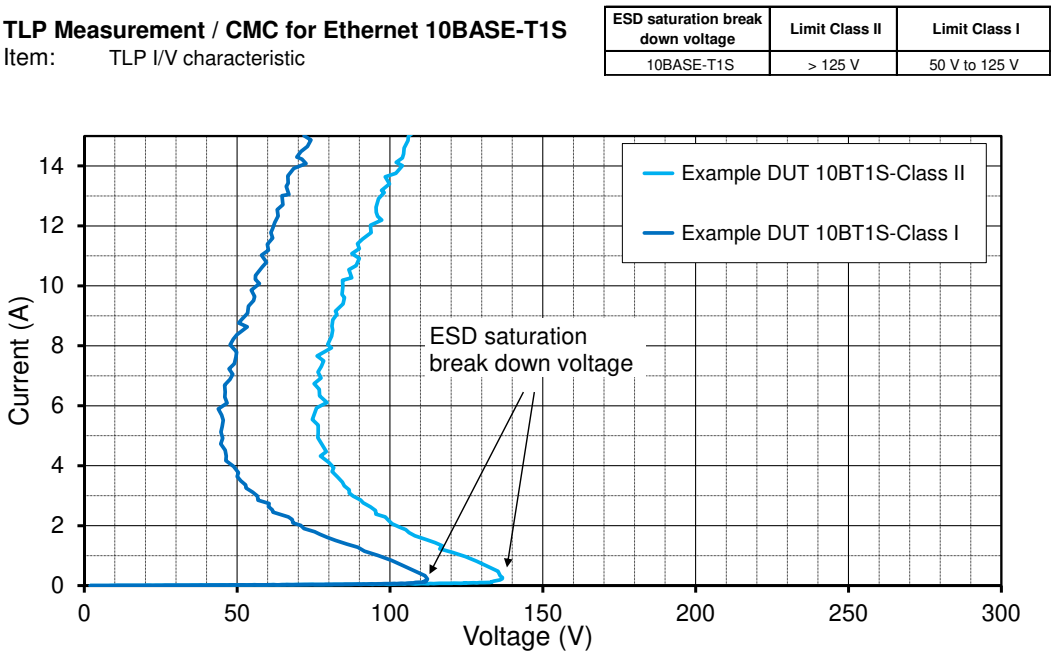


Figure A-14: Example of ESD saturation tests results for CMC

Annex B

Correction methods for usage of DUT connection cable longer than 0.1 m for TPL measurements

B.1 Reference time correction procedure

If a long DUT connection cable is used, the reflected wave observed on the TLP voltage and current sense probes - connected with the oscilloscope - will be delayed from the pulse output timing as shown in Figure B-1, resulting in current and voltage shapes being affected by the cable propagation delay. The time when the pulse arrives at the DUT is defined as the reference time t_0, instead of the TLP pulse starting time, for the measurement time window to compensate the signal propagation delay on the connection cable.

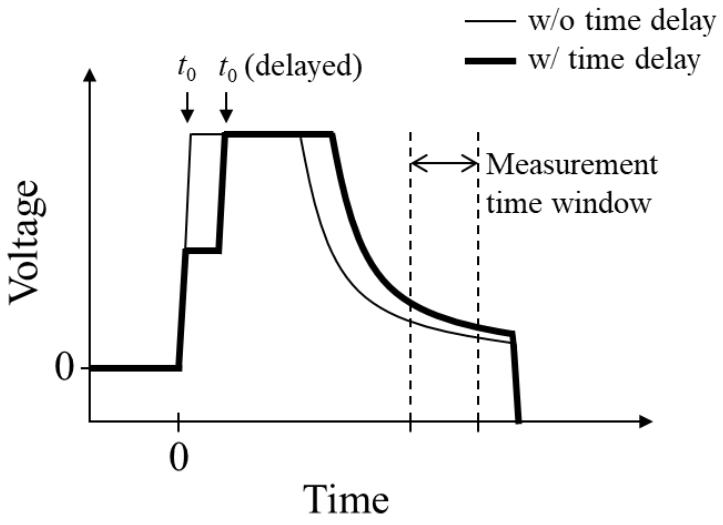


Figure B-1: Parasitic impact of DUT connection cable propagation delay

The reference time t_0 should be corrected in one of the following methods.

a) Prepare a time delay in a TLP test system in advance and use it for correction. The adjustments derived from this way should be applied to the data within the operating system software or during post-processing using spreadsheet or other data analysis software.
b) During the error correction open circuit methodology in 6.2.3 of the IEC 62615, determine t_0 from the timing when the rising edge of the voltage reflected wave becomes 10 % of its amplitude as shown in Figure B-2. The adjustment derived from this way should be applied to the data within the operating system software or during post-processing using spreadsheet or other data analysis software.
c) During the pulse waveform measurement, trigger at the timing when the rising edge of the voltage reflection wave becomes 10 % of its amplitude and use the trigger timing as t_0 as shown in Figure B-3.

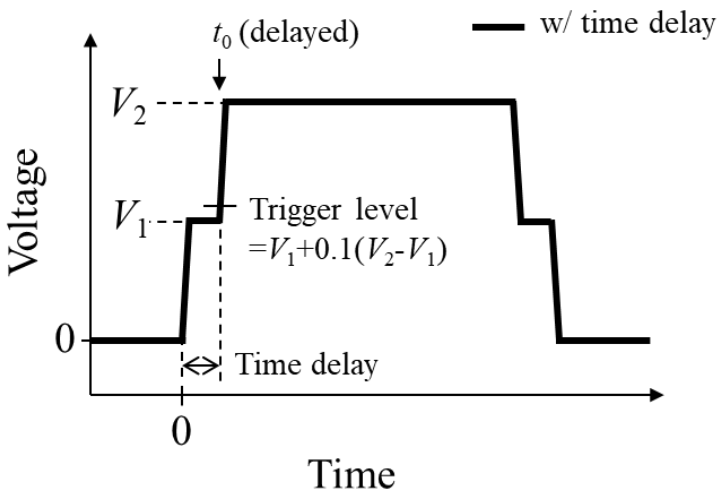


Figure B-2: Correction method b) for reference time t_0

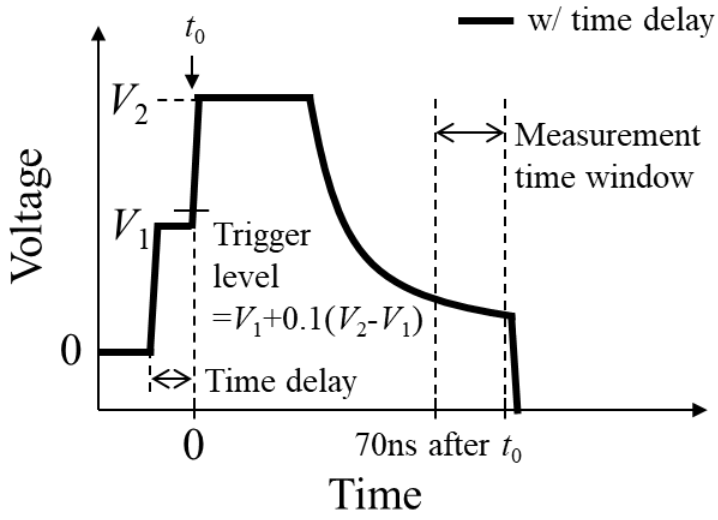


Figure B-3: Correction method c) for reference time t_0

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