IEEE 10BASE-T1S EMC Test Specification for ESD Suppression Devices

Version 1.0

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This EMC measurement specification shall be used as a standardized common scale for EMC evaluation of ESD suppression devices for 10BASE-T1S applications.

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Introduction

The IEEE 802.3cg standard defines a 10 Mbit/s Ethernet communication over an unshielded single pair of conductors and separate the two systems 10BASE-T1S and 10BASE-T1L. The 10BASE-T1S implementation covers a half duplex communication using a CSMA/CD for point to point channel and the optional functionalities full duplex communication for a point to point channel and a half duplex communication for a so called mixing segment (or multidrop mode) with at least 8 nodes and 25 m length of bus lines. In any case, the bus cable is terminated with the line impedance of 100 Ω at both ends of the channel. As an optional feature to enable a deterministic access time for each bus node in a mixing segment the new access method PLCA is overlaid to the CSMA/CD system. Due to the high communication rate of 10BASE-T1 and the intended use of unshielded twisted pair cable, a high risk of EMC problems is expected. For this reason, an EMC optimization of all components of the Ethernet physical layer is required.

An ESD suppression device can be used to increase the ESD robustness of 10BASE-T1S Ethernet transceivers according to [1] and can have a significant effect on EMC test results in communication networks. In principle there are two possible positions of ESD suppression device implementation within an Ethernet interface: between the transceiver and the CMC or between the MDI connector and the common mode termination network as described in Figure 1.

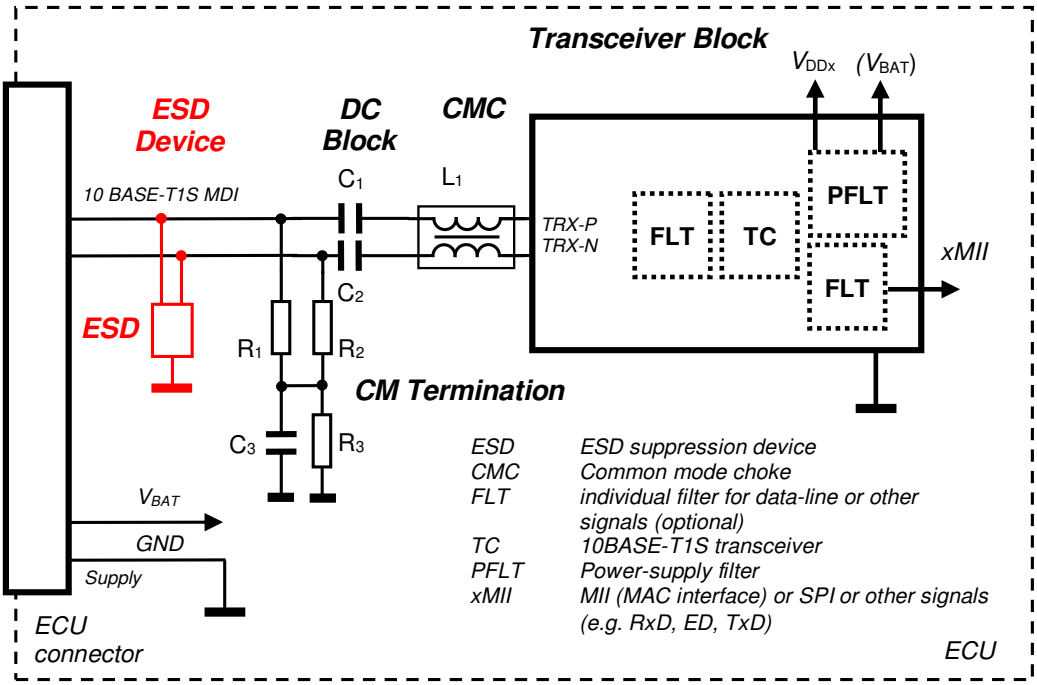


Figure 1: Arrangement of ESD suppression device within the 10BASE-T1S MDI interface

This EMC measurement specification is focused on evaluation of the ESD suppression device characteristics related to high frequency and functional aspects as well as ESD.

Abbreviation/Symbols

BIN	*Bus Interface Network*
CMC	*Common Mode Choke*
CMR	*Common Mode Rejection*
CMT	*Common Mode Termination*
DCMR	*Differential to Common Mode Rejection, common mode single ended measured*
ESD	*Electro Static Discharge*
IL	*Insertion Loss*
MDI	*Medium Dependent Interface*
RF	*Radio Frequency*
RL	*Return Loss*
S-Parameter	*Scattering Parameter*
VNA	*Vector Network Analyzer*
TLP	*Transmission Line Pulse*

1 Scope

This document specifies test and measurement methods for characterization of ESD suppression device intended to use for the position between MDI connector and common mode termination network within the 10BASE-T1S interface according to Figure 1. It contains definitions for test methods, test conditions, performance criteria, test procedures, test setups, test boards and recommended limits and covers

- evaluation of datasheet parameters;
- parasitic capacitance;
- S-Parameter measurement mixed mode;
- ESD damage test;
- test of unwanted clamping effect at RF immunity tests;
- impact to ESD discharge current in a defined 10BASE-T1S network.

It shall be used for evaluation of ESD suppression devices or passive components with internal ESD suppression unit (e.g. combination of ESD suppression and common mode termination circuit).

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

[1] IEEE P802.3cg™: Physical Layer Specifications and Management Parameters for 10 Mb/s Operation and Associated Power Delivery over a Single Balanced Pair of Conductors

[2] IEC 62615, Electrostatic discharge sensitivity testing – Transmission line pulse (TLP) – Component level

[3] ISO 10605, Road vehicles – Test methods for electrical disturbances from electrostatic discharge

[4] OPEN ALLIANCE, IEEE 10BASE-T1S EMC Test Specification for Common mode chokes

[5] OPEN ALLIANCE, IEEE 10BASE-T1S EMC Test Specification for Transceivers

3 Terms and Definitions

For the purposes of this document, the terms and definitions given in 2 and following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- ISO Online browsing platform: available at https://www.iso.org/obp;
- IEC Electropedia: available at http://www.electropedia.org.

4 General

The intention of this document is to evaluate the EMC performance of ESD suppression devices intended to use for 10BASE-T1S Ethernet interfaces. The final judgment of the tested device is left to the customer.

5 Test and measurement

5.1 General definitions

All tests are performed for standard room temperature (23 °C +/- 3 K).

A printed circuit board with RF board-to-coax connectors should be used for RF parameter related tests. To ensure reliable RF parameters, a test board with at least two layers with enlarged GND reference plane is required. The traces on the test board should be designed as 50 (± 5) Ω single ended transmission lines with a length as short as possible.

The test board design and the method of connecting the ESD suppression device with the test board shall provide high accuracy and reproducible test results.

All test are defined at a two-line ESD suppression device used in a 10BASE-T1S MDI. If the ESD suppression device has more than two lines, the test setup should be adapted accordingly. The test of single-line ESD suppression devices shall be performed with a combination of two devices of the same type.

Prior to performing any RF and ESD tests, the S-Parameter measurements shall be performed on a minimum of 10 samples.

The following parameters for ESD suppression device shall be ensured and documented in the datasheet.

Parameter	Target Value
Working direction	bi-directional
Operation voltage (V_{DCmax})	≥ 24 V
ESD trigger voltage	≥ 100 V
ESD robustness	+/- 15kV contact discharge for unpowered device using discharge module according to ISO 10605 (discharge storage capacitor C = 150 pF and discharge resistor R = 330 Ω)
Minimum number of discharges	> 1000
TLP characteristic according to [2]	I/V characteristics

Table 5-1: Target values for ESD suppression device

The given target values for operation voltage and ESD trigger voltage are related to the position of ESD protection device within the BIN as given in Figure 1.

5.2 Measurement of parasitic capacitance

In general, the parasitic capacitance of ESD suppression device is measured between the two pins that connect the MDI lines of a 10BASE-T1S interface while the GND pin of the device is connected to common GND. In consequence, the resulting measured parasitic capacitance for single-line ESD suppression devices is half of the single device value itself.

The parasitic capacitance should be measured ether with VNA measurement method or with LCR meter / impedance analyzer measurement method.

5.2.1 VNA measurement method

5.2.1.1 Test setup

The test setup for measuring the parasitic capacitance consists of a VNA in combination with a special test board (adapter test board). The test board is included into the test setup during VNA calibration. The reference points for calibration are defined to the pads of the ESD suppression device at the test board.

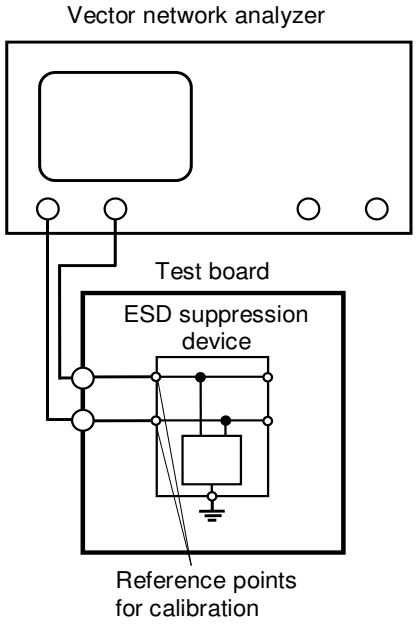


Figure 5-1: Test setup for parasitic capacitance measurement for VNA method

The test equipment definitions are the following:

- vector network analyzer;
- test board parasitic capacitance.

The connecting traces of the test board from RF connectors to the ESD suppression device should be routed symmetrically at 45° to decrease parasitic inductive coupling. An example for test board is given in Figure 5-2.

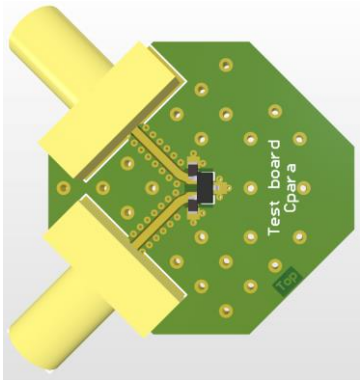
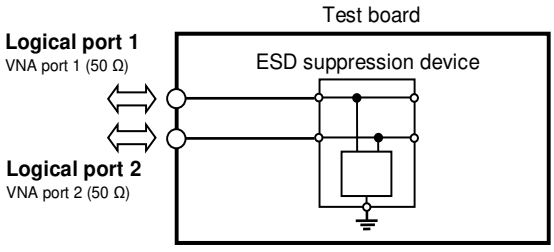


Figure 5-2: Example of test board parasitic capacitance measurement for VNA method, top layer

The test board symmetry and calibration accuracy should be validated with measurement of an open-circuit (without DUT). The remaining open-circuit capacitance should not exceed 50 fF.

5.2.1.2 Test procedure and parameters

The test procedure and parameters are defined in Table 5-7.

Item	Parameter
Frequency range:	1 MHz to 100 MHz
S-parameter per single path:	S_{11}, Re + j Im / ESD suppression device line 1 S_{22}, Re + j Im / ESD suppression device line 2 S_{21}, Re + j Im / ESD suppression device line 1 to line 2 S_{12}, Re + j Im / ESD suppression device line 2 to line 1
VNA measurement circuit:	port definitions: logic port 1: physical port 1 / ESD suppression device line 1 logic port 2: physical port 2 / ESD suppression device line 2 

Calculation method:	1. Calculate Y-Parameters from S-Parameters: $[S] = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \Longrightarrow [Y] = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}$ Note: All calculations should be performed using raw or linearly interpolated data, to avoid inaccuracy introduced by e.g. spline interpolation or rational fitting. 2. Calculate the mean transfer Y-Parameter Y_T: $Y_T = \frac{(Y_{21} + Y_{12})}{2} = \frac{S_{12} + S_{21}}{50 \cdot (1 + S_{11} - S_{12} \cdot S_{21} + S_{22} + S_{11} \cdot S_{22})}$ 3. Calculate the parasitic capacitance C_{para}(f) while extracting the negative imaginary part of Y_T: $C_{para}(f) \approx \frac{Im(-Y_T)}{2\pi f}$ 4. The resulting value C_{para_max} is the maximum value of C_{para} (f) in the frequency range from f = 5 MHz to f = 15 MHz.

Table 5-2: Test procedure and parameters for parasitic capacitance measurements at ESD suppression device using VNA method

The tests should be performed at 10 samples and documented in a diagram with C_{para} (f) and C_{para_max} according to the scheme given in Table 5-3. Recommended limits for evaluation are given in Annex A.1.

Test	Item	Sample
CP1	C_{para_max}	10 samples

Table 5-3: Required parasitic capacitance measurements for ESD suppression device

5.2.2 LCR meter or impedance analyzer measurement method

5.2.2.1 Test setup

The test setup for measuring the parasitic capacitance consists of a LCR meter or an impedance analyzer in combination with a special test fixture extension, direct mounted to the measuring device. The reference points for calibration are defined to electrode plates at the test fixture extension the contact the ESD suppression device. As shown in Figure 5-3 two-line ESD protection devices and single-line ESD protection devices can be measured in a different way.

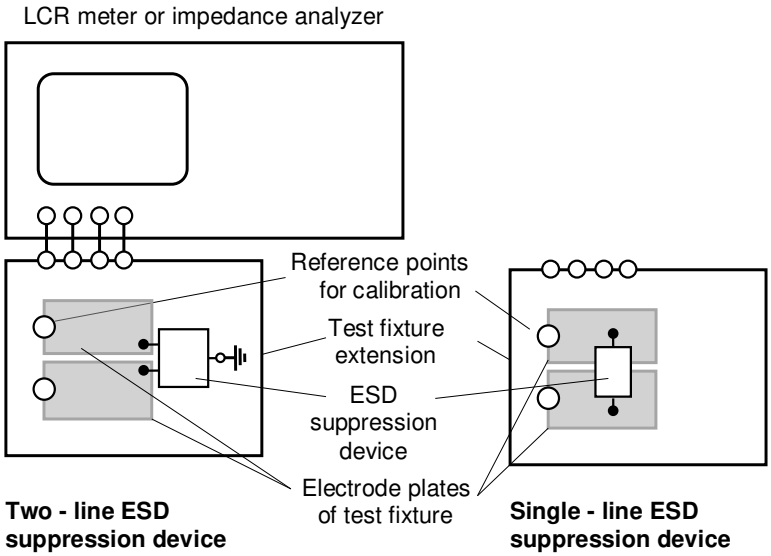


Figure 5-3: Test setup for parasitic capacitance measurement for LCR meter or impedance analyzer method

The test equipment definitions are the following:

- LCR meter or impedance analyzer;
- test fixture extension, direct mounted to the measuring device.

5.2.2.2 Test procedure and parameters

The test procedure and parameters are defined in Table 5-4.

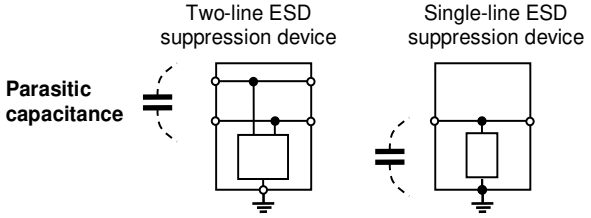
Item	Parameter
Test frequency:	5 MHz
LCR meter or impedance analyzer setting:	Parameter: C_p Measuring voltage: ≥ 100 mV_{rms} DC bias voltage: 0 V
LCR or impedance analyzer measurement circuit:	 Comment: for consistency purpose the value C_p is half of the measurement result for single-line ESD suppression device.

Table 5-4: Test procedure and parameters for parasitic capacitance measurements at ESD suppression device using LCR meter or impedance analyzer method

The tests should be performed at 10 samples and documented. Recommended limits for evaluation are given in Annex A.1.

Test	Item	Sample
CP1	C_{para_max}	10 samples

Table 5-5: Required parasitic capacitance measurements for CMC

5.3 S-parameter measurement mixed mode

5.3.1 Test setup

The test setup for measuring the mixed mode *S*-parameters consists of a 4-port VNA in combination with a special test board (adapter test board). The test board is included into the test setup during VNA calibration. The reference points for calibration are defined to the pads of the ESD suppression device at the test board.

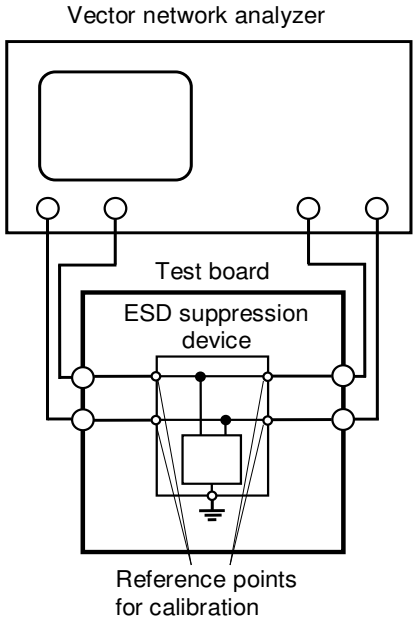


Figure 5-4: Test setup for S-parameter measurements

The test equipment definitions are the following:

- 4-port vector network analyzer;
- test board *S*-parameter mixed mode (4-port) and
- test board *S*-parameter single ended (3-port).

For the *S*-parameter 3-port test board, additional specific requirements are defined. The 3-port test board with soldered RF connectors used for balance measurement should have a very high grade of self-balance. To ensure the test board self-balance characteristic of symmetrical network at logical port 2 (common mode), the traces between the DUT and all resistors (R1, R2 and R3) must be kept highly symmetric and as short as possible. To verify the test board self-balance characteristic, the test parameter and requirements given in Table 5-6 are defined.

Examples for test boards are given in Figure 5-5 and Figure 5-6.

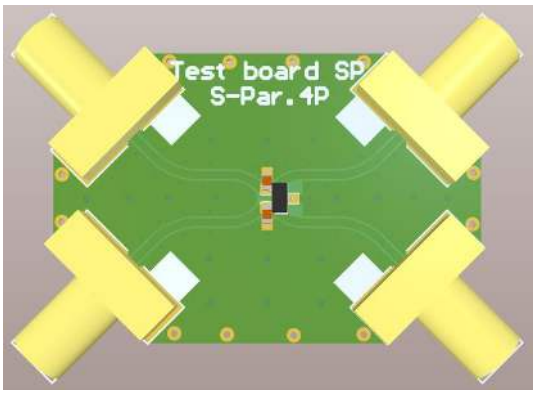


Figure 5-5: Example of test board 4-port S-parameter measurement for ESD suppression device – mixed mode, top layer

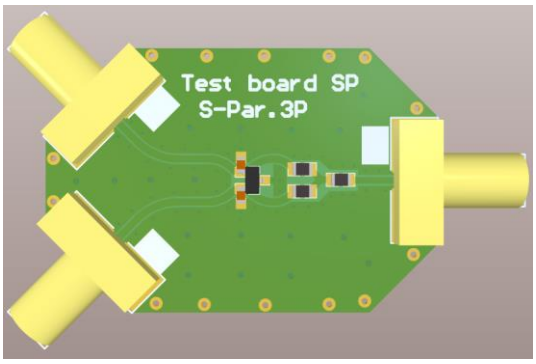


Figure 5-6: Example of test board 3-port S-parameter measurement ESD suppression device – single ended, top layer

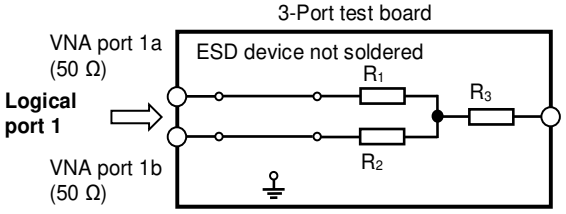
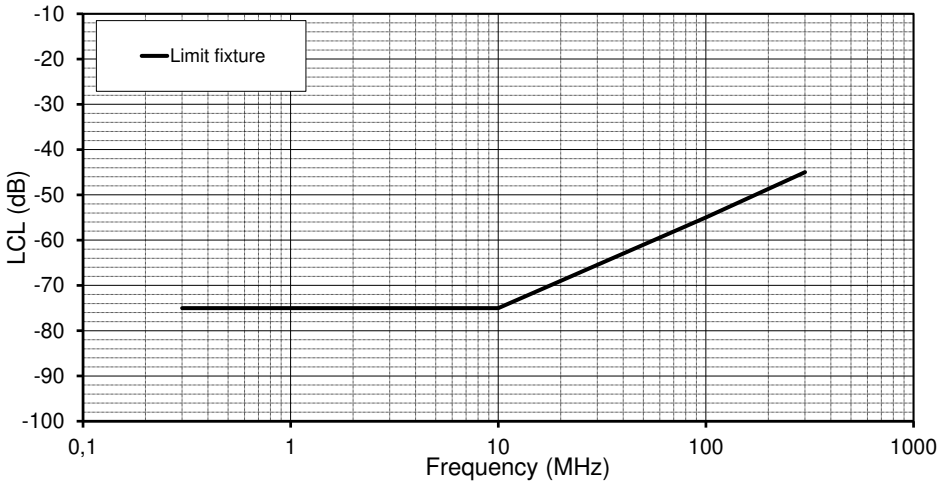
Parameter	Description
Frequency range:	0.3 MHz to 1 GHz
S-parameter:	S_{dc11} (LCL), logarithmic magnitude in dB / differential port side of 3-port test board.
VNA measurement circuit:	port definitions: mixed mode logic port 1: physical port 1a and port 1b differential mode input (logical port 1): 50 Ω impedance each  R = 49,9 Ω for R_1 and R_2 R = 124 Ω for R_3 The ESD suppression device should not be populated at the test board for self-balance measurement.
Requirement for 3-port fixture:	**S - Parameter / ESD supression device for Ethernet 10BASE-T1S** Item: Self-balance requirement for 3-Port test fixture Longitudinal Conversion Loss / LCL (S_{cd11}) [MHz] / Limit fixture: 0,3 / -75; 10 / -75; 100 / -55; 300 / -45 

Table 5-6: Test procedure and parameters for 3-port test board characterization for ESD suppression device

5.3.2 Test procedure and parameters

The test procedure and parameters are defined in Table 5-7.

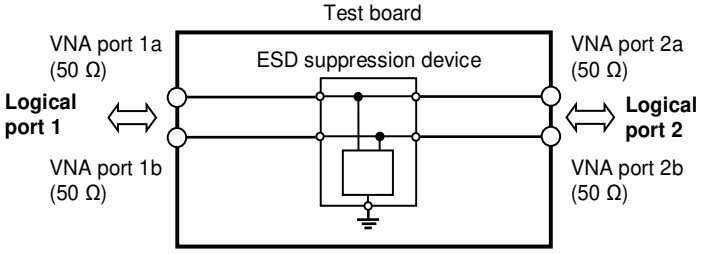
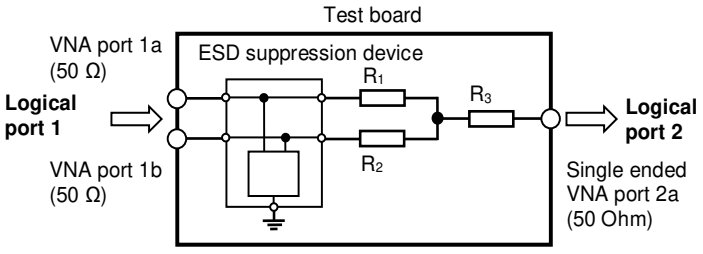
Item	Parameter
Frequency range:	0.3 MHz to 1 GHz
S-parameter per single path:	4-port parameters S_{dd11} (RL), logarithmic magnitude in dB S_{dd21} (IL), logarithmic magnitude in dB 3-port parameters S_{sd21} (DCMR), logarithmic magnitude in dB
VNA measurement circuit:	port definitions: mixed mode logic port 1: physical port 1a and port 1b mixed mode logic port 2: physical port 2a and port 2b 4-port measurements / S_{dd11} and S_{dd21}mixed mode: 50 Ω input impedance at each measurement port  3-port measurements / S_{sd21} single ended: differential mode input (logical port 1): 50 Ω impedance each common mode output (logical port 2): single ended network with 200 Ω impedance $R = (R_1 \mid\mid R_2) + R_3 + R_{\text{VNA port 2a}}$  $R_1 = R_2 = 49.9\ \Omega$, $R_3 = 124\ \Omega$ The accuracy of resistor values should be ≤ 1 %. The difference between matching resistors should be ≤ 0.1 %.

Table 5-7: Test procedure and parameters for S-parameter measurements at ESD suppression device

The measurements should be performed and documented according to the scheme given in Table 5-8.

Test	S-parameter	Sample
S1	S_{dd11} (RL)	10 samples each
S2	S_{dd21} (IL)	
S3	S_{sd21} (DCMR)	

Table 5-8: Required S-parameter measurements for ESD suppression device

For each test case, the results for all 10 samples should be documented as diagram in the ESD suppression device characterization report. Recommended limits for evaluation are given in Annex A.2.

5.4 ESD damage

5.4.1 Test setup

The test setup given in Figure 5-7 is used for testing the ESD robustness of ESD suppression device.

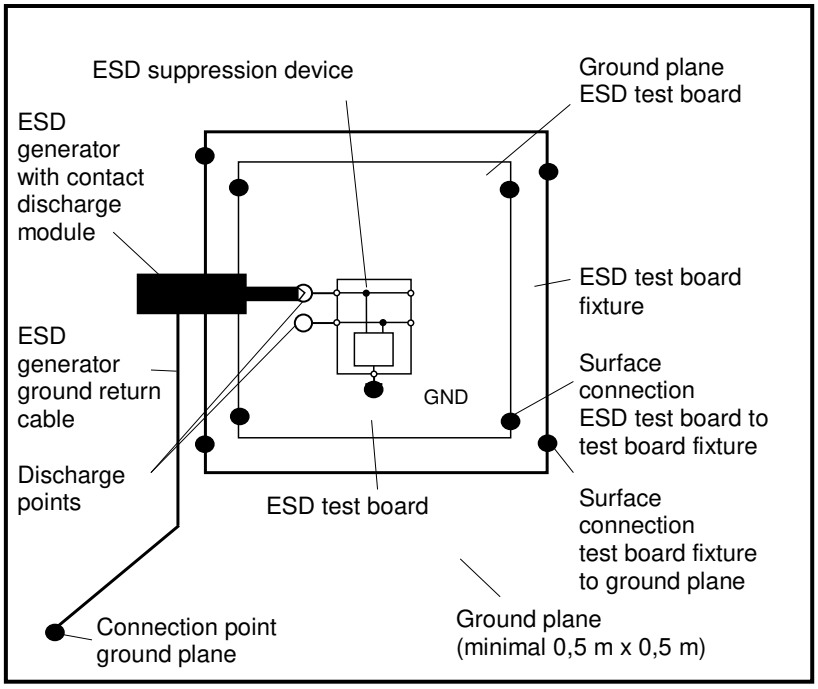


Figure 5-7: Test setup for ESD damage tests at ESD suppression device

The test equipment definitions are the following:

- ESD generator (according to ISO 10605, discharge storage capacitor C = 150 pF and discharge resistor *R* = 330 Ω);
- ESD test board;
- ground plane and
- test board fixture.

The ground plane with a minimum size of 0.5 m × 0.5 m is connected to protective earth of the electrical grounding system of the test laboratory. The ESD generator ground return cable is directly connected to this ground plane. The metallic test fixture positions the ESD test board and directly connects the ESD test board ground plane to the reference ground plane. The ground connection of the test fixture is connected to ground plane with low impedance and low inductance. This surface connection should have a contact area of at least 4 cm^2. Copper tapes can be used in addition. The tip of the ESD generator is directly contacted with one of the discharge points DP1 and DP2 of the ESD test board for testing. For this purpose, the discharge points can be implemented as rounded landing pads or vias in the layout of the ESD test board and are directly connected by a trace 15 (±5) mm with the respective pin of the ESD suppression device.

An example for ESD test board is given in Figure 5-8.

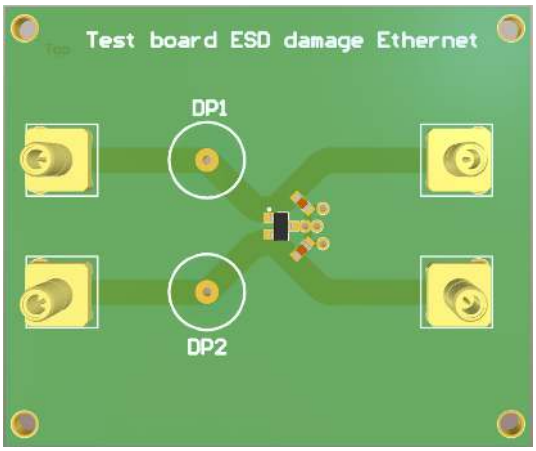


Figure 5-8: Example of ESD test board for ESD suppression device, top layer

For check of damage evaluation criteria (S-parameter), the reference points for calibration are the input of RF connector (SMA) at the test board.

To achieve a high grade of accuracy of required *S*-parameter measurements for damage evaluation, it is recommended to use the same test board for *S*-parameter and ESD tests without re-soldering the DUT.

5.4.2 Test procedure and parameters

The required tests and procedure are defined in Table 5-9 and should be done on one sample.

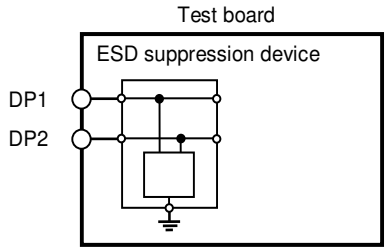
Item	Parameter
Coupling of ESD:	Direct discharge method according to ISO 10605 (discharge storage capacitor C = 150 pF and discharge resistor R = 330 Ω)
Test circuit:	
ESD test voltage:	± 8 kV, ± 15 kV
Number of discharges:	20 per polarity
Time between discharges:	5 s
Damage evaluation criteria:	– degrade by more than 0,1 dB from the initial value after performing the tests for S-parameter S_{dd21} for frequencies $f \leq 200$ MHz – degrade by more than 1 dB from the initial value after performing the tests for S-parameter S_{dd11}, S_{dd22} and S_{cd21} for frequencies $f \leq 200$ MHz The S-parameter measurements should be done according to 5.3. Frequency ranges or frequency spots with a level at noise floor or below the related limits of 5.3 should not be weighted for applying the damage evaluation criteria. For simplification of measurement for check of mode conversion loss the S-parameter S_{cd21} is used instead of S_{sd21}. The setup for S-parameter S_{cd21} is same as used for the other required S-parameter. Because of different test circuitry for S-parameter S_{cd21} and S_{sd21} the related limit for S-parameter S_{cd21} is corrected by + 10 dB.
Test procedure:	1. *S*-parameter reference measurement before ESD test 2. apply ESD discharges at DP1 (± 8 kV, 10 per polarity, 5 s delay) 3. apply ESD discharges at DP2 (± 8 kV, 10 per polarity, 5 s delay) 4. evaluate damage using damage evaluation criteria 5. apply ESD discharges at DP1 (± 15 kV, 10 per polarity, 5 s delay) 6. apply ESD discharges at DP2 (± 15 kV, 10 per polarity, 5 s delay) 7. evaluate damage using damage evaluation criteria If a damage occurs at ± 8 kV or ± 15 kV the test should be repeated with a reduced ESD test voltage to find out the immunity threshold of the DUT. Nevertheless, applying an ESD test voltage of ± 15 kV without damage for DUT is required to pass the test.

Table 5-9: Test parameters for ESD damage tests at ESD suppression device

The measurements should be performed and documented according to the scheme given in Table 5-10.

Test	Discharge point	Comment	Sample
E1	DP1	Line 1	3 samples
E2	DP2	Line 2	

Table 5-10: Required ESD tests for damage for ESD suppression device

The ESD suppression device should withstand the ESD discharge without damage according to the damage evaluation criteria. Recommended limits are given in Annex A.3.

5.5 ESD discharge current measurement

5.5.1 Test setup

The setup given in Figure 5-9 should be used for measuring the ESD discharge current through a 10BASE-T1S transceiver simulation network if the ESD suppression device is used as a part of the MDI network.

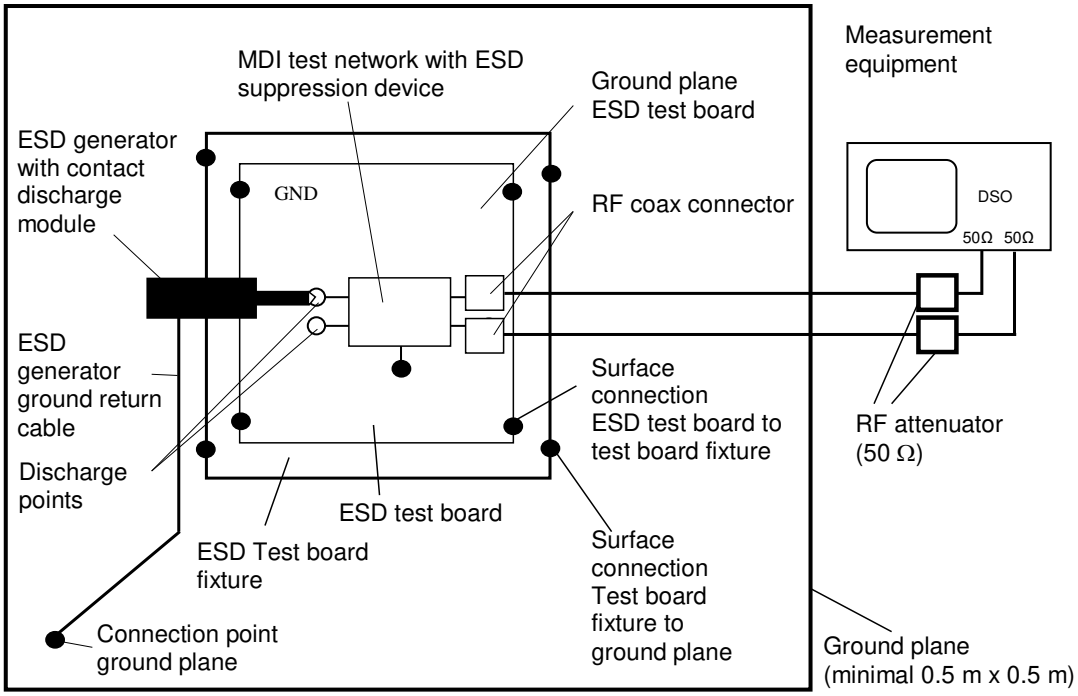


Figure 5-9: Test setup for ESD discharge current measurement

The test equipment definitions are the following:

- ESD generator (according to ISO 10605, discharge storage capacitor C = 150 pF and discharge resistor R = 330 Ω);
- digital storage oscilloscope (DSO, 50 Ω input impedance, minimum 1GHz analog input bandwidth);
- RF attenuator (50 Ω);
- ESD test board discharge current;
- ground plane, and
- test board fixture.

The ground plane with a minimum size of 0.5 m × 0.5 m is connected to protective earth of the electrical grounding system of the test laboratory. The ESD generator ground return cable is directly connected to this ground plane. The metallic test fixture positions the ESD test board and directly connects the ESD test board ground plane to the reference ground plane. The ground connection of the test fixture is connected to ground plane with low impedance and low inductance. This surface connection should have a contact area of at least 4 cm2. Copper tapes can be used in addition. For reduction of parasitic field coupling from ESD generator into the test circuit it is recommended to position the ESD test board with passive components on bottom side into the metallic test fixture.

The tip of the ESD generator is directly contacted with one of the discharge points DP1 and DP2 of the ESD test board for testing. For this purpose, the discharge points are implemented as rounded vias in the layout of the ESD test board and are directly connected by a trace 15 (±5) mm with the respective pin of the ESD suppression device.

Shielded cables are used for connection of measurement outputs of the MDI test network on the ESD test board to the DSO's 50 Ω inputs. An additional attenuator is recommended to prevent the DSO inputs from damage. Care should be taken that the used DSO is not influenced by the ESD discharge event.

A verification of used test setup shall be performed using the test parameter and requirements defined in Table 5-11.

An example for ESD test board discharge current is given in Figure 5-10.

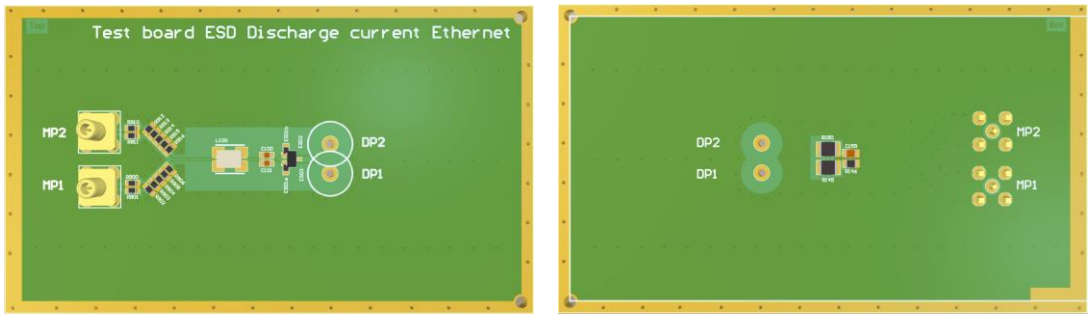


Figure 5-10: Example of ESD test board discharge current for ESD suppression device, top and bottom layer

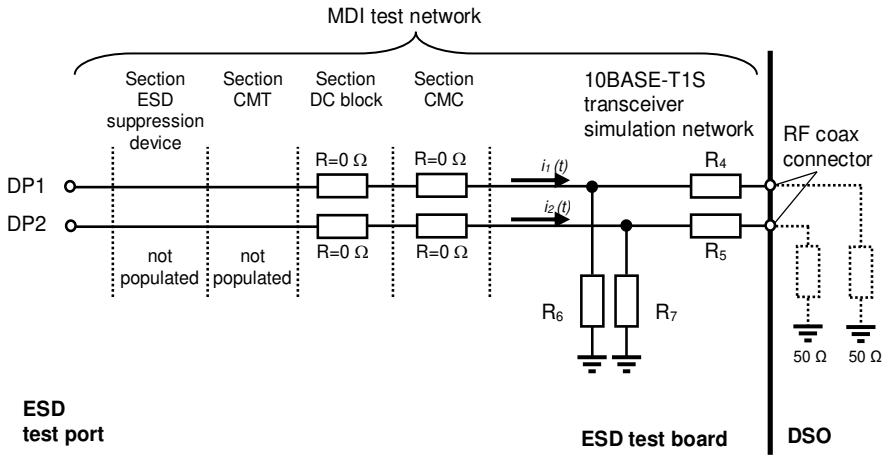
Item	Parameter
Coupling of ESD:	Direct discharge method according to ISO 10605 (discharge storage capacitor C = 150 pF and discharge resistor R = 330Ω)
Test circuit:	 See test circuit definition given in Table 5-12 with changed passive components of MDI test network except 10BASE-T1S transceiver simulation network: • serial elements shorted with resistor R = 0 Ω or small wire • elements to ground not populated
ESD test voltage:	+ 6 kV
Requirement:	measured ESD discharge current shapes i_1(t) and i_2(t) with an analog bandwidth setting of 1 GHz at the used DSO shall fulfill the contact discharge mode current specification of ISO 10605: • peak current: 22.5 A ± 2.5 A • current at t_1 = 30 ns: 12 A ± 3.6 A • current at t_1 = 60 ns: 6 A ± 1.8 A

Table 5-11: Test procedure and parameters for ESD discharge current measurement test board characterization

5.5.2 Test procedure and parameters

The required test procedure and parameters are defined in Table 5-12.

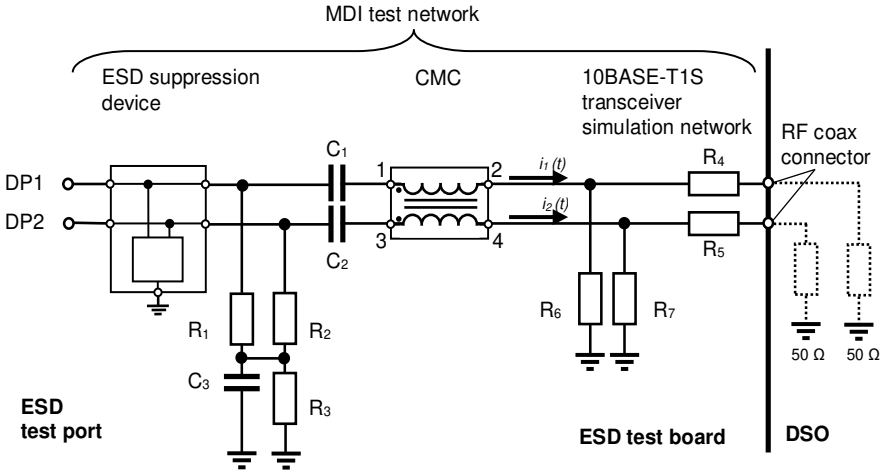
Item	Parameter
Coupling of ESD:	Direct discharge method according to ISO 10605 (discharge storage capacitor C = 150 pF and discharge resistor R = 330Ω)
Test circuit:	 $C_1 = C_2 = 100$ nF, $C_3 = 100$ nF $R_1 = R_2 = 1.5$ kΩ (≤ 1 %), $R_3 = 100$ kΩ, $R_4 = R_5 = 50$ Ω, $R_6 = R_7 = 2$ Ω The CMC should fulfil the related requirements given in [4]. If available, a representing CMC for each CMC ESD saturation class I and II should be used for testing. All resistors R_1 and R_2 have SMD design 1206 or larger. To achieve low inductance value for resistors R_4, R_5, R_6 and R_7 a parallel circuit of resistors with higher nominal value and SMD design 0603 or 0402 is recommended.
ESD test voltage:	± 3 kV, ± 5 kV, ± 6 kV, ± 7 kV, ± 15 kV
Evaluation criteria:	measured ESD discharge current shapes i_1(t) and i_2(t) with an analog bandwidth setting of 1 GHz at the used DSO

Table 5-12: Test procedure and parameters for ESD discharge current measurement

The tests should be performed and documented according to the scheme given in Table 5-13.

Test	Discharge point	Comment	ESD saturation class of used CMC according to [4]	Sample
E1	DP1	Line 1	I	3 samples each
E2			II	
E3	DP2	Line 2	I	
E4			II	

Table 5-13: Required current measurement for ESD suppression device

For each test case the remaining ESD discharge current waveform, measured after the MDI test network, should be recorded and documented in a diagram in the test report. The measured ESD discharge current waveform should be below the recommended limits given in Annex A.4.

5.6 Test of unwanted clamping effect at RF immunity tests

5.6.1 Test setup

The test setup for measuring the unwanted clamping effect of ESD suppression device at RF immunity tests of a RF generation unit, consisting of RF generator, RF amplifier, RF power meter with directional coupler, in combination with a special test board, RF attenuator and RF power analyzer. The test setup is given in Figure 5-11.

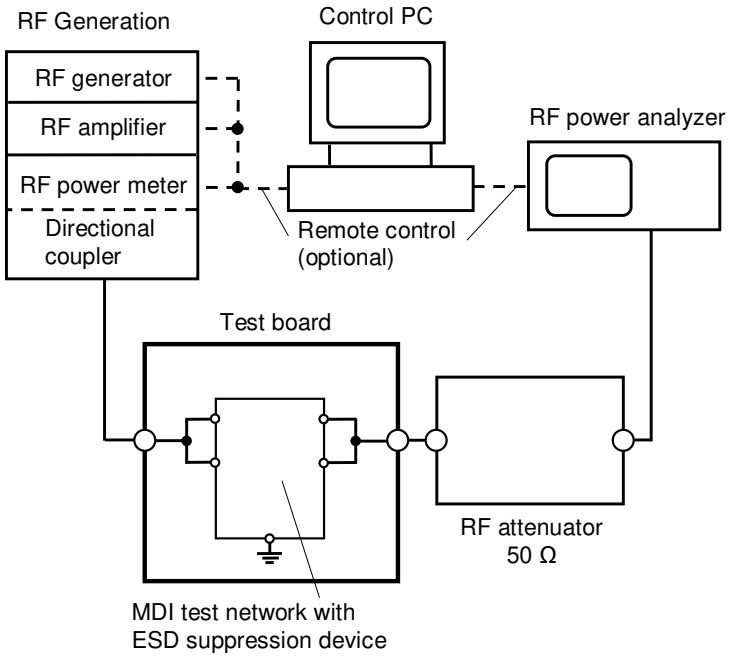


Figure 5-11: Test setup for RF clamping test at ESD suppression device

The test equipment definitions are the following:

- RF generator;
- RF amplifier (output impedance 50 Ω, $P_{CW} \geq 10$ W);
- RF power meter with directional coupler;
- test board;
- RF attenuator (impedance 50 Ω, $P_{CW} \geq 10$ W, ≥ 40 dB attenuation), and
- control PC (optional).

An example for RF clamping test board is given in Figure 5-12.

Figure 5-12: Example of RF clamping test board for ESD suppression device, top layer

5.6.2 Test procedure and parameters

The required test procedure and parameters are defined in Table 5-14.

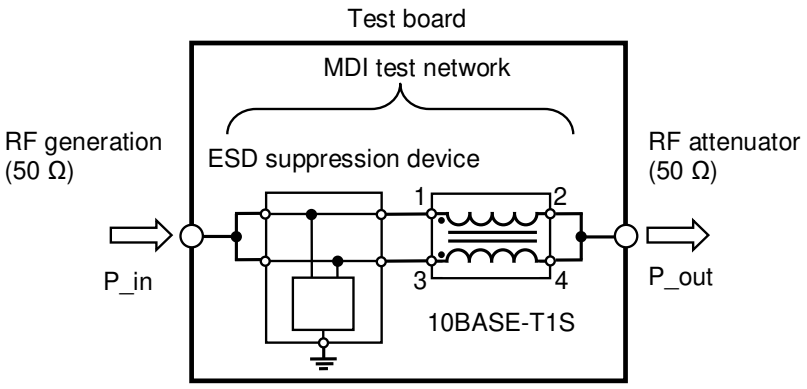
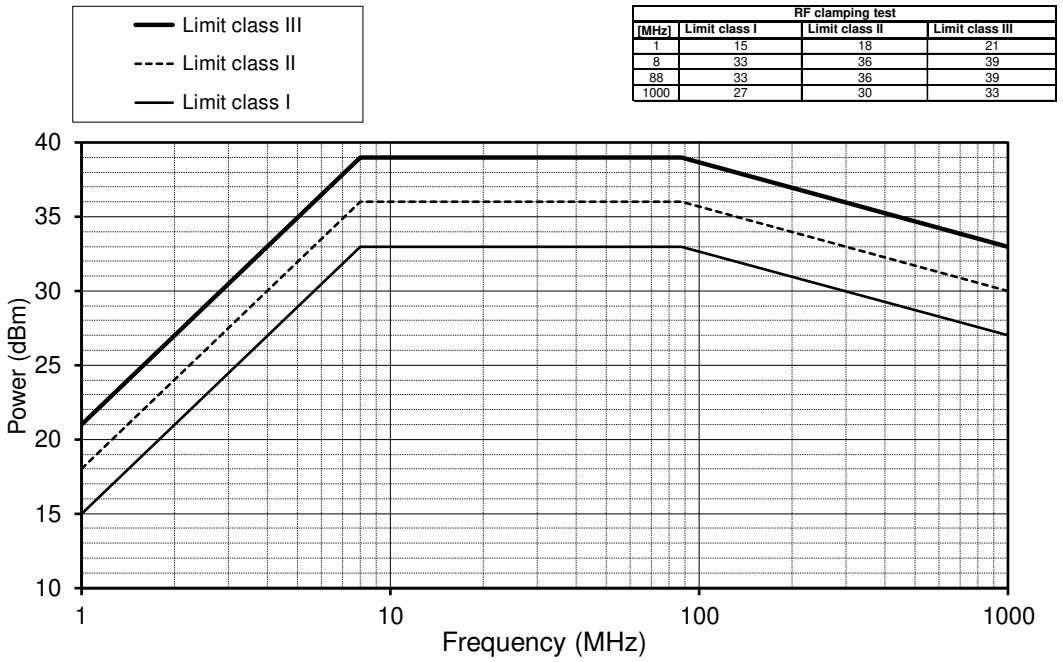
Parameter	Description	
Frequency:	Range	Step
	1 MHz to 10 MHz	0.25 MHz
	10 MHz to 100 MHz	1 MHz
	100 MHz to 200 MHz	2 MHz
	200 MHz to 400 MHz	4 MHz
	400 MHz to 1000 MHz	10 MHz
Dwell time per step:	1 s	
Modulation:	AM 80 % 1 kHz ($\hat{P}_{AM} = \hat{P}_{CW}$)	
Test parameter:	CMR value	
Test circuit:	 Note: The used CMC should fulfil the requirements of [4]. Calculation of MDI test network CMR value: CMR(f) = *P_in*(f) – *P_out*(f)	
Test power level:	Controlled forward power [dBm] for classes according to Figure 5-13	
Test procedure:	1. test with test power 20 dBm for setting the reference value for CMR 2. test with power level class I according Figure 5-13 3. test with power level class II according to Figure 5-13 4. test with power level class III according to Figure 5-13	
Evaluation of clamping effect:	Maximum deviation of 1 dB from CMR reference value at 20 dBm for test power level according to limit classes	

Table 5-14: Test parameters for RF clamping test



RF clamping test			
[MHz]	Limit class I	Limit class II	Limit class III
1	15	18	21
8	33	36	39
88	33	36	39
1000	27	30	33

Figure 5-13: Recommended test power levels for RF clamping tests at ESD suppression device

The tests should be performed at one sample and documented according to the scheme given in Table 5-15.

Test	Parameter	Sample
RF-CL	CMR	1 sample

Table 5-15: Required RF clamping test for ESD suppression device

The ESD suppression device should not show an unwanted clamping effect during the RF immunity test according to the evaluation criteria. Recommended limits are given in Annex A.5.

Annex A

Recommended limits for tests

A.1 Parasitic capacitance

It is recommended that the parasitic capacitance of ESD suppression device, measured between the two pins of a two-line device that connect the MDI lines of a 10BASE-T1S interface while the GND pin of the device is connected to common GND, is less or equal to 1 pF. In case of usage single-line devices, this limit applies to two elements of the same type in series.

A.2 S-parameter measurement mixed mode

For evaluation of mixed mode S-Parameters the limits given in Figure A-1 to Figure A-3 are recommended.

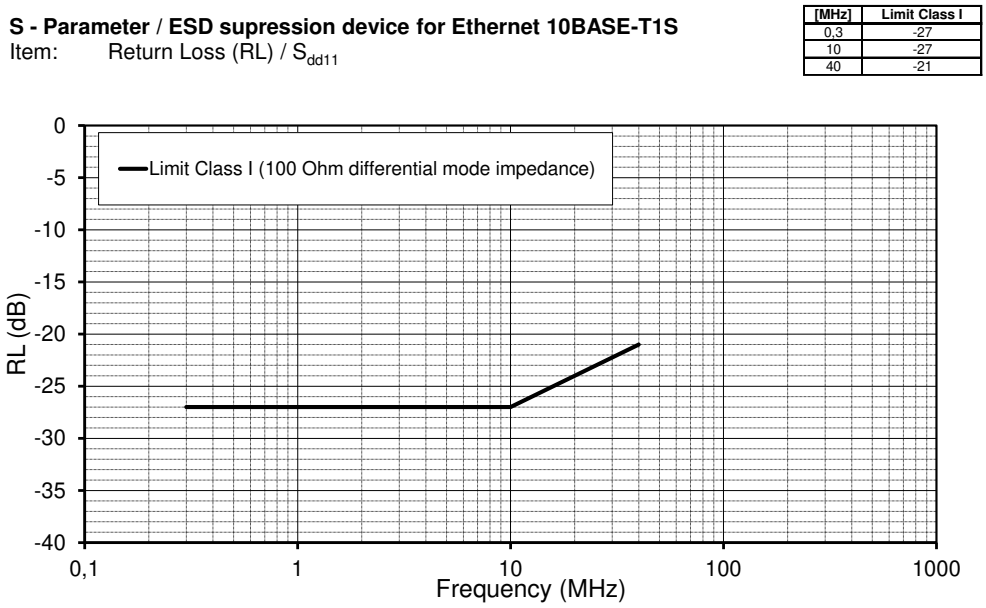


Figure A-1: Recommended characteristics for Sdd11 (RL) for ESD suppression device

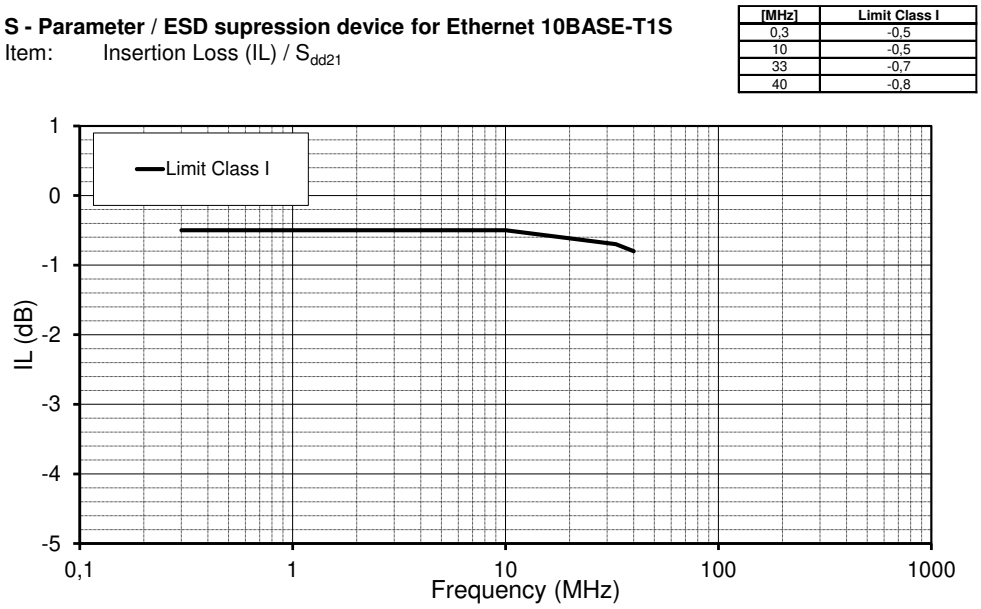


Figure A-2: Recommended characteristics for *S*dd21 (IL) for ESD suppression device

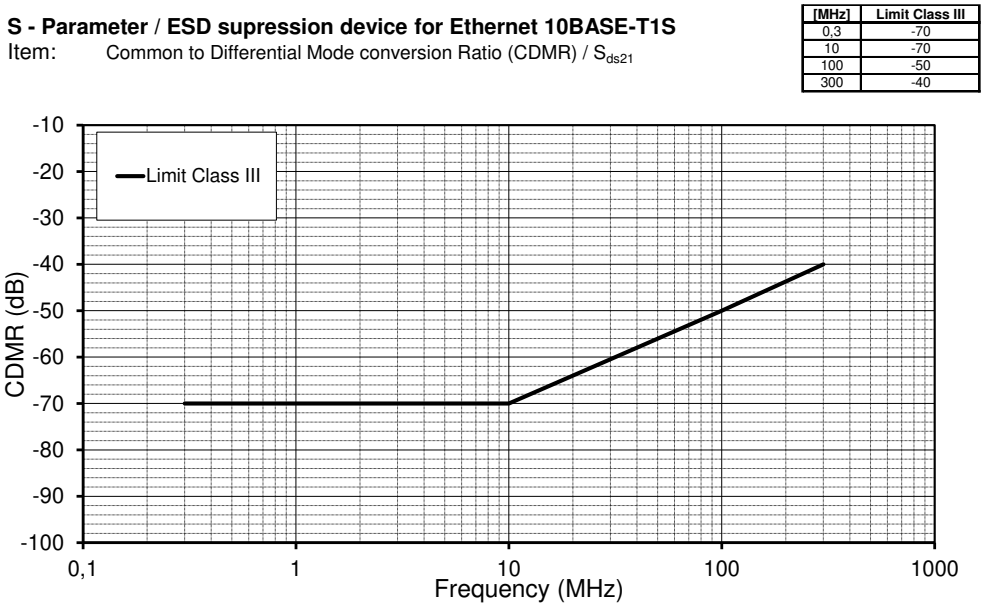


Figure A-3: Recommended characteristics for Ssd21 (DCMR) for ESD suppression device

A.3 ESD damage

It is recommended that the ESD suppression device must withstand the ESD discharge with discharge voltage amplitude of +/- 15 kV without damage.

A.4 ESD Discharge Current Measurement

For evaluation of the impact of ESD suppression device to ESD discharge current through a 10BASE-T1S MDI test network limits given in Figure A-4 for positive ESD test voltages are recommended. For negative ESD test voltages the given limits with inverted amplitudes should be applied.

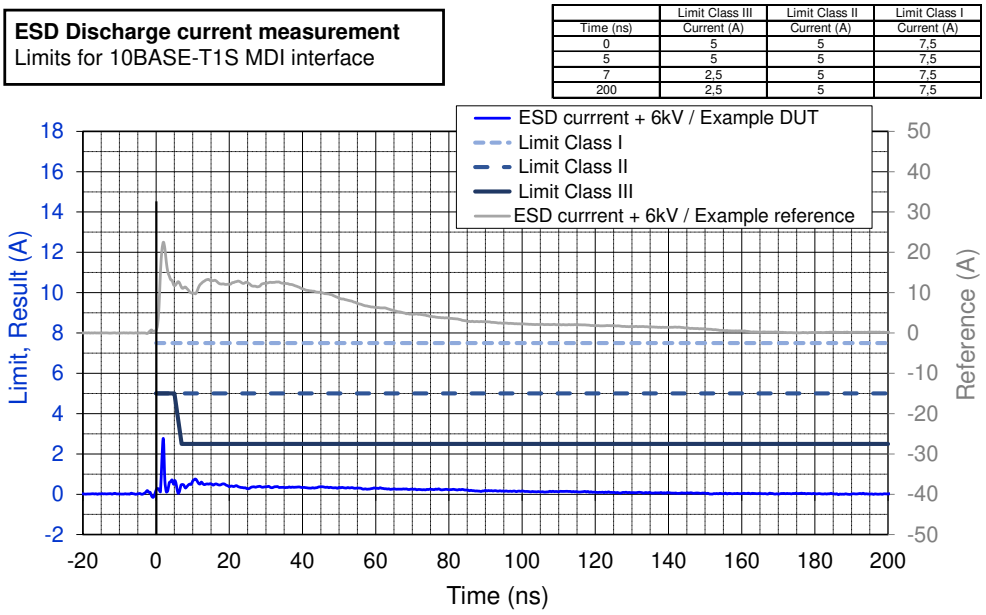


Figure A-4: Recommended limits for ESD discharge current

NOTE The example reference of ESD discharge current shape given in Figure A-4 is the measurement result of the test board configuration without mounted components CMC, C_1, C_2, C_3, R_1, R_2 and ESD suppression device of the test circuitry given in Table 5-11, while series components are shorted by R = 0 Ω.

Table A-1 shows the relation between the required ESD robustness of the MDI interface that should be achieved using the ESD suppression device, the ESD robustness of Ethernet transceiver to be protected, applicable ESD test voltages and the related limit classes for the ESD suppression device.

ESD robustness requirement on MDI interface	ESD robustness of transceiver to be protected	ESD test voltages to be applied at MDI test network	Limit class for ESD suppression device
± 6 kV	at least ± 2 kV and less than ± 6 kV	± 3 kV and ± 6 kV	III
± 6 kV	at least ± 4 kV and less than ± 6 kV	± 5 kV and ± 6 kV	II
± 15 kV	at least ± 2 kV and less than ± 15 kV	± 3 kV and ± 15 kV	III
± 15 kV	at least ± 4 kV and less than ± 15 kV	± 5 kV and ± 15 kV	II
± 15 kV	at least ± 6 kV and less than ± 15 kV	± 7 kV and ± 15 kV	I
Note: The ESD robustness of transceiver to be protected is a result of ESD test according to [5].			

Table A-16: Limit classes and related applied ESD test voltages

A.5 Test of unwanted Clamping Effect at RF Immunity Tests

It is recommended that the ESD suppression device doesn't show an unwanted clamping effect during the RF immunity test with a power level of limit class III according to Figure 5-13.

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