IEEE 1000BASE-T1 EMC Test Specification for Common Mode Chokes

Version 2.0

Author & Company	Dr. Bernd Körber, FTZ Zwickau
Title	1000BASE-T1 EMC Test Specification for Common Mode Chokes
Version	2.0
Date	June 20, 2020
Status	Final
Restriction Level	Public

This measurement specification shall be used as a standardized common scale for EMC evaluation of common mode chokes for 1000BASE-T1 in automotive applications.

Version Control of Document

Version	Author	Description	Date
0.1	B. Körber	Initial document	05/26/16
0.2	B. Körber	• Editorial changes • Reference to EMC test specification for transceiver deleted • Measurement network for single ended S-Parameter measurements changed • Example for ESD test board added • Formula expression added for recommended limits • Section TDR tests shifted to informative Appendix	08/20/16
0.3	B. Körber	• Editorial changes • Limit for S-Parameter IL added	12/05/16
0.4	B. Körber	• Disclaimer updated • Evaluation criteria and test procedure for ESD damage test changed • Test board for ESD tests changed • Limits for CMR, DCMR and CDMR changed • TDR measurement shifted to optional annex	07/27/17
0.5	B. Körber	• Editorial changes • Requirements for test fixture added	08/16/17
1.0	B. Körber	• Shift to final version	01/16/18
1.0 rev.	B. Körber	Adaptations to IEC 62228-5 draft version	12/30/18
1.0 rev.2	B. Körber	• Editorial changes • Description of RF saturation test changed (no technical change)	03/19/19
1.0 rev.3	B. Körber	• Editorial changes • Adaptations to IEC 62228-5 draft version • Load resistors for ESD damage test changed • S-Parameter LCL measurement added • ESD saturation test added	01/25/20
2.0	B. Körber	Shift to final version	06/20/20

Restriction level history of Document

Version	Restriction Level	Description	Date
0.1	Open internal only		05/26/16
0.2	Open internal only		08/20/16
0.3	Open internal only		12/05/16
0.4	Open internal only		07/27/17
0.5	Open internal only		08/16/17
1.0	Public		01/06/18
1.0 rev.	Open internal only		12/30/18
1.0 rev.2	Open internal only		03/19/19
1.0 rev.3	Open internal only		01/25/20
2.0	Public		06/20/20

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Contents

1 Introduction

1.1 Scope

This measurement specification shall be used as a standardized common scale for EMC evaluation of common mode chokes (CMCs) intended to use with 1000BASE-T1 in automotive applications according to [IEEE1]. It contains recommended limits. The final judgment of the tested device is left to the customer.

This specification does not cover devices that are intended for use in [IEEE2] Power over Data Line applications.

This instruction includes test procedures and test setups concerning:

- mixed mode S-Parameter measurement
- test of damage from ESD
- test of saturation effect at RF immunity tests
- test of saturation effect at ESD tests.

For optional TDR measurement of differential mode impedance procedures and test setup are given in an informative appendix.

1.2 References

[IEEE1] IEEE Std. 802.3bp

[IEEE2] IEEE Std. 802.3bu

[IEC1] IEC 62615, Electrostatic discharge sensitivity testing - Transmission line pulse (TLP) - Component level

[ISO1] ISO 10605, Road vehicles – Test methods for electrical disturbances from electrostatic discharge

1.3 List of abbreviations and definitions

CDMR	Common to Differential Mode Rejection, common mode single ended measured
CMC	Common Mode Choke
CMR	Common Mode Rejection
DCMR	Differential to Common Mode Rejection, common mode single ended measured
ESD	Electro Static Discharge
IL	Insertion Loss
LCL	Longitudinal Conversion Loss
RF	Radio Frequency
RL	Return Loss
S-Parameter	Scattering Parameter
TDR	Time Domain Reflection
VNA	Vector Network Analyzer

2 Required Tests

2.1 General

For evaluation of EMC behaviour of the CMC the following tests are defined:

- mixed mode S-Parameter
- damage from ESD
- saturation test with RF power exposure
- saturation test with ESD exposure
- optional TDR measurement.

Prior to performing any ESD, RF and optional TDR tests, the S-Parameter measurements shall be performed on a minimum of 10 samples.

A general electrical drawing with winding and pin definitions of a CMC is shown in Figure 2-1.

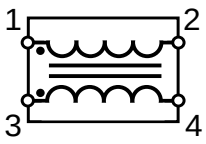


Figure 2-1: General electrical drawing of a CMC

For the measurements described below the CMC line 1 is defined as the CMC winding between pin 1 and pin 2 and line 2 is defined as the winding between pin 3 and pin 4.

2.2 Mixed mode S-Parameter measurement

2.2.1 Test setup

For measuring the mixed mode S-Parameters a 4-port VNA in combination with a special test fixture (adapter test board) shall be used. The test fixture must be included into the test setup during calibration of VNA test setup. The reference points by calibration are defined to the pads of the CMC at the test fixture board.

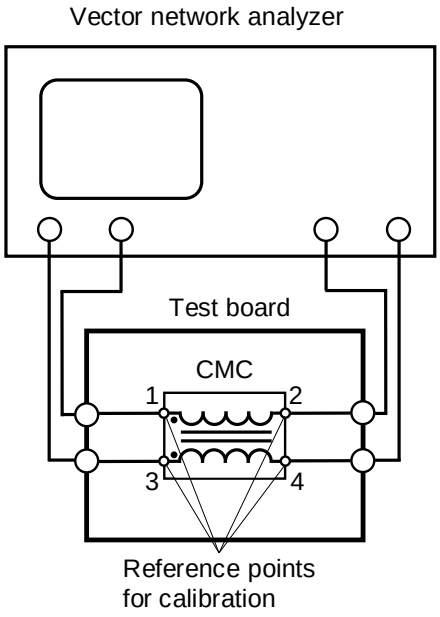


Figure 2-2: Test setup for S-Parameter measurements

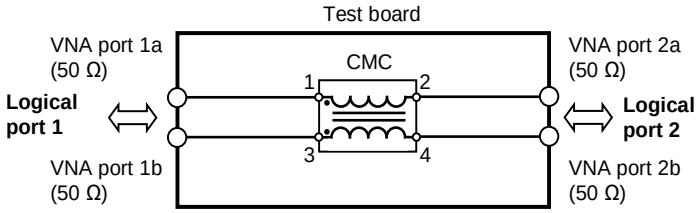
Test equipment requirements:

Network analyzer:	4-port vector network analyzer f = 1 MHz to 1000 MHz (in minimum)
Test fixture:	according to Appendix A

To achieve a high sensitivity and accuracy of balance measurements results and to avoid a dominance of test fixture characteristics to the balance measuring results the use test fixture shall fulfil the requirement for self-balance, given in section A.2.

2.2.2 Test procedure and parameters

The required measurements are defined in Table 2-1.

Parameter	Description
Frequency range:	1 MHz to 1 GHz, logarithmic scale
S-Parameter per single path:	S_{dd11} (RL), log. Magnitude in dB / CMC orientation 1 S_{dd22} (RL), log. Magnitude in dB / CMC orientation 2 S_{dd21} (IL), log. Magnitude in dB S_{cc21} (CMR), log. Magnitude in dB S_{dc11} (LCL), logarithmic magnitude in dB / CMC orientation 1 S_{dc22} (LCL), logarithmic magnitude in dB / CMC orientation 2 S_{sd21} (DCMR), log. Magnitude in dB / CMC orientation 1 S_{sd12} (DCMR), log. Magnitude in dB / CMC orientation 2 S_{ds21} (CDMR), log. Magnitude in dB / CMC orientation 1 S_{ds12} (CDMR), log. Magnitude in dB / CMC orientation 2 For S_{dc22}, S_{sd12} and S_{ds12} measurement the terminal orientation of the CMC is rotated on the test board.
VNA measurement circuit:	Port definitions: Mixed mode logic port 1: physical port 1a and port 1b Mixed mode logic port 2: physical port 2a and port 2b Pin 1 of CMC is placed on logic port 1. S_{dd11}, S_{dd22}, S_{dd21} and S_{cc21} measurement: 50 Ω input impedance at each measurement port  S_{dc11}, S_{dc22}, S_{sd21}, S_{sd21}, S_{sd12},S_{ds21} and S_{ds12} measurement: Differential mode input (logical port 1): 50 Ω impedance each Common mode output (logical port 2): symmetrical single ended network with 200 Ω impedance $R = R_1 \mid\mid R_2 + R_3 + R_{VNA\ port\ 2a}$

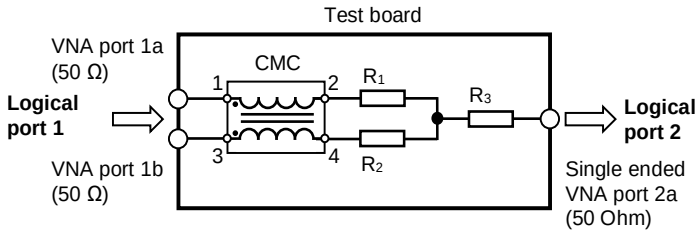
VNA measurement circuit (continue):	 $R_1 = R_2 = 49.9\ \Omega$, $R_3 = 124\ \Omega$ Note: The accuracy of resistor values should be ≤ 1 %. The difference between matching resistors should be ≤ 0.1 %.

Table 2-1: Test parameters for S- Parameter measurements

The measurements shall be performed and documented according the scheme given in Table 2-2.

Test	S- Parameter	Sample
S1	S_{dd11} (RL)	10 samples
S2	S_{dd22} (RL)	
S3	S_{dd21} (IL)	
S4	S_{cc21} (CMR)	
S5	S_{dc11} (LCL)	
S6	S_{dc22} (LCL)	
S7	S_{sd21} (DCMR)	
S8	S_{sd12} (DCMR)	
S9	S_{ds21} (CDMR)	
S10	S_{ds12} (CDMR)	

Table 2-2: Required S-Parameter measurements

For each test case the results for all 10 samples must be documented as diagram in the test report. Recommended limits for evaluation are given in Appendix B.1.

2.3 Damage from ESD

2.3.1 Test setup

The setup given in Figure 2-3 shall be used for testing the ESD robustness of CMC.

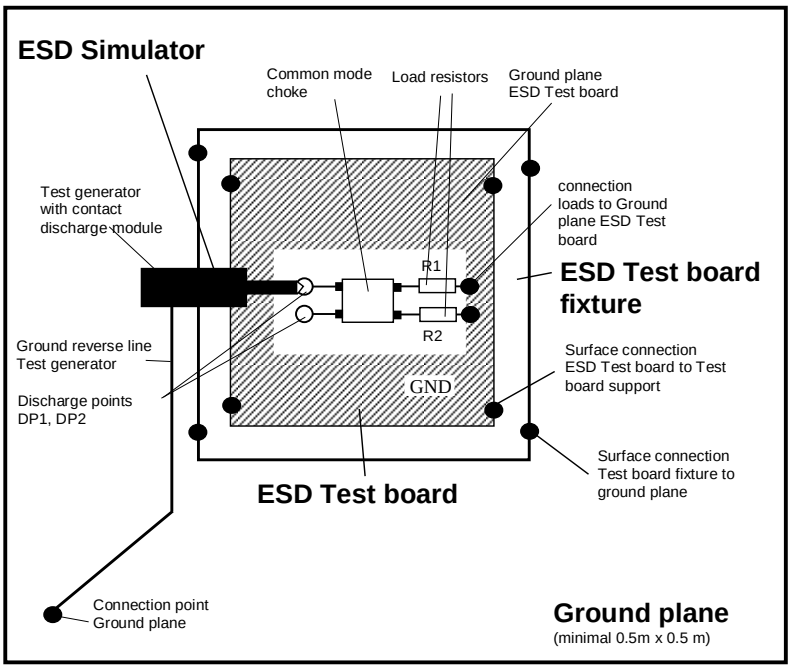


Figure 2-3: Test setup for ESD damage tests

The ground plane with a minimum size of 0.5 m x 0.5 m builds the reference ground plane for the ESD Test setup and must be connected with the electrical grounding system of the test laboratory. The ESD Test generator ground cable shall be connected to this reference plane. The test board fixture realizes the positioning of the ESD Test board and the electrical connection of the ESD Test board ground plane with the reference ground plane. This connection must have low impedance (R < 25 mΩ) and should be built by a surface contact.

During testing the tip of the ESD Test generator discharge module shall be directly contacted with one of the discharge pads DP1 or DP2 of the ESD test board. For this purpose, the discharge points DP1 and DP2 are implemented as rounded vias in the layout of the ESD test board and are directly connected by a trace with the respective pin of the CMC. The trace length should be in a range of 10 mm to 20 mm.

Test Equipment Requirements:

ESD test generator:	according to [ISO1]; contact discharge module with discharge capacitor 150 pF and discharge resistor 330 Ω
ESD test board:	according to Appendix A

2.3.2 Test procedure and parameters

The required tests are defined in Table 2-3 and should be done on one sample.

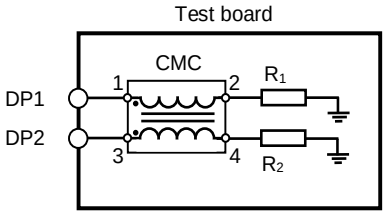
Parameter	Description
Coupling of ESD:	Direct discharge method according to [ISO1] (C = 150 pF, R = 330 Ω)
Test circuit:	 $R_1 = R_2 = 2\ \Omega$ Note: All resistors shall be from the SMD design 1206 or larger with a maximum tolerance of 2 %. The exact type ID and manufacturer of the used resistors must be documented in the test report.
ESD test voltage:	± 8 kV
Number of discharges:	10 per polarity
Time between discharges:	5 s
Damage evaluation criteria:	– deviate by more than 1 dB from the original value after performing the tests for S-Parameter S_{dd11}, S_{dd22}, S_{cd21})$_1$ for frequencies f ≤ 200 MHz – deviate by more than 0.1 dB from the original value after performing the tests for S-Parameter S_{dd21} for frequencies f ≤ 200 MHz)$_1$ for simplification of measurement the S-Parameter S_{cd21} shall be measured with the same test setup as used for the other required parameters. Note: The S-Parameter measurements should be done according to section 2.2. Level at noise floor or below the related limits of section shall be ignored for evaluation.
Test procedure:	1. S-Parameter reference measurement before ESD test 2. Apply ESD discharges at DP1 (± 8 kV, 10 per polarity, 5 s delay) 3. Apply ESD discharges at DP2 (± 8 kV, 10 per polarity, 5 s delay) 4. Demagnetization of CMC (if needed) 5. Evaluate damage using damage evaluation criteria Note: If a damage occurs at ± 8 kV the test shall be repeated with a reduced ESD test voltage to find out the immunity threshold of the DUT. Nevertheless applying an ESD test voltage of ± 8 kV without damage for DUT is required to pass the test.

Table 2-3: Test parameters for ESD damage tests

The tests shall be performed and documented according the scheme given in Table 2-4.

Test	Discharge points	Comment	Sample
E1	DP1	Line 1	1 sample
E2	DP2	Line 2	

Table 2-4: Required ESD tests for damage

The CMC must withstand the ESD discharge without damage according to the damage evaluation criteria. Recommended limits are given in Appendix B.2.

2.4 Test of saturation effect at RF immunity tests

2.4.1 Test setup

For measuring the saturation effect at RF immunity tests a 4-port VNA or 2-port network analyzer in combination with a RF amplifier, RF attenuator and a special test fixture (adapter test board) shall be used.

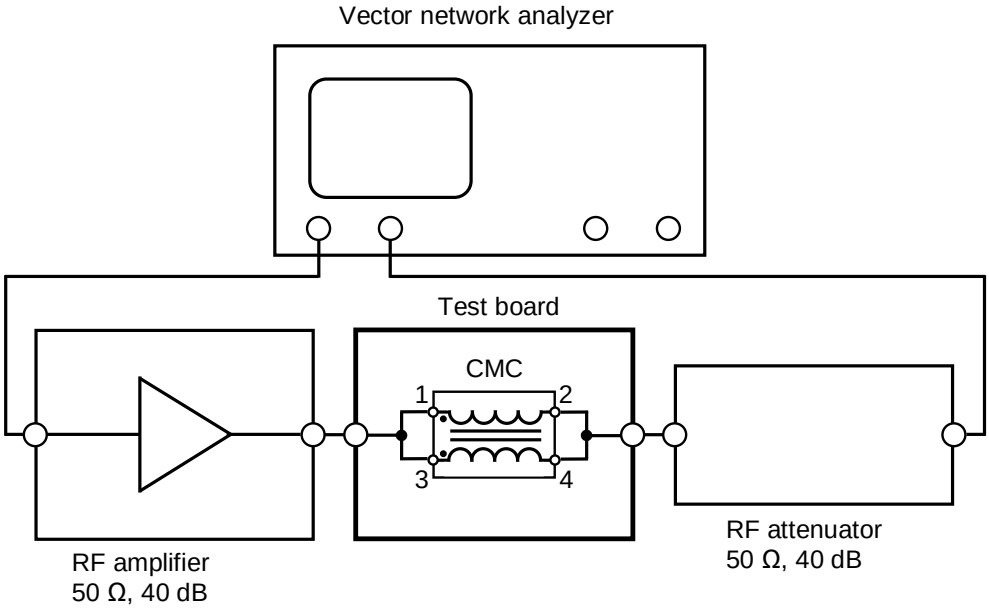


Figure 2-4: Test setup for RF saturation measurements

Test equipment requirements:

Network analyzer:	4-port vector network analyzer or 2-port analyzer f = 1 MHz to 1000 MHz (in minimum)
RF Amplifier:	Impedance 50 Ω, gain 40 dB, $P_{CW} \geq 10$ W
RF Attenuator:	Impedance 50 Ω, attenuation 40 dB
Test fixture:	according to Appendix A

2.4.2 Test procedure and parameters

The required tests are defined in Table 2-5 and should be done on one sample.

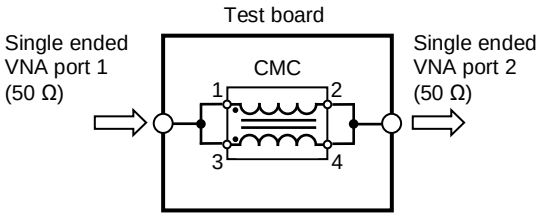
Parameter	Description
Frequency range:	1 MHz to 1 GHz
S-Parameter power level:	S_{21} (CMR), log. Magnitude in dB / transceiver side
VNA measurement test circuit:	Port definitions: Logic port 1: physical port 1 Logic port 2: physical port 2 Pin 1 of CMC is placed on logic port 1 S_{21} measurement: 50 Ω input impedance at each measurement port 
Test power level:	24 dBm, 30 dBm, 33 dBm, 36 dBm Note: These test levels are obtained from test level measurement into a 50 Ohm load.
Dwell time per power level:	≥ 60 s
Evaluation of saturation effect:	Maximum deviation of 1 dB from the CMR reference value at 24 dBm for power level 30 dBm maximum deviation of 1 dB from the CMR reference value at 24 dBm for power level 33 dBm above 5 MHz only maximum deviation of 1 dB from the CMR reference value at 24 dBm for power level 36 dBm above 7 MHz only
Test procedure:	1. Define test equipment settings for test power levels 24 dBm, 30 dBm, 33 dBm, 36 dBm with replacement of test fixture with DUT by a RF thought connection. 2. Test with power level 24 dBm for setting the reference value 3. Test with power level 30 dBm and evaluation 4. Test with power level 33 dBm and evaluation 5. Test with power level 36 dBm and evaluation

Table 2-5: Test parameters for RF saturation measurements

The tests shall be performed and documented according the scheme given in Table 2-6.

Test	S- Parameter	Sample
RFS	S_{21} (CMR)	1 sample

Table 2-6: Required RF saturation measurements

The CMC must withstand the RF power saturation test according to the evaluation criteria. Recommended limits are given in Appendix B.3.

2.5 Test of saturation effect at ESD tests

2.5.1 Test setup

For measuring the saturation effect at ESD tests a TLP test system in combination with digital storage oscilloscope and a special test fixture (adapter test board) shall be used.

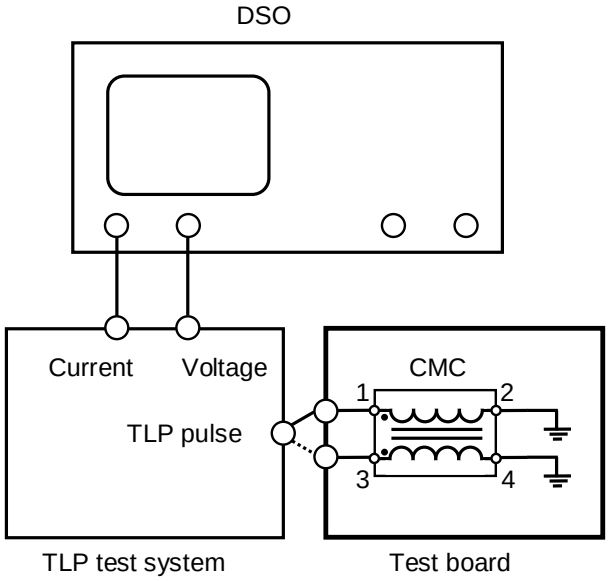


Figure 2-5: Test setup for ESD saturation measurements

Test equipment requirements:

TLP test system:	according to [IEC1], including TLP generator, current probe and voltage probe
Digital storage oscilloscope (DSO):	50 Ω input impedance, minimum 4GHz analog input bandwidth
Test fixture:	according to Appendix A

2.5.2 Test procedure and parameters

The required tests are defined in Table 2-7 and should be done on one sample.

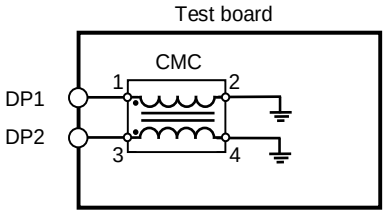
Parameter	Description
Coupling of ESD:	TLP test system according to [IEC1]
Test circuit:	
TLP test parameter:	Current pulse width: 100 ns Current rise time: 600 ps Measurement time window: 10 ns to 90 ns Maximum test voltage: 500 V Test voltage step size: ≤ 2 V Maximum test current: 15 A
Evaluation of saturation effect:	CMC ESD saturation break down voltage V_{ESD_br} derived from measured TLP I/V characteristic and limits according to Appendix B.4.

Table 2-7: Test parameters for RF saturation measurements

The tests shall be performed and documented according the scheme given in Table 2-8.

Test	Discharge point	Comment	Parameter	Sample
ES1	DP1	Line 1	CMC ESD saturation break down voltage	1 sample
ES2	DP2	Line 2		

Table 2-8: Required RF saturation tests

For each test case the TLP I/V characteristic should be recorded and documented in a diagram in the test report. The derived CMC ESD saturation break down voltage should be below the recommended limits given in Appendix B.4.

Appendix A - Test fixtures

A.1 General requirements for test fixtures

A printed circuit board design with RF board-to-coax connectors shall be used for all test fixtures. To ensure reliable RF parameters of the test fixture, a PCB with at least two layers with enlarged GND reference plane is required. The traces on the test board should be designed as 50 (+/- 5) Ohm single ended transmission line with a length as short as possible. For design of CMC footprint and the definition of minimal distance of CMC housing and CMC terminals to the GND plane the related specification of CMC manufacturer have to be meet.

For S-Parameter 3-Port test fixture additional specific requirements are defined in section A.2.

In general the test fixture design and the method of connecting the CMC with the test fixture shall allow high accuracy and reproducible test results.

A.2 Self-balance requirements for S-Parameter test fixture

The 3-Port test fixture (test circuit board with soldered RF connectors) used for balance measurement shall have a very high grade of self-balance.

To prove the test fixture self-balance characteristic of logical port 1 (differential mode), the test parameter and requirements given in Table A-1 are defined.

To ensure the test fixture self-balance characteristic of symmetrical network at logical port 2 (common mode), the traces between the DUT and all resistors (R_1, R_2 and R_3) must kept highly symmetric and as short as possible.

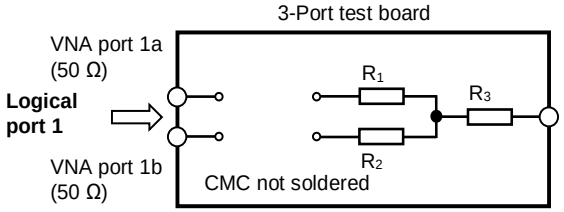
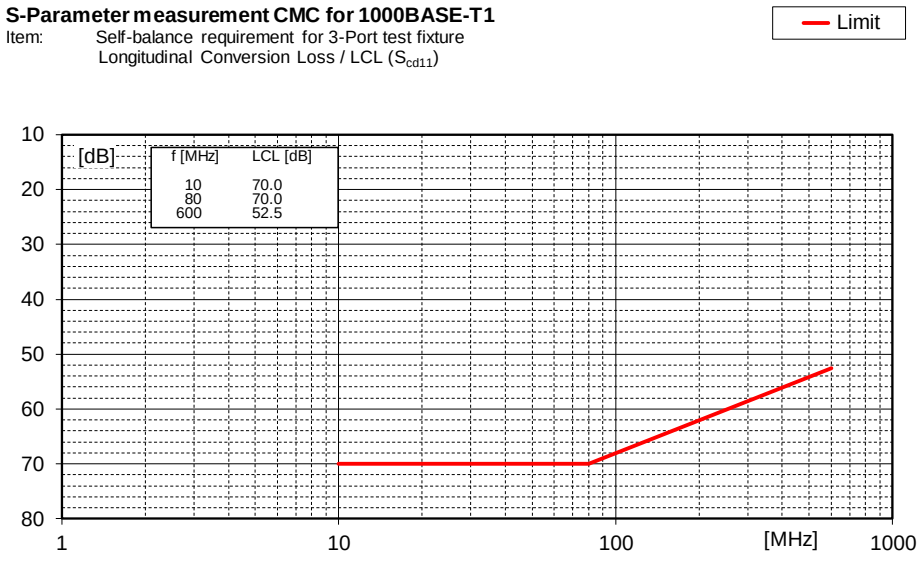
Parameter	Description
Frequency range:	1 MHz to 1 GHz, logarithmic scale
S-Parameter:	S_{dc11} (LCL), log. Magnitude in dB / differential port side of 3-Port test fixture
VNA measurement circuit:	Port definitions: Mixed mode logic port 1: physical port 1a and port 1b Differential mode input (logical port 1): 50 Ω impedance each  $R_1 = R_2 = 49.9\ \Omega$, $R_3 = 124\ \Omega$ Note: The DUT shall be not soldered at the fixture self-balance measurement.
Requirement:	$LCL \geq \begin{pmatrix} 70 & 10 \leq f \leq 80 \\ 70 - 20log\left(\frac{f}{80}\right) & 80 \leq f \leq 600 \end{pmatrix} dB$, frequency f in MHz 

Table A-1: Test parameters and requirements for 3-Port test fixture

A.3 Example of test fixture S-Parameter measurement

The reference points by calibration are the pads of the CMC at the test fixture board.

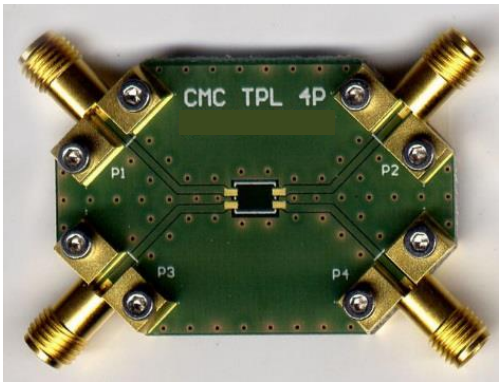


Figure A-1: Example of test fixture for S-Parameter measurement - mixed mode, top layer

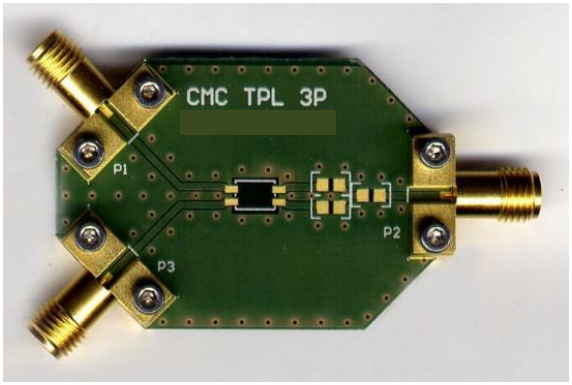


Figure A-2: Example of test fixture for S-Parameter measurement - single ended, top layer

A.4 Example for test fixture ESD damage test

The reference points by calibration are the input of RF connector (SMA) at the test fixture board.

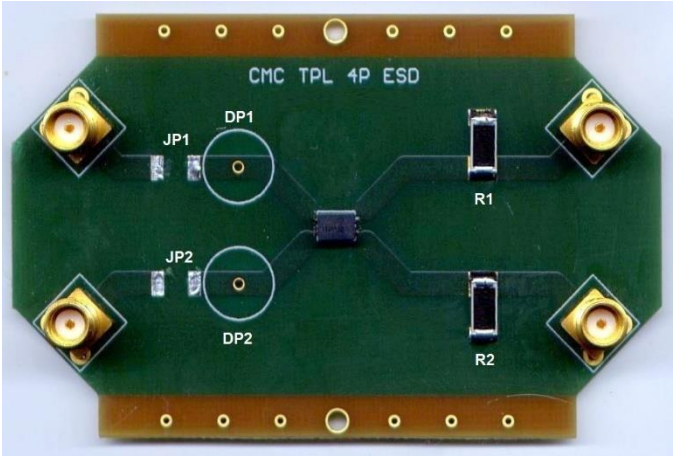


Figure A-3: Example of test fixture for ESD damage test, top layer

Note: For ESD tests the serial jumpers JP1 and JP2 are left open and the resistors R1 and R2 are placed.
For S-Parameter measurement the jumpers JP1 and JP2 are closed and the resistors R1 and R2 are not placed.

A.5 Example for test fixture RF saturation test

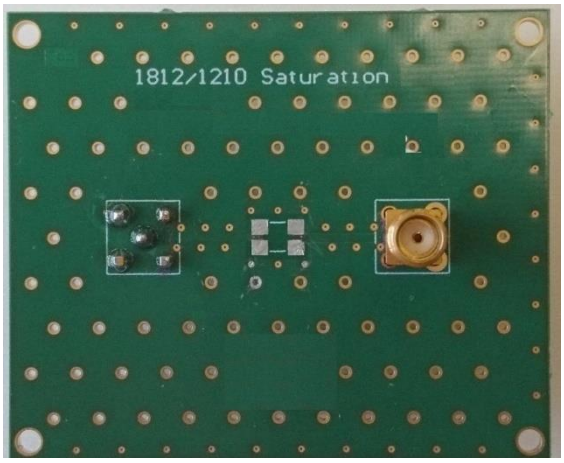


Figure A-4: Example of test fixture for RF saturation test, top layer

A.5 Example for test fixture ESD saturation test

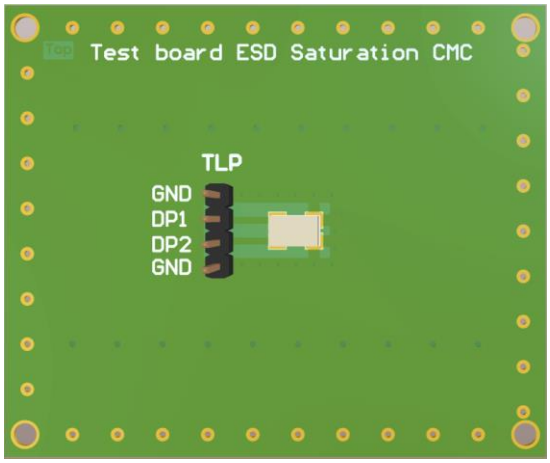


Figure A-5: Example of test fixture for ESD saturation test, top layer

Appendix B – Recommended limits for tests

B.1 S-Parameter measurements

For evaluation of mixed mode S-Parameters two limit classes for each parameter given in Figure B-1 through Figure B-5 are recommended. The limits are valid for test cases S1 through S10.

$$RL \geq \begin{pmatrix} 25 & 10 \leq f \leq 80 \\ 25 - 12log\left(\frac{f}{80}\right) & 80 \leq f \leq 600 \end{pmatrix} dB, \text{ frequency } f \text{ in MHz}$$

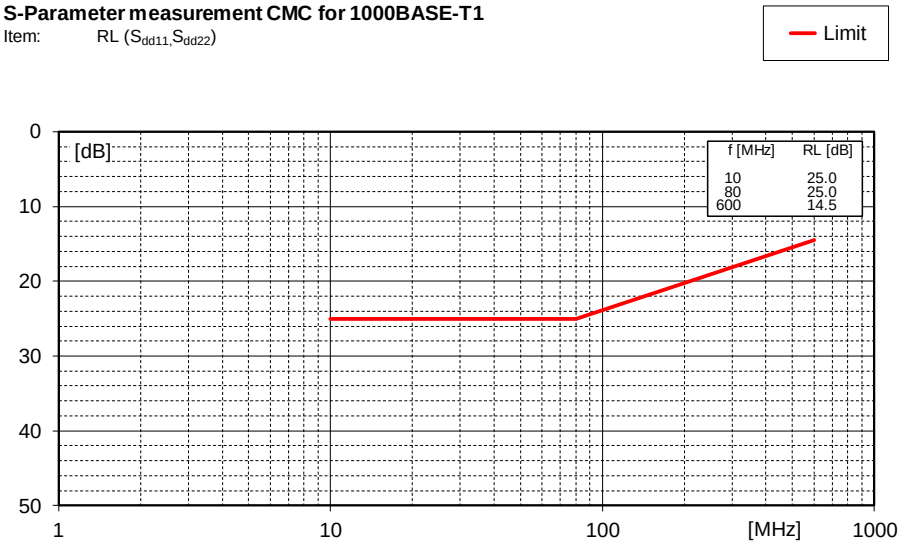


Figure B-1: Recommended limits for S_{dd11} and S_{dd22} (RL)

$$IL \leq \begin{pmatrix} 0.5 & 10 \leq f \leq 20 \\ 0.5 + 0.43log\left(\frac{f}{20}\right) & 20 \leq f \leq 100 \\ 0.8 + 1.163log\left(\frac{f}{100}\right) & 100 \leq f \leq 400 \end{pmatrix} dB, \text{frequency } f \text{ in MHz}$$

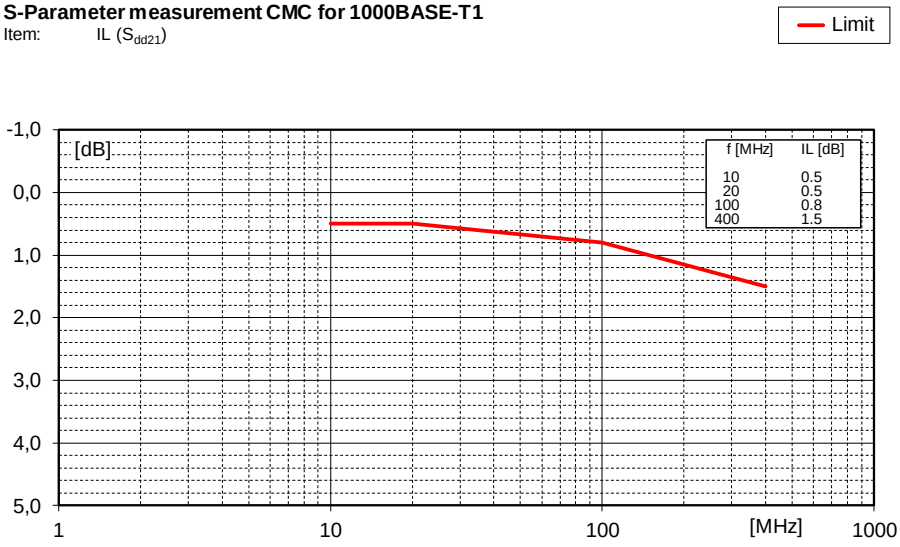


Figure B-2: Recommended limits for S_{dd21} (IL)

$$CMR \geq \begin{pmatrix} 32.5 + 20log\left(\frac{f}{10}\right) & 10 \leq f \leq 30 \\ 42 & 30 \leq f \leq 200 \\ 42 - 20log\left(\frac{f}{200}\right) & 200 \leq f \leq 600 \end{pmatrix} dB, \text{frequency } f \text{ in MHz}$$

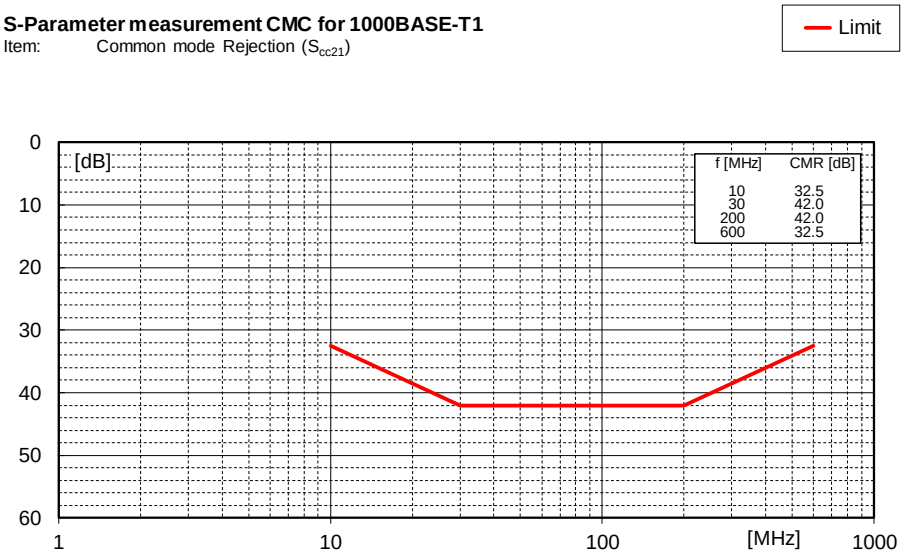


Figure B-3: Recommended limits for S_{cc21} (CMR)

$$LCL \geq \begin{pmatrix} 55 & 10 \leq f \leq 80 \\ 77 - 11.51log\left(\frac{f}{80}\right) & 80 \leq f \leq 600 \end{pmatrix} dB, \text{ frequency } f \text{ in MHz}$$

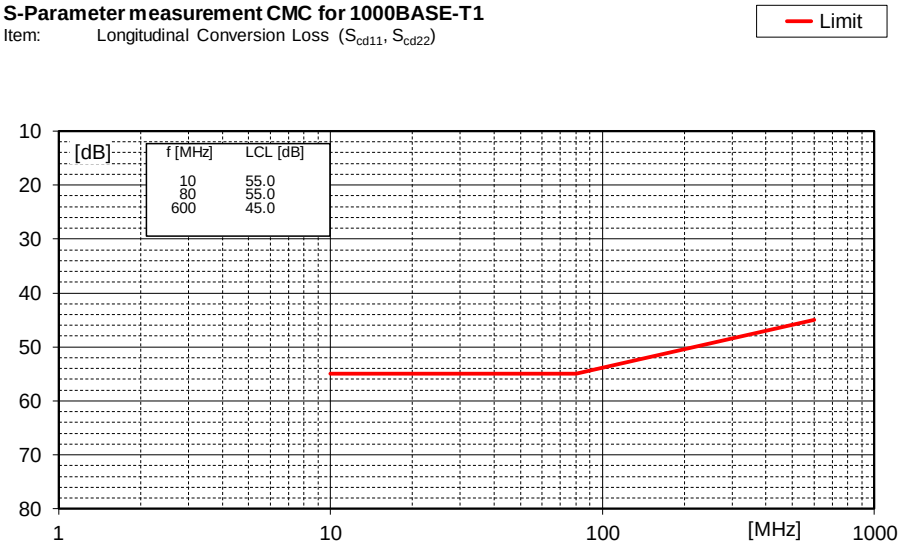


Figure B-4: Recommended limits for S_{cd11} and S_{cd22} (LCL)

$$\begin{matrix} DCMR \\ CDMR \end{matrix} \geq \begin{pmatrix} 65 & 10 \leq f \leq 80 \\ 65 - 20log\left(\frac{f}{80}\right) & 80 \leq f \leq 600 \end{pmatrix} dB, \text{ frequency } f \text{ in MHz}$$

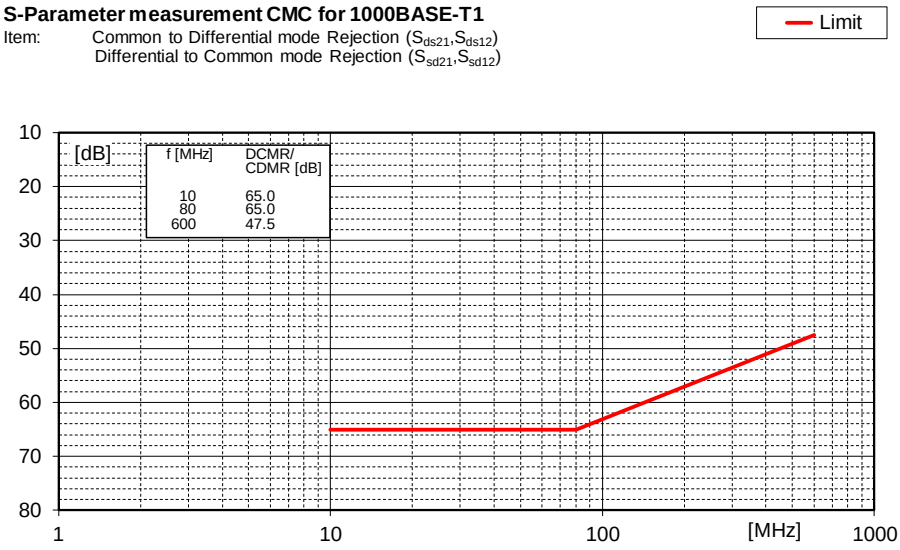


Figure B-5: Recommended limits for S_{sd21}, S_{sd12} (DCMR) and S_{ds21}, S_{ds12} (CDMR)

B.2 Damage from ESD

It is recommended that the CMC must withstand the ESD discharge with discharge voltage amplitude of +/- 8 kV without damage.

B.3 Test of saturation effect at RF immunity tests

It is recommended that the CMC must withstand the RF power saturation test according to the evaluation criteria up to power amplitude of 36 dBm.

B.4 Test of saturation effect at ESD tests

Based on measurement result of TLP I/V characteristic the CMC shall be classified using the definition of Table B-1 and Figure B-6.

Class	V_{ESD_br}
I	50 V to 125 V
II	≥ 125 V

Table B-1: ESD saturation break down voltage classes for CMC

An example of measurement results for typical CMCs is shown in Figure B-6.

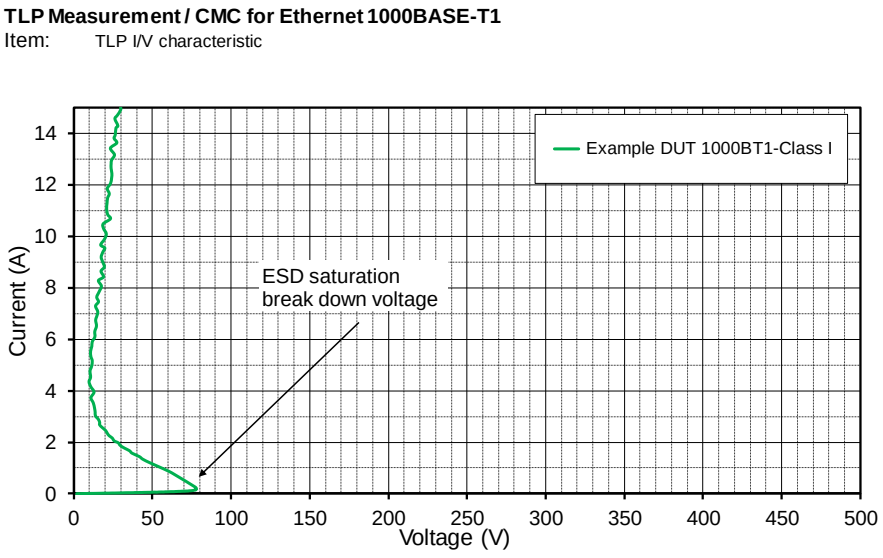


Figure B-6: Example of ESD saturation tests results for CMC

Appendix C – TDR measurement of differential mode impedance (informative)

C.1 Test setup

For measuring the differential mode impedance of the CMC a two-channel TDR test equipment in combination with a special test fixture (adapter test board) shall be used.

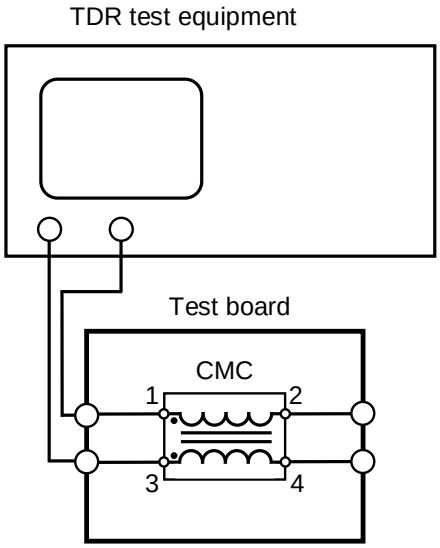


Figure C-1: Test setup for TDR measurements

Test equipment requirements:

TDR measurement system:	Type:	2 channel differential mode
	System impedance:	50 Ω single ended / 100 Ω differential mode
	Rise time:	≤ 25 ps internal (≤ 100 ps at test fixture)
Test fixture:	Use test fixture from 4 port S-Parameter measurements or given example of Figure C-2	

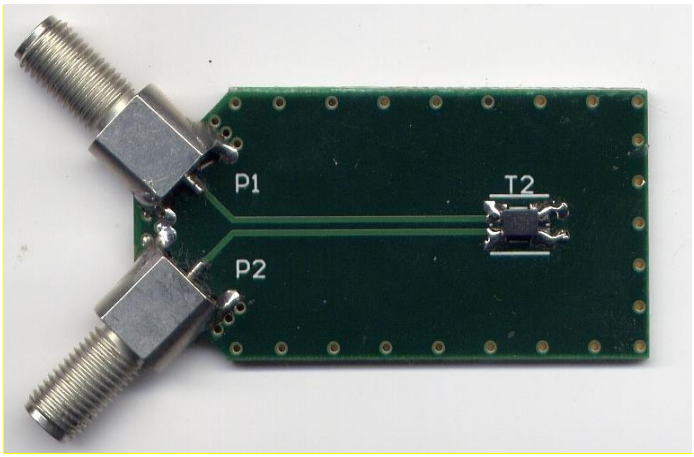


Figure C-2: Example of TDR test board for CMC, top layer

C.2 Test procedure and parameters

The required measurements are defined in Table C-1 and should be done on one sample.

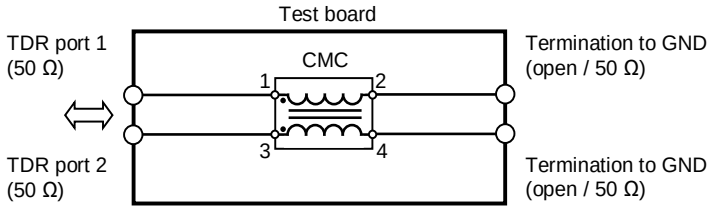
Parameter	Description
TDR measurement circuit:	Definition: Pin 1 of CMC is placed on the transceiver side (TDR measurement port)  Note: The TDR shall be deskewed at the CMC terminals.

Table C-1: Test parameters for TDR measurements

The measurements shall be performed and documented according the scheme given in Table C-2.

Test	Parameter	Sample
T1	Differential mode impedance	1 sample

Table C-2: Required TDR measurements

There is no recommendation for limit. This test is only for information purpose and can be used for additional interpretation of results of S-Parameter measurements.

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