# IEEE 1000BASE-T1 EMC Test Specification for Transceivers

Version 2.1


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**Version Control of Document**

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# Contents

# 1 Introduction

## 1.1 Scope

This EMC measurement specification shall be used as a standardized common scale for EMC evaluation of 1000BASE-T1 transceivers in automotive applications according to [IEEE1]. It contains recommended limits. The final judgment of the tested device is left to the customer.

This specification is not applicable for devices which are intended for use in Power over Ethernet applications.

This specification uses standard EMC test methods for ICs according to [IEC1] to [IEC5] and can be applied for stand-alone transceivers and integrated transceiver cells. In case of devices with an integrated Ethernet transceiver (e.g. SBCs), the test conditions cannot be fixed for each type of IC. Therefore, if it is possible, the test conditions of standard stand-alone transceiver should be used. The configuration of the physical layer of the Ethernet communication system is fixed in any case.

All EMC relevant pins (functions) described in this document shall be tested. If an Ethernet transceiver includes additional product specific EMC relevant pins (functions) it shall be tested as well. The test conditions and failure validation criteria shall be adapted to the definitions for stand-alone Ethernet transceiver.

## 1.2 References

[IEEE1] IEEE Std. 802.3bp

[OPEN1] OPEN ALLIANCE: IEEE 1000BASE-T1 EMC Test Specification for Common Mode Chokes

[OPEN2] OPEN ALLIANCE: Channel and Components Requirements for 1000BASE-T1 Automotive Ethernet

[IEC1] IEC 61967-1, Integrated circuits, Measurement of electromagnetic emissions, 150 kHz to 1 GHz – Part 1: General and definitions

[IEC2] IEC 61967-4, Integrated circuits, Measurement of electromagnetic emissions, 150 kHz to 1 GHz – Part 4: Measurement of conducted emissions – 1 Ω/150 Ω direct coupling method

[IEC3] IEC 62132-1, Integrated circuits, Measurement of electromagnetic immunity, 150 kHz to 1 GHz – Part 1: General and definitions

[IEC4] IEC 62132-4, Integrated circuits, Measurement of electromagnetic immunity, 150 kHz to 1 GHz – Part 4: Direct RF power injection method

[IEC5] IEC62215-3: Integrated circuits – Measurement of impulse immunity, Part 3: Non-synchronous transient injection method

[IEC6] IEC 61000-4-2, Electromagnetic compatibility, Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test

[ISO1] ISO 7637-2, Road vehicles, electrical disturbances by conduction and coupling – Part 2: Vehicles with nominal 12 V or 24 V supply voltage – Electrical transients along supply lines only

## 1.3 List of abbreviations and definitions

AM: Amplitude Modulation

BIN: MDI Test Network

BIST: Built In Self Tests

CMC: Common Mode Choke

CW: Continuous Wave

DPI: Direct Power Injection

DSO: Digital Storage Oscilloscope

DTT: Data Transfer Test

ECU: Electronic Control Unit

Global pin: Pins that can be connected direct or via external passive components to the wiring harness

GMII: Gigabit Media Independent Interface

LPF: Low Pass Filter

MDI: Medium Dependent Interface

MII: Media Independent Interface

MSE: Mean Squared Error

PM: Pulse Modulation

PRBS: Pseudo Random Bit Stream

RGMII: Reduced Gigabit Media Independent Interface

RF: Radio Frequency

RS-FEC: Reed Solomon Forward Error Correction

SBC: System Basis Chip

SGMII: Serial Gigabit Media-Independent Interface

SNR: Signal Noise Ratio

# 2 Test Philosophy

## 2.1 General

Due to the very high communication rate of 1000BASE-T1 and the intended use of unshielded twisted pair cable for automotive applications, a high risk of EMC problems is expected. For this reason, an EMC optimization of all components of the Ethernet physical layer is required. The EMC results are influenced by different aspects:

- Ethernet transceiver software configuration (register settings)
- Ethernet transceiver itself
- MDI test network (BIN)
- layout implementation of transceiver and interface network
- other active ICs that are necessary for Ethernet communication and for function of application device (e.g. µC)
- EMC concept of application device
- symmetry of Ethernet wire and connector
- disturbing transfer function of used test and measuring method.

For EMC tests of a 1000BASE-T1 communication system on ECU level BCI and antenna measurement are usually required test methods. But they are affected by all given aspects in parallel. An advantageous strategy for EMC optimization of the application device is to analyze the influence of each aspect separately.

This EMC measurement specification is focused on the physical layer of the Ethernet interface using standard EMC test methods for ICs. The intent of this specification is:

- a common EMC evaluation of 1000BASE-T1 transceiver for comparison purpose
- checking the EMC behavior of the transceiver in combination with different MDI test networks
- separation of emitted disturbance into disturbing source:
    - MDI pins
    - voltage supplies
    - other digital interfaces (e.g. RGMII or SGMII)
    - clock out signals
- evaluation of EMC behavior for symmetrical and unbalanced disturbances at MDI pins

## 2.2 Tested EMC phenomena

Derived from the EMC requirements at the application layer, tests for the following EMC phenomena are specified:

| EMC phenomena | Transceiver pins | Test method |
|---|---|---|
| RF emission | – MDI<br>– other global pins (e.g. $V_{BAT}$ pin)<br>– local pins such as voltage supply pins | 150 Ohm test method acc. to [IEC2] |
| RF immunity | – MDI<br>– other global pins | DPI test method acc. to [IEC4] |
| Transient immunity | – MDI<br>– other global pins | [ISO1] pulses using [IEC5] |
| ESD immunity | – MDI<br>– other global pins | discharge module according to [IEC6] |

**Table 2-1: Tested EMC phenomena and related test methods**

# 3 Required Tests

## 3.1 RF and transient disturbances

### 3.1.1 General test conditions for RF and transient disturbances

#### *3.1.1.1 Test conditions*

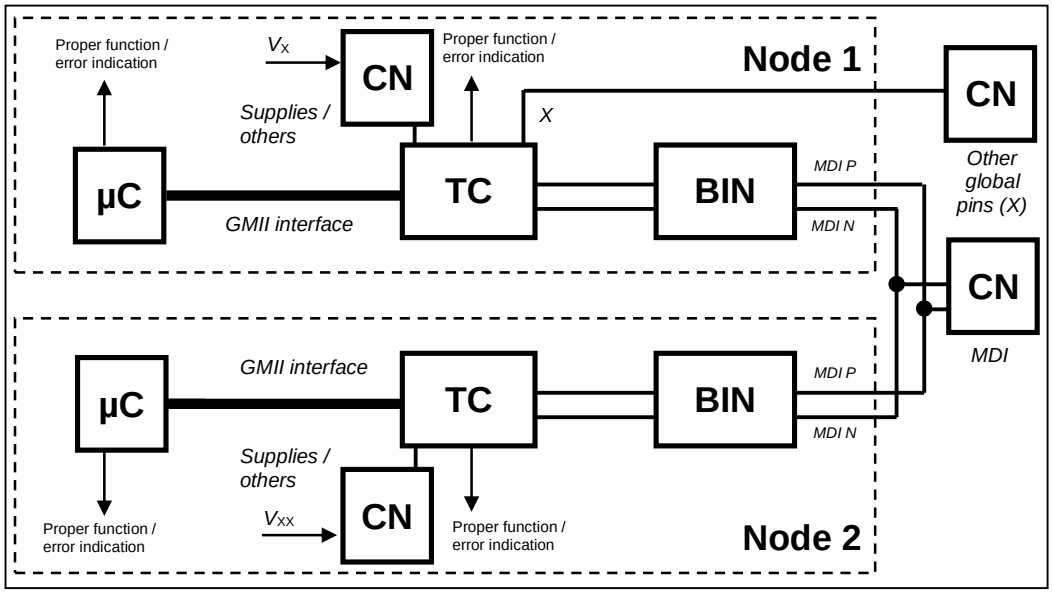
The general test conditions are given below.

| Parameter | Value |
|---|---|
| Battery voltage supply | (14.0 ± 0.2) V |
| Voltage supply, auxiliary supply | ($U_{nom}$ ± 0.1) V |
| Test ambient temperature | (23 ± 5) C |

**Table 3-1: General test conditions**

#### *3.1.1.2 Test configuration*

For testing the EMC behavior (except ESD) of Ethernet transceivers the following node to node network is used.




µC Automotive microcontroller or FPGA with GMII, RGMII and SGMII interface

TC Ethernet transceiver (device under test – DUT)

BIN MDI test network (including DC decoupling, CMC and if used: termination, additional filter elements and ESD protection devices)

CN EMC coupling network

**Figure 3-1: Basic test configuration for RF and transient tests at Ethernet transceiver**

An Ethernet node consists of a microcontroller, the Ethernet transceiver and a MDI test network. Both nodes are equivalently configured to establish a full duplex Ethernet link. The link has one bidirectional connection. This connection is carried out as line impedance controlled PCB traces and not a wire connection.

The microcontroller or FPGA used for this setup implements a GMII interface which is used for configuring and monitoring the Ethernet transceiver and for generating an Ethernet test signal. If common used management interface (MDC, MDIO) is not available on the Ethernet transceiver, another interface (such as SPI) should be used. The µC is EMC decoupled from the tested transceiver (and its EMC coupling networks) using filter networks at voltage supplies and by considering specific layout requirements. A specific software implementation runs on the µC. It must be adapted to the transceiver type, especially for configuration and monitoring.

For Ethernet transceiver that supports RGMII and SGMII interface node 1 should be configured with RGMII and node 2 with SGMII. If only one interface type is implemented both nodes are configured with the same available interface (RGMII or SGMII).

If a multiport device is being evaluated, each port that is intended to be used for wired Ethernet communication must be tested. Doing this, the tested port of node 1 shall be connected with the same port of node 2 (port1 with port 1, port 2 with port 2, …).

The Ethernet transceiver (TC) has a circuitry of external passive components according to the data sheet requirements of the semiconductor manufacturer.

Three different types of MDI test networks (BIN) shall be used for testing:

- Minimum MDI interface network (Min-BIN):
  DC decoupling capacitor Cac1 = Cac2 = 100 nF )$_1$ and a biasing network (if required for operation) as illustrated in Figure 3-2
- Standard MDI interface (S-BIN):
  DC decoupling capacitor Cac1 = Cac2 = 100 nF )$_1$, a biasing network (if required for operation) and a CMC that fulfill the requirements of [OPEN 1] Appendix B.1 as illustrated in Figure 3-3
- Optimized MDI interface (Opt-BIN):
  DC decoupling capacitor Cac1 = Cac2 = 100 nF )$_1$, a biasing network (if required for operation), a CMC that fulfill the requirements of [OPEN 1] Appendix B.1 , a Low pass filter (LPF) and ESD suppression devices or terminations defined by semiconductor manufacturer as illustrated in Figure 3-4. The position of the termination within the interface network can diversity between CMC and Cac1/ Cac2 or between Cac1 and Cac2 and MDI node. The position of ESD suppression devices within the interface network can diversity between transceiver and CMC or between Cac1 and Cac2 and MDI node.

  )$_1$ Cac1 = Cac2 = 100 nF is default value. Other values can be used if required by semiconductor manufacturer.

The S- Parameters $S_{CC21}$, $S_{DD21}$, $S_{DC21}$ and $S_{CD21}$ of CMC samples used during testing shall be measured according to [OPEN 1] and shall be documented in the test report.

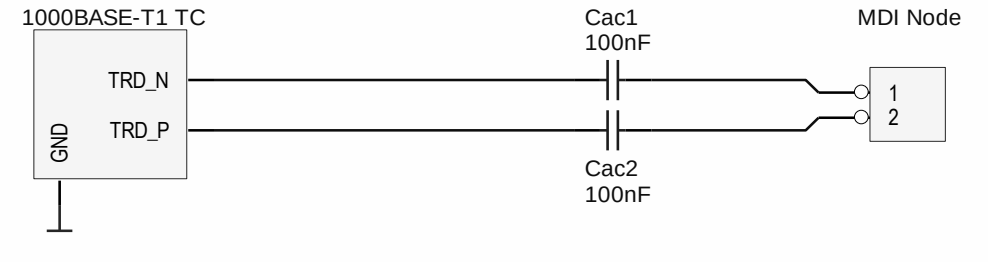



**Figure 3-2: Minimum MDI interface test network (Min-BIN)**

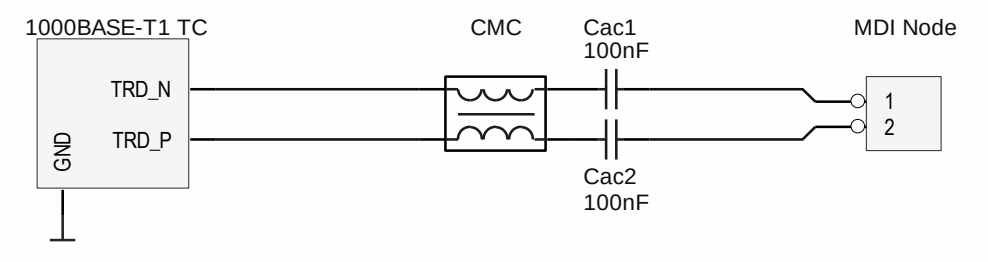



**Figure 3-3: Standard MDI interface test network (S-BIN)**

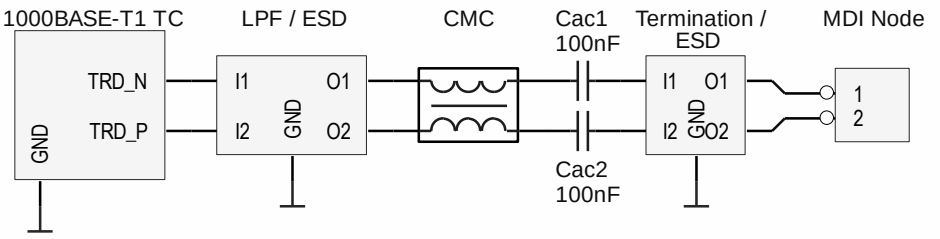



**Figure 3-4: Optimized MDI interface test network (Opt-BIN)**

EMC coupling networks are used for coupling disturbances during immunity testing and for measuring emissions. The EMC coupling network utilized depends on the type of the pin and the test being performed, and is specified in the test configuration section for each test.

In general, all parts of the basic test configuration should be placed on one test circuit board with a minimum of 4 layers. For practical measurement optimization a separation of the test configuration into a universal host µC board and a specific transceiver RF test board is intended. They are connected to each other via a defined enhanced GMII interface according to Figure 3-5. Especially the transceiver RF test

board has to be in line with definitions of [IEC1], [IEC2], [IEC3] and [IEC4]. For more information regarding the test boards see Appendix A.

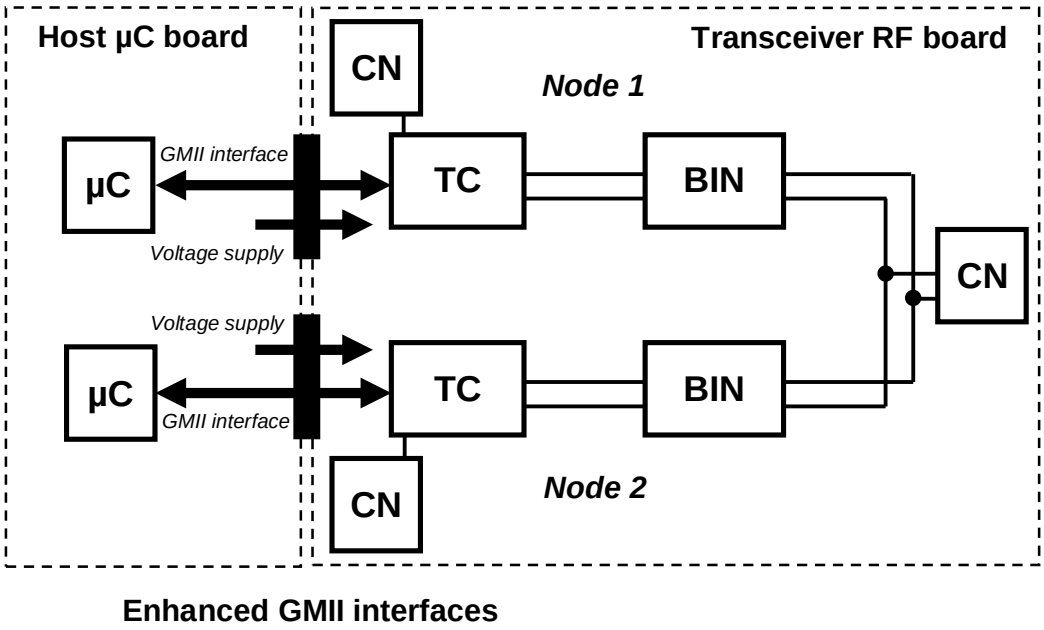



**Figure 3-5: Arrangement of host µC board and transceiver RF test board**

### *3.1.1.3 Definitions for Ethernet test communication and software configuration of transceiver*

The Ethernet test communication signals for 1000 Mbit/s communication rate in full duplex mode are defined as:

| Topic | Content |
|---|---|
| Software | MDI relevant configuration for tests in active mode (normal mode):<br>– 1000BASE-T1 full duplex<br>– Automatic Polarity Detection enabled<br>– Driver strength maximum - default (if configurable)<br>– Transceiver configuration specified by semiconductor manufacturer )$_1$ (to be documented in the test report)<br>– Data frame transmission initiate by host controller<br>o Protocol type TCP/IP 0x800<br>o packet size minimum 1014 bytes<br>o cycle time 25µs (minimum 20 % bus load)<br>o payload data 0x5A<br>– Data frame transmission initiate by 1000BASE-T1 transceiver itself<br>o Activation of internal BIST or PRBS test with maximum possible performance<br>MDI relevant configuration for tests in low power mode (sleep or standby mode):<br>– Transceiver configuration as specified by semiconductor manufacturer )$_1$ (to be documented at test report)<br>MII relevant configuration:<br>– Transceiver configuration as specified by semiconductor manufacturer )$_1$<br>– (e.g. GMII driver strength, to be documented at test report)<br><br>Note 1: )$_1$: Configuration as specified by semiconductor manufacturer in datasheet, application note or comparable documentation. |

**Table 3-2: Definition for software configuration**

For additional tests, especially in combination with optimized BIN, other configurations for reduction of emission or improvement of immunity can be used. For all combinations tested, Ethernet communication must be possible over 15 m of UTP cable and 4 standard inline connectors in the absence of disturbers. The transceiver configuration data necessary for standard and, if used, for EMC optimized configuration must be supplied by the semiconductor manufacturer. It must be documented in detail (register write data and order of writing) in the test report.

#### *3.1.1.4 Evaluation of system immunity*

A malfunction test and a damage test are required to evaluate system immunity. The malfunction test examines function status class A while the damage test examines function status classes C and D (see Table 3-3).

##### 3.1.1.4.1 Malfunction test

A malfunction test is required to be performed after a link is established between two test transceivers (normal mode) or the transceivers are set into low power mode, if available. The following criteria will be evaluated:

- Evaluation during immunity tests for tests in normal mode (I-n)
  - read out of all available error registers for the transceiver. At a minimum the register information for Link error and CRC error should be examined.
    Note 1: If no read out of required error registers at the transceiver is possible, the error validation shall be implemented into the microcontroller software in comparable way.
  - Data Transfer Test
    - For data frame transmission initiate by host controller: Data Transfer Test (DTT) error detection by microcontroller software application (checking of all transferred data between the two nodes of the test network)
    - For Data frame transmission initiate by 1000BASE-T1 transceiver itself: error check for BIST or PRBS test
  - If available for tested transceiver, read out and documentation of all available registers for indication of SNR value (e.g. signal quality indicator or MSE value)
    Note 2: This data should be used for information only. Actually there is no immunity requirement with limit is defined.
  - If available for tested transceiver, read out and documentation of available registers for indication of RS-FEC events
    Note 2: This data should be used for information only. Actually there is no immunity requirement with limit is defined.
- Evaluation during immunity tests for tests in low power mode (I-lp)
  - Check indication for wakeup
- Evaluation after immunity tests for tests in normal mode (II-n)
  - Read out of transceiver configuration registers and comparison with initial state

##### 3.1.1.4.2 Damage test

A damage test related to functional status class D means that one or more functions of a transceiver do not perform as designed during exposure and do not return to normal operation until exposure is removed and the transceiver is reset by simple "operator/use" action (e.g. restart by GMII interface). No physical damage of transceiver occurs.

The following evaluation criteria have to be used for detection of a physical damage:

- Evaluation criterion 1: Evaluation of current consumption at voltage supply input(s) of tested transceiver after damage test. Any change of more than ± 5 % of the initial value indicates a damage of the tested pin.
- Evaluation criterion 2: Evaluation of functionality of tested transceiver after damage test and reset by simple "operator/use", if necessary.
- Evaluation criterion 3: The characteristic curve of pin voltage versus pin current of the tested pin to GND pin must be measured using a Semiconductor Parameter Analyzer. If possible the maximum current and voltage level used for characteristic curve measurement should be indicating the break down voltage of the internal ESD structure. Commonly used voltages are ± (50 to 70) V and ± (0.5 to 5) mA. Any change of more than ± 5 % of the maximum used voltage or current indicates a damage of the tested pin.

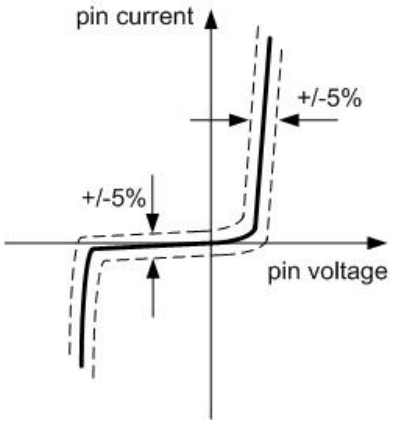



**Figure 3-6: Example for maximum deviation definition at characteristic curve measurement**

#### 3.1.1.4.4 Resulting status classes

The test results shall be related to function status class A or C using the definitions of Table 4.

| Resulting status class | Comment |
|---|---|
| A | – no error occurred during exposure (I-n / I-lp) |
| A1 | – no Link error occurred during exposure |
| A2 | – no CRC error and DDT error occurred during exposure |
| A3 | – no unwanted wake-up caused by ESD discharges during exposure, proper wake-up functionality and correct change into normal mode on request during exposure |
| C | – error occurred during exposure (I-n)<br>– no error after exposure (A)<br>– no change of internal transceiver configuration (II)<br>– system comes back into proper operation automatically |
| D | – error occurred during exposure (I-n)<br>– error occurred after exposure (I-n) or change of internal transceiver configuration (II)<br>– system does not come back into proper operation automatically until exposure is removed and the transceiver is reset by simple "operator/use" action (e.g. power off/on)<br>– no physical damage of IC occurs (according to section 3.1.1.4.2) |

**Table 3-3: Definition for immunity status classes**

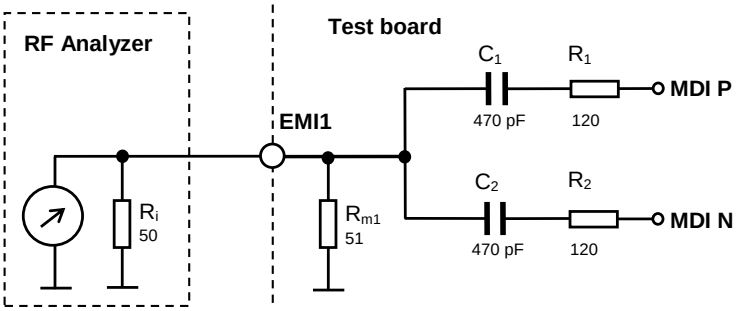
The failure validation applies to both transceivers of the node to node test network. As soon as at least one transceiver in the network fulfils the fault criteria, the error event for this test has occurred.

### 3.1.2 Emission of RF disturbances

#### *3.1.2.1 Test configuration*

For measuring RF emissions the basic test configuration given in Figure 3-1 is used. The EMC coupling networks are defined for the 150 Ohm RF voltage measurement at the MDI, voltage supply pins and other global pins.

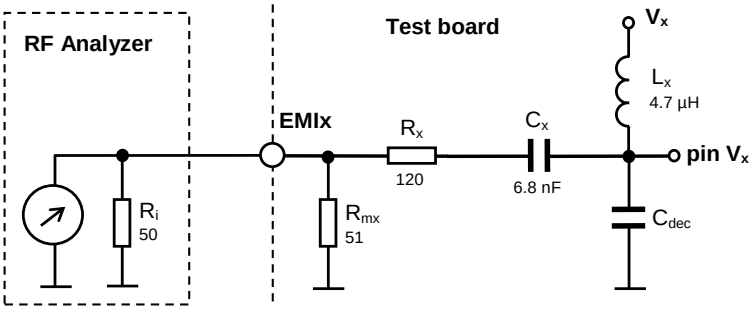
For each Ethernet link a symmetrical measuring network given in Figure 3-7 is used. The difference between symmetrical passive components $C_1$ and $C_2$ as well as $R_1$ and $R_2$ must be less than or equal to 0.1 %, which can be confirmed by measurement.




Comment: The resistors $R_{1(2)}$ (120 Ω) in series with [$R_{m1}$ (51 Ω) parallel to $R_i$ (50 Ω)] and in combination with capacitors $C_{1(2)}$ represent the 150 Ohm RF voltage measurement network.

**Figure 3-7: RF emission measuring network for Ethernet link**

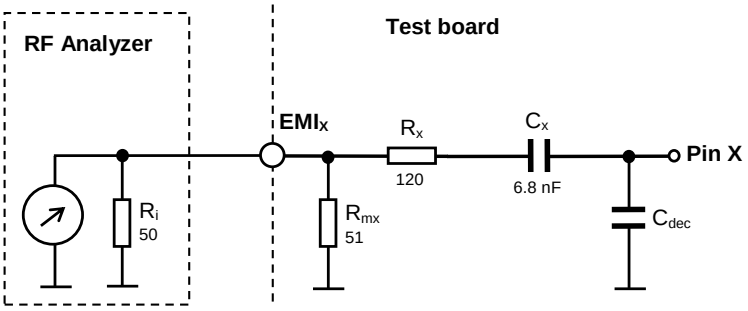
The emission at each voltage supply pin of the transceiver, which is connected to the application device voltage supply, must be measured using the network given in Figure 3-8. The central voltage $V_x$ ($V_x$ represents different possible voltage supply domains) is RF decoupled from the transceiver pin with an inductor $L_x$ = 4.7 µH. The decoupling capacitor $C_{dec}$ or multi-stage filter – according to data sheet definitions – is placed directly at the transceiver pin.




Comment: The resistor $R_x$ (120 Ω) in series with [$R_{mx}$ (51 Ω) parallel to $R_i$ (50 Ω)] and in combination with capacitor $C_x$ represent the 150 Ohm RF voltage measurement network.

**Figure 3-8: RF emission measuring network for voltage supply pins**

The emission at other global pins of the transceiver, which can be connected to wiring harness, must be measured using the network given in Figure 3-9. The decoupling capacitor $C_{dec}$ or multi-stage filter – according to data sheet definitions – is placed directly at the transceiver pin.




Comment: The resistor $R_x$ (120 Ω) in series with [$R_{mx}$ (51 Ω) parallel to $R_i$ (50 Ω)] and in combination with capacitor $C_x$ represent the 150 Ohm RF voltage measurement network.

**Figure 3-9: RF emission measuring network for other global pins**

### *3.1.2.2 Test setup*

The measurement of the RF disturbances emission of the transceiver should be carried out according to Figure 3-10 in the frequency domain according to [IEC1] and [IEC2].

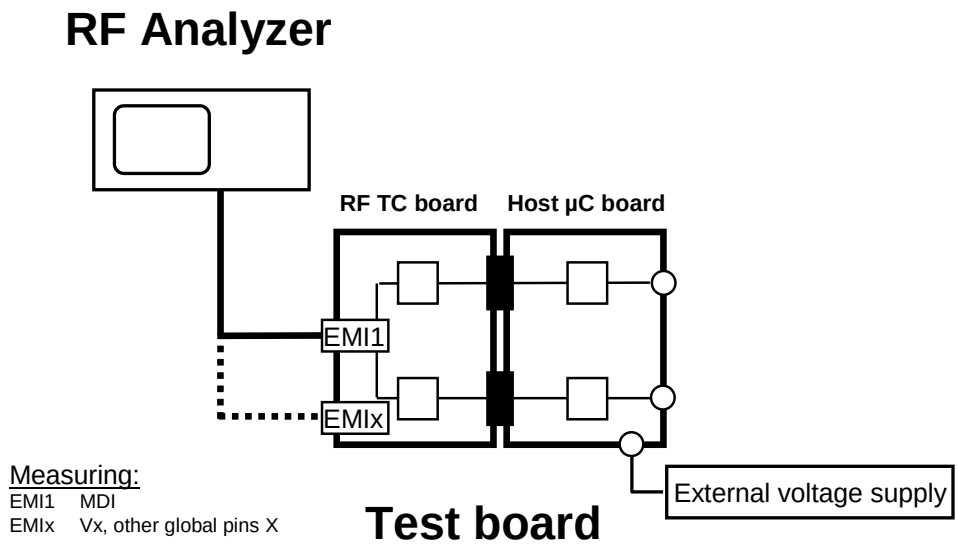



**Figure 3-10: Test setup for measurement of RF disturbances**

Test equipment requirements:

| | |
|---|---|
| RF Analyzer: | Spectrum analyzer or measuring receiver according to [IEC1] |
| Test board: | according to Appendix A |
| External voltage supply | |

The insertion losses (S21 measurement) of the respective transceiver signal pad to the ports EMI1 through EMIx of the test board (without transceiver) shall be measured and documented in the test report.

### *3.1.2.3 Test procedure and parameters*

For characterization of the emission the following test parameters listed in Table 3-4 shall be applied. The results shall be presented as a diagram in the test report.

| **Mode** | **Coupling** | | | |
|---|---|---|---|---|
| | **Port** | **Pin** | **MDI test network (BIN)** | **Parameter coupling** |
| normal mode / with Ethernet test communication (and/or activated PRBS test or BIST) ? | EMI1 | MDI P / N | minimum | symmetric |
| | | | standard | symmetric |
| | | | | +/- 1.25 % unbalance )$_1$ |
| | | | | +/- 2.5 % unbalance )$_1$ |
| | | | optimized | Symmetric |
| | | | | +/- 1.25 % unbalance )$_1$ |
| | | | | +/- 2.5 % unbalance )$_1$ |
| | EMIx | voltage supplies $V_x$ at node configured with RGMII | optimized | pin circuit according to data sheet or application hints |
| | | voltage supplies $V_x$ at node configured with SGMII | | |
| | EMIx | other global pins at node configured with RGMII | optimized | pin circuit according to data sheet or application hints |

)$_1$ To adjust the unbalance of coupling, the resistance values of the two coupling resistors $R_1$ and $R_2$ shall be changed according to Table 3-5.

**Table 3-4: Required emission measurements**

| | R1 [Ω] (MDI P) | R2 [Ω] (MDI N) |
|---|---|---|
| Symmetry | 120 | 120 |
| + 1.25 % unbalance | 121 | 119.5 |
| - 1.25 % unbalance | 119.5 | 121 |
| + 2.5 % unbalance | 121 | 118 |
| - 2.5 % unbalance | 118 | 121 |

**Table 3-5: Combination of resistors for tests at MDI pins**

The settings of the spectrum analyzer or measuring receivers are given in Table 3-6.

| Measuring equipment | Spectrum analyzer | Measuring receiver |
|---|---|---|
| Measurement unit | dBµV | |
| Detector | Peak | |
| Frequency range | 0.15 to 2750 MHz | |
| Resolution bandwidth (RBW)<br>150 kHz to 30 MHz:<br>30 MHz to 2750 MHz: | <br>10 kHz<br>100 kHz | <br>9 kHz<br>120 kHz |
| Video bandwidth (VBW) | > 3 x RBW | - |
| Numbers of passes | 10 (max hold) | 1 |
| Measurement time per step | - | ≥ 1 ms |
| Frequency sweep time | ≥ 20 s | - |
| Frequency step width | - | ≤ 0.4 x RBW |

**Table 3-6: Settings for measurement device**

Recommended limits for evaluation are given in Appendix C.1.

### 3.1.3 Immunity to RF disturbances

#### *3.1.3.1 Test configuration*

For testing the RF immunity of the MDI interface the basic test configuration given in Figure 3-1 is used. The EMC coupling network for the DPI test method are defined at MDI and other global pins.

The symmetrical coupling network given in Figure 3-11 is used when testing the Ethernet link. The difference between symmetrical passive components $C_1$ and $C_2$ as well as $R_1$ and $R_2$ must be less than or equal to 0.1 %, which can be confirmed by measurement.

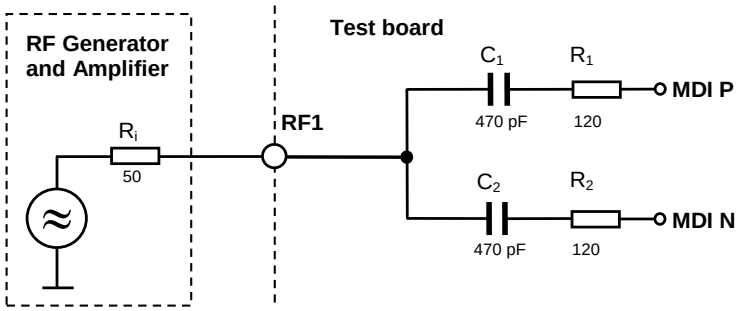



**Figure 3-11: DPI test network for Ethernet link**

The coupling network shown in Figure 3-12 is used when testing RF immunity of other global pins of the transceiver. The decoupling capacitor $C_{dec}$ or multi-stage filter – according to data sheet definitions – is placed directly at the transceiver pin.

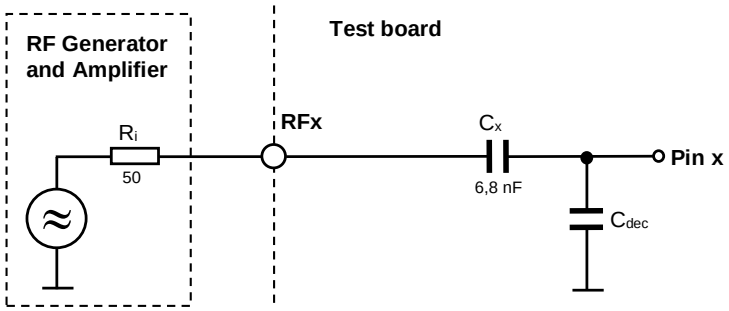



**Figure 3-12: DPI test network for other global pins**

#### *3.1.3.2 Test setup*

For testing the RF immunity of the transceiver using the DPI test method according to [IEC3] and [IEC4] the test setup given in Figure 3-13 is used.

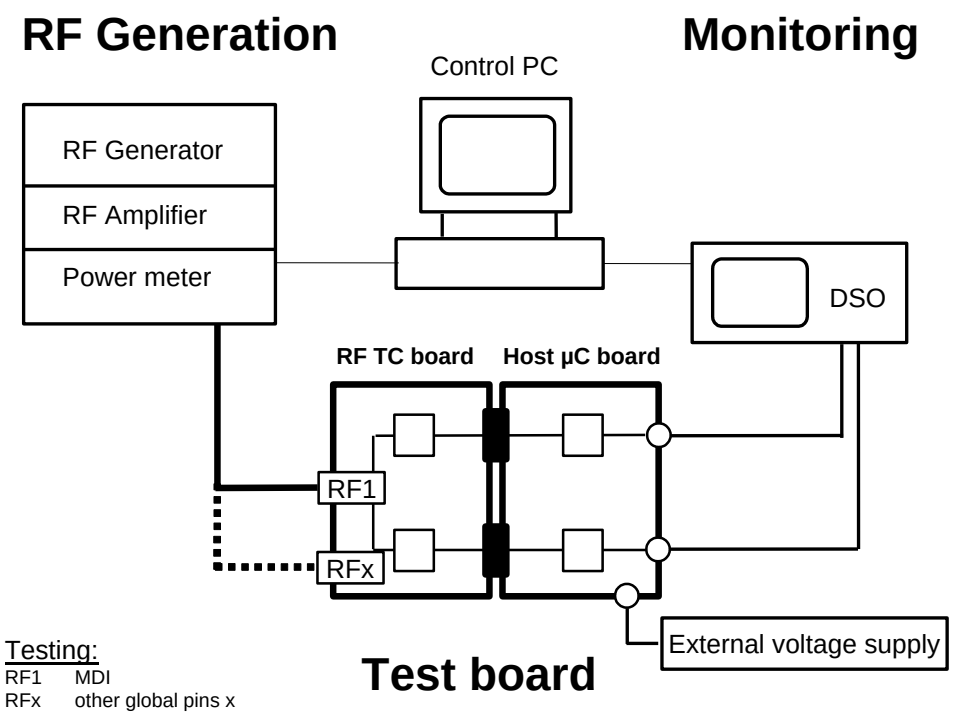



**Figure 3-13: Test setup for RF immunity testing**

Test equipment requirements:

| | |
|---|---|
| RF Generator: | f = 1 MHz – 1000 MHz, modulation AM and PM |
| RF Amplifier: | $P_{CW} \geq 10$ W |
| RF Power meter with directional coupler: | f = 1 MHz - 2000 MHz |
| Test board: | according to Appendix A |
| DSO | |
| External voltage supply | |
| Control PC | |
| Semiconductor parameter analyzer: | used for I/V measurement after damage test |

The insertion losses ($S_{21}$ measurement) of ports RF1 through RFx to the respective transceiver signal pad of the test board (without transceiver) shall be measured and documented in the test report.

### *3.1.3.3 Test parameters*

To determine the immunity of the transceiver against narrow-band disturbances (defined in [IEC3]) tests with the test parameters given in Table 3-7 shall be carried out.

| | **Parameters** | |
|---|---|---|
| Frequency [MHz] | Range | Step |
| | 1 to 10 | 0.25 |
| | 10 to 100 | 1 |
| | 100 to 200 | 2 |
| | 200 to 400 | 4 |
| | 400 to 2000 | 10 |
| Presentation of immunity | Immunity threshold curve with forward power as the parameter | |
| Minimum forward power | 10 dBm | |
| Maximum forward power | 36 dBm in general (39 dBm for MDI with S-BIN and Opt-BIN) | |
| Power step size | 0.5 dB | |
| Power control procedure | Searching for malfunction while power is increased. A combined control procedure to reduce the measurement time can be used.<br>Example procedure for each frequency:<br>1. Start with maximum forward power or with the power of immunity for the last frequency<br>2. Test with half power in each case of malfunction but don't use power level below the minimum forward power<br>3. increase the power by power step size to malfunction | |
| Dwell time | 1 s | |
| Modulation | f = 1 MHz to 1000 MHz: CW<br>f = 1 MHz to 800 MHz: AM 80 %, 1 kHz )$_1$<br>f = 800 MHz to 2000 MHz: PM 217Hz, ton 577µs )$_1$ | |

)$_1$ use peak conversation for the forward power ( $\hat{P}_{Modulation} = \hat{P}_{CW}$ ) according to [IEC3]

**Table 3-7: Test parameters for DPI tests**

### *3.1.3.5 Test procedure*

#### 3.1.3.5.1 Malfunction test

The malfunction tests (function status class A) are to be carried out and documented according to the scheme given in Table 3-8.

| Mode | Coupling | | | | Failure validation class A Error / Function | | | |
|---|---|---|---|---|---|---|---|---|
| | Port | Pin | MDI test network (BIN) | Parameter coupling | CRC / Link / DTT | SNR indication )7 | Sum)4 | Wake up |
| normal mode / with Ethernet test communi-cation | RF1 | MDI P / N | minimum )2 | symmetric | | | X | |
| | | | standard )3 | symmetric | | | X | |
| | | | | +/- 1.25% unbalance )1 | | | X | |
| | | | | +/- 2.5% unbalance )1 | X / X / X | | X | |
| | | | optimized )3 | symmetric | | X | X | |
| | | | | +/- 1.25% unbalance )1 | | X | X | |
| | | | | +/- 2.5% unbalance )1 | | | X | |
| | RFx | other global pins | standard or optimized)2 | pin circuit according to data sheet or application hints | | | X | |
| low power mode / test of wanted wakeup )5,6 | RF1 | MDI P / N | minimum )2 | symmetric | | | | X |
| | | | standard )3 | symmetric | | | | X |
| | | | | +/- 1.25% unbalance )1 | | | | X |
| | | | | +/- 2.5% unbalance )1 | | | | X |
| | | | optimized )3 | symmetric | | | | X |
| | | | | +/- 1.25% unbalance )1 | | | | X |
| | | | | +/- 2.5% unbalance )1 | | | | X |
| low power mode / test of unwanted wakeup )5 | RF1 | MDI P / N | minimum )2 | symmetric | | | | X |
| | | | standard )3 | symmetric | | | | X |
| | | | | +/- 1.25% unbalance )1 | | | | X |
| | | | | +/- 2.5% unbalance )1 | | | | X |
| | | | optimized )3 | symmetric | | | | X |
| | | | | +/- 1.25% unbalance )1 | | | | X |
| | | | | +/- 2.5% unbalance )1 | | | | X |

X A test shall be performed.

)1 To adjust the unbalance of coupling the resistance values of the two coupling resistors R1 and R2 shall be changed according to Table 3-5.

)2 Test shall be done with CW and modulation (AM, PM), maximum test power 36 dBm.

)3 Test shall be done only with modulation (AM, PM), maximum test power 39 dBm.

)4 Sum error: CRC, Link and DTT evaluated in parallel.

)5 Test to wanted or unwanted wake up or Ethernet signal activity detection, depending on implemented function.

)6 One node is set to low power mode, second node sends periodically signal to be detected as wakeup by node in low power mode.

)7 Documentation of SNR value (e.g. signal quality indicator or MSE value), if implemented. Test should be done for information only. There is no immunity limit defined.

**Table 3-8: Required DPI tests for malfunction test**

For each test an immunity threshold curve with the forward power as the parameter has to be carried out and has to be presented in the test report in a diagram.

Recommended limits for evaluation are given in Appendix C.2.

#### 3.1.3.5.2 Damage test

The damage tests are to be carried out and documented according to the scheme given in Table 3-9. The fault criteria are evaluated after each single test. All tests shall be done only with modulation (AM, PM).

| **Mode** | **Coupling** | | | | **Failure validation class** |
|---|---|---|---|---|---|
| | **Port** | **Pin** | **MDI test network (BIN)** | **Parameter coupling** | |
| normal mode / with Ethernet test communi-cation | RF1 | MDI P / N | standard or optimized | symmetric | C or D must be stated as test result |
| | RFx | other global pins | standard or optimized | pin circuit according to data sheet or application hints | |

**Table 3-9: Required DPI tests for damage test**

Recommended limits are given in Appendix C.2.

### 3.1.4 Immunity to transients

#### *3.1.4.1 Test configuration*

For testing the immunity against transients at the MDI interface the basic test configuration given in Figure 3-1 is used. The EMC coupling networks are defined for the direct capacitive coupling (DCC) defined at MDI and other global pins.

The symmetrical coupling network given in Figure 3-14 is used when testing the Ethernet link. The difference between symmetrical passive components $C_1$ and $C_2$ as well as $R_1$ and $R_2$ must be less than or equal to 0.1 %, which can be confirmed by measurement.

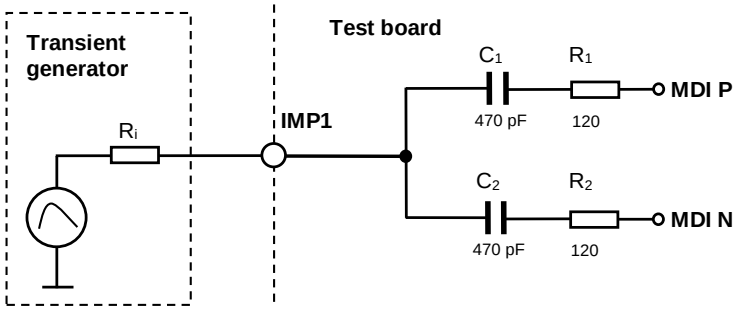



**Figure 3-14: Transient test network for Ethernet link**

The coupling network shown in Figure 3-15 is used when testing transient immunity of other global pins of the transceiver. The decoupling capacitor $C_{dec}$ or multi-stage filter – according to data sheet definitions – is placed directly at the transceiver pin. If coupling to VBAT pin, the coupling capacitor $C_x$ has to be replaced by a reverse protection diode.

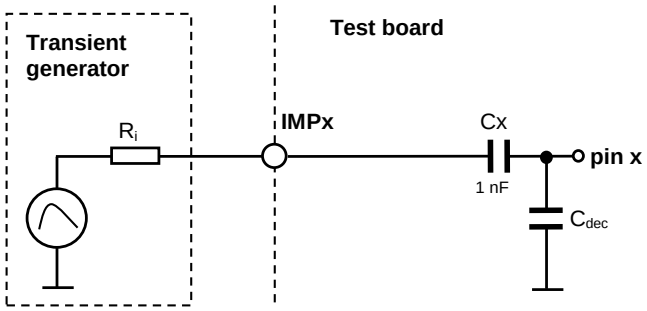



**Figure 3-15: Transient test network for other global pins**

### *3.1.4.2 Test setup*

For testing the transient immunity of the transceiver using the DCC test method according to [IEC5] the test set-up given in Figure 3-16 is used.

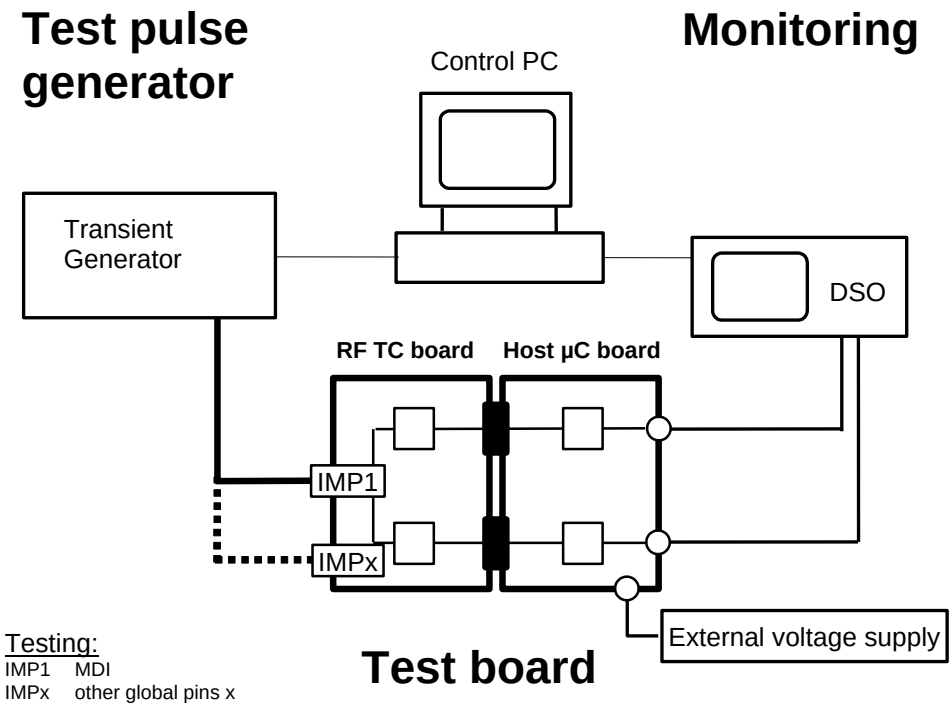



**Figure 3-16: Test setup for transient immunity testing**

Test equipment requirements:

| | |
|---|---|
| Test pulse generator: | according to [ISO1] |
| Test board: | according to Appendix A |
| DSO | |
| External voltage supply | |
| Control PC | |
| Semiconductor parameter analyzer: | used for I/V measurement after damage test |

### *3.1.4.3 Test parameters*

To prove transceiver immunity against transient tests with standard pulses (defined in [ISO1]) tests with parameters given in Table 12 shall be carried out.

| Test pulse )1 | Pulse repetition frequency [Hz] (1/T1 )1) | Test duration )3 [s] | Ri [Ω] | Remarks |
|---|---|---|---|---|
| 1)2 | 2 | 600 / 60 / 5 | 10 | Battery shall be off only during the pulse |
| 2a | 2 | | 2 | |
| 3a | 10000 | | 50 | |
| 3b | 10000 | | 50 | |

)1 according to [ISO1]

)2 parameters for 12 V-Systems

)3 600 s for damage test, 60 s for malfunction test result validation (maximum achieved test level), 5 s for malfunction test at every voltage step

**Table 3-10: Parameters for transient malfunction and damage test**

As a test result, the respective peak voltage values of each standard pulse (see [ISO1]) shall be documented for the immunity of the Ethernet system. The maximum test values are given in Table 3-11.

| Test pulse | Vs [V] |
|---|---|
| 1 | - 100 |
| 2a | + 75 |
| 3a | - 150 |
| 3b | + 100 |

**Table 3-11: Maximum test voltages for transient malfunction and damage test**

For malfunction tests, the amplitudes of the standard impulses shall be increased up to the malfunction or up to the respective maximum test voltage is reached with an increment of 10 V. For every voltage level, a minimum dwell time of 5 s is required. The maximum voltage level for the immunity achieved in this case shall be proven with a dwell time of 60 s.

For damage test, the test amplitude shall applied 600 s for each test case.

### *3.1.4.4 Test procedure*

#### 3.1.4.4.1 Malfunction test

The malfunction tests (function status class A) are to be carried out and documented according to the scheme given in Table 3-12.

| Mode | Coupling | | | | Failure validation class A Error / Function | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Port | Pin | MDI test network (BIN) | Parameter coupling | CRC | Link | DTT | Sum)$_1$ | Wake up |
| normal mode / with Ethernet test communi-cation | IMP1 | MDI P / N | minimum | symmetric | | | | X | |
| | | | standard | symmetric | X | X | X | X | |
| | | | optimized | symmetric | | | | X | |
| | IMPx | other global pins | standard or optimized | pin circuit according to data sheet or application hints | | | | X | |
| low power mode / test of wanted wakeup )$_{2,3}$ | IMP1 | MDI P / N | minimum | symmetric | | | | | X |
| | | | standard | symmetric | | | | | X |
| | | | optimized | symmetric | | | | | X |
| low power mode / test of unwanted wakeup )$_{2,3}$ | IMP1 | MDI P / N | minimum | symmetric | | | | | X |
| | | | standard | symmetric | | | | | X |
| | | | optimized | symmetric | | | | | X |

X A test shall be performed.

)$_1$ Sum error: CRC, Link and DTT evaluated in parallel

)$_2$ Test to wanted or unwanted wake up or Ethernet signal activity detection, depending on implemented function

)$_3$ One node is set to low power mode, second node sends periodically signal to be detected as wakeup by node in low power mode.

**Table 3-12: Required transient tests for malfunction test**

For malfunction tests, no limits are recommended. The results are only for information purpose.

#### 3.1.4.4.2 Damage test

The damage tests are to be carried out and documented according to the scheme given in Table 3-13. The fault criteria are evaluated after each single test.

| Mode | Coupling | | | | Failure validation class |
|---|---|---|---|---|---|
| | Port | Pin | MDI test network (BIN) | Parameter coupling | |
| normal mode / with Ethernet test communi-cation | IMP1 | MDI P / N | standard or optimized | symmetric | C or D must be stated as test result |
| | IMPx | other global pins | standard or optimized | pin circuit according to data sheet or application hints | |

**Table 3-13: Required transient tests for damage test**

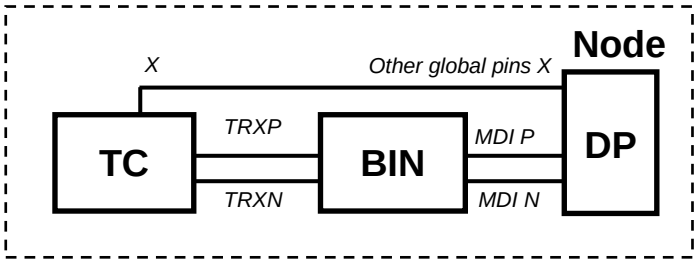
Recommended limits are given in Appendix C.3.

## 3.2 ESD

### 3.2.1 Unpowered ESD test

#### *3.2.1.1 Test configuration*

For testing the immunity of the unpowered transceiver against ESD, a damage test of the MDI pins and other global pins is required. The basic test configuration is given in Figure 3-17.




TC Ethernet transceiver (device under test – DUT)

BIN MDI test network (including CMC, termination, additional filter elements, ESD protection)

DP Direct ESD discharge points

**Figure 3-17: Basic test configuration for ESD tests at unpowered Ethernet transceiver**

For the transceiver and MDI test network the same definitions are valid as stated for RF and transient testing (see section 3.1.1.2). For evaluation of damage to the transceiver a functional test and a measurement of the I/V characteristic curve of the tested pin to GND are performed after applying each ESD discharge. The ESD coupling shall be implemented in a direct galvanic way by using a contact discharge module according to [IEC6] (C = 150 pF, R = 330 Ω). For this purpose, the discharge points DP – carried out as rounded vias in the layout of the ESD test board – are directly connected by a traces with a length between 25 mm and 30 mm to the MDI test network or other global pins according to Figure 3-18.

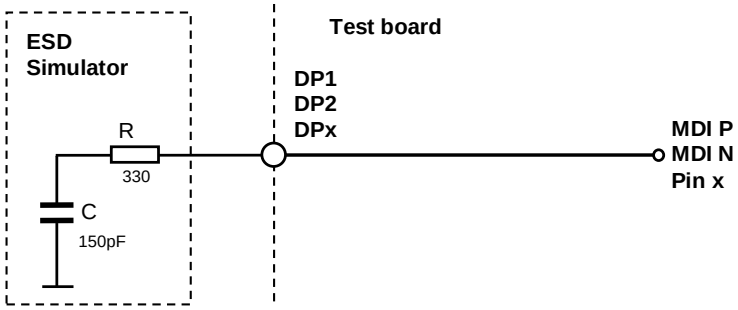



**Figure 3-18: Direct ESD test network for Ethernet link**

Special environmental conditions:

The requirements of [IEC6] climatic environmental conditions shall be fulfilled.

### *3.2.1.2 Evaluation of transceiver immunity*

See section 3.1.1.4.2.

### *3.2.1.3 Test setup*

For testing ESD immunity of an unpowered transceiver, tests according to [IEC6] shall be performed. The test setup is shown in Figure 3-19 and Figure 3-20.

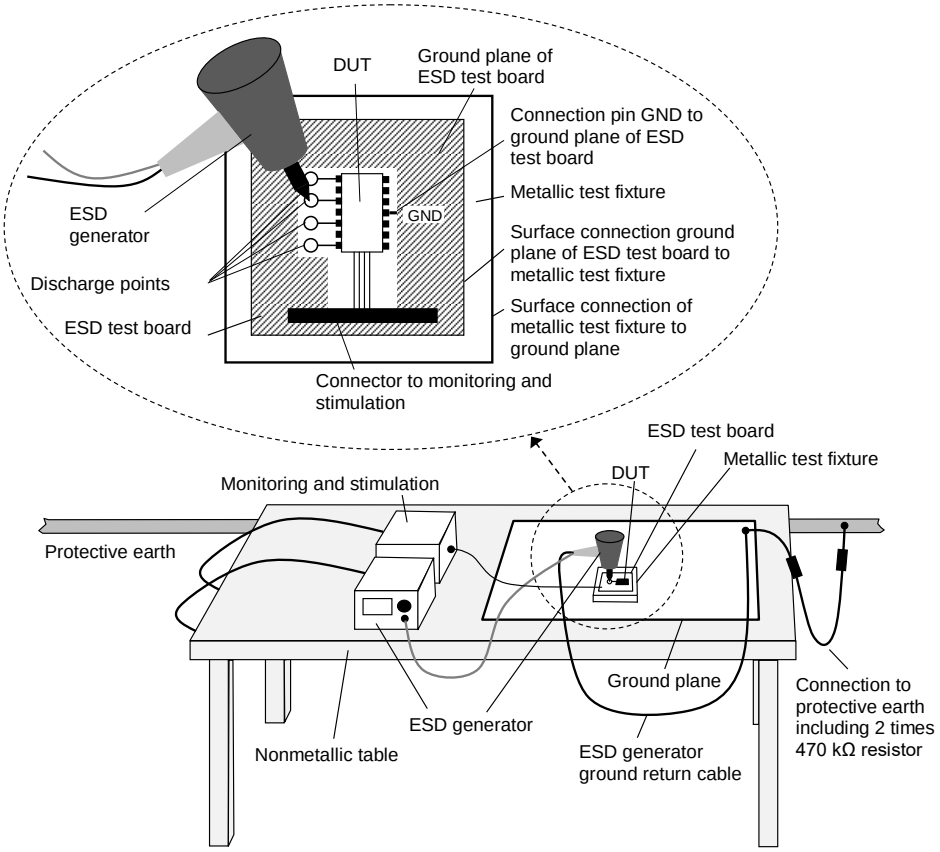



**Figure 3-19: Test setup for unpowered ESD tests – principal arrangement**

The ground plane with a minimum size of 0.5 m x 0.5 m represents the reference ground plane for the ESD test set-up and shall be connected to protective earth of the electrical grounding system of the test laboratory. The ESD test generator ground return cable shall be directly connected to this reference plane. The metallic test fixture positions the ESD test board and directly connects the ESD test board ground plane to the reference ground plane. The connections are made by surface contacts and must have a low impedance (R < 25 mΩ). This surface connection should have a contact area of at least 4 $cm^2$. Copper tapes can be used in addition. On testing the tip of the ESD test generator discharge module shall be directly contacted with one of the discharge points of the ESD test board.

For the evaluation of proper functionality of tested transceiver after each single test a specific test extension frame according to Figure 3-20 may be used for this purpose for contacting the ESD test board.

Test equipment requirements:

| | |
|---|---|
| ESD test generator: | according to [IEC6]; contact discharge unit with discharge capacitor 150 pF and discharge resistor 330 Ω |
| ESD test board: | according to Appendix A |
| Second Ethernet node system: | used as Ethernet link partner for functional validation after ESD test |
| Semiconductor parameter analyzer: | used for I/V measurement after ESD test |

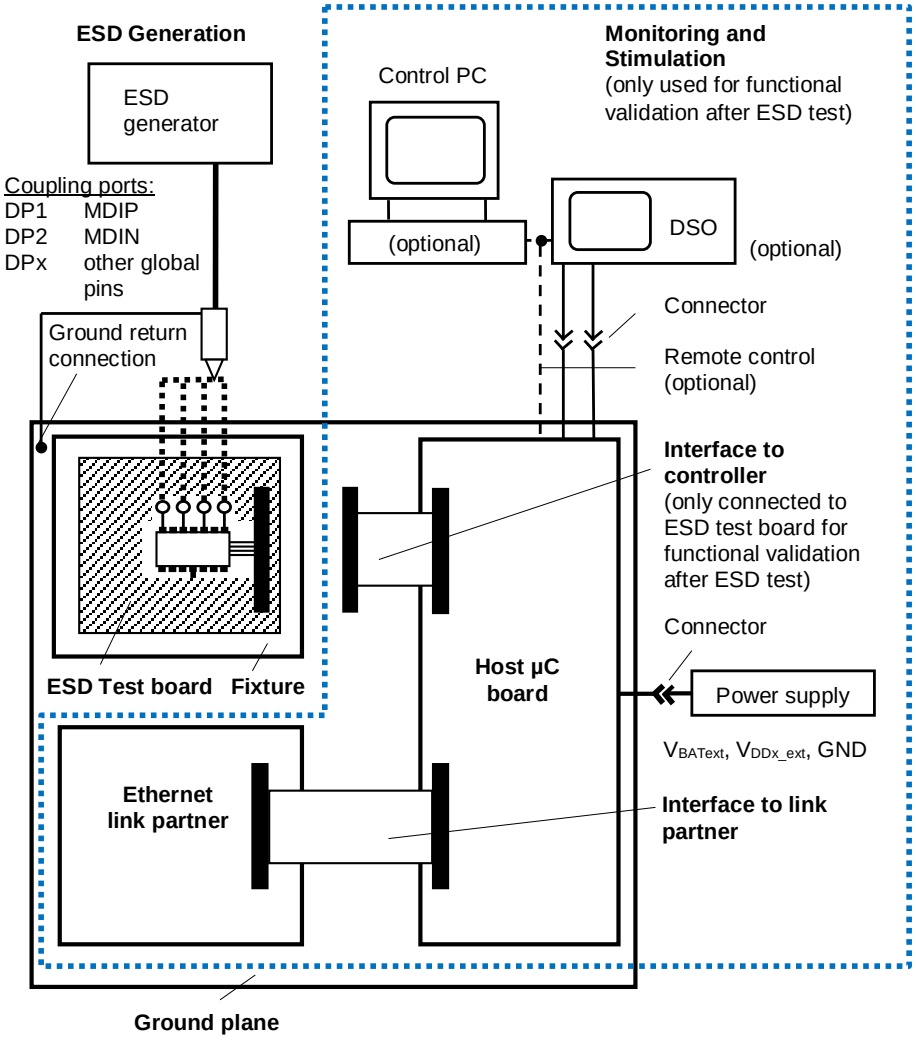



**Figure 3-20: Unpowered ESD tests – test setup, stimulation and monitoring for functional validation after ESD test**

#### *3.2.1.4 Test parameters*

To determine transceiver immunity against ESD, damage tests according to [IEC6] shall be done for every required pin with the parameters given in Table 3-14.

| | **Parameters** |
|---|---|
| Type of discharge | contact |
| Discharge circuit | R = 330 Ω, C = 150 pF [IEC6] |
| Discharge voltage levels | 1 kV to $V_{ESD\_damage}$ (max. 15 kV) |
| Discharge voltage steps | 1 kV |
| Test procedure | 1. Perform a reference test for function and a reference measurement for the I/V characteristic curve (pin to GND) on all pins to be tested.<br>2. Perform 3 discharges with positive polarity on discharge pad DP1 (MDI P) with 5 s delay between the discharges.<br>3. Connect the pin or discharge pad to the ground reference plane via a 1 MΩ resistor to ensure zero potential on the pin.<br>4. Perform failure validation<br>5. Repeat steps 2 through 4 on discharge pad DP2 (MDI N) and all other discharge pads if present (global pins X).<br>6. Repeat steps 2 through 5 using a discharge with negative polarity.<br>7. Repeat steps 2 through 6 using the next discharge voltage level until all tested pins are damaged. |
| Failure validation | Damage test to function status class D |
| MDI test network (BIN) | – none (discharge directly to the IC pins)<br>– standard<br>– optimized |

**Table 3-14: Test parameters and required tests for unpowered ESD**

The test shall be done at the specified ESD test voltages with a minimum of 3 transceivers.

The failure validation (functional test and V/I characteristic measurement) is to be carried out on a soldered transceiver. A specific test extension frame or IC adapter may be used for the purpose of contacting all necessary pins.

### *3.2.1.5 Test procedure for damage test*

The damage tests are to be carried out and documented according to the scheme given in Table 3-15. The fault criteria are evaluated after each single test.

| **Coupling** | | | | **Failure validation class** |
|---|---|---|---|---|
| **Points** | **Pin** | **MDI test network (BIN)** | **Parameter coupling** | |
| DP1,2 | MDI P / N | none (discharge direct to IC pins) | direct, contact discharge | D |
| | | standard | direct, contact discharge | |
| | | optimized | direct, contact discharge | |
| DPx | other global pins | standard or optimized | direct, contact discharge, external pin circuit according to data sheet or application hints | |

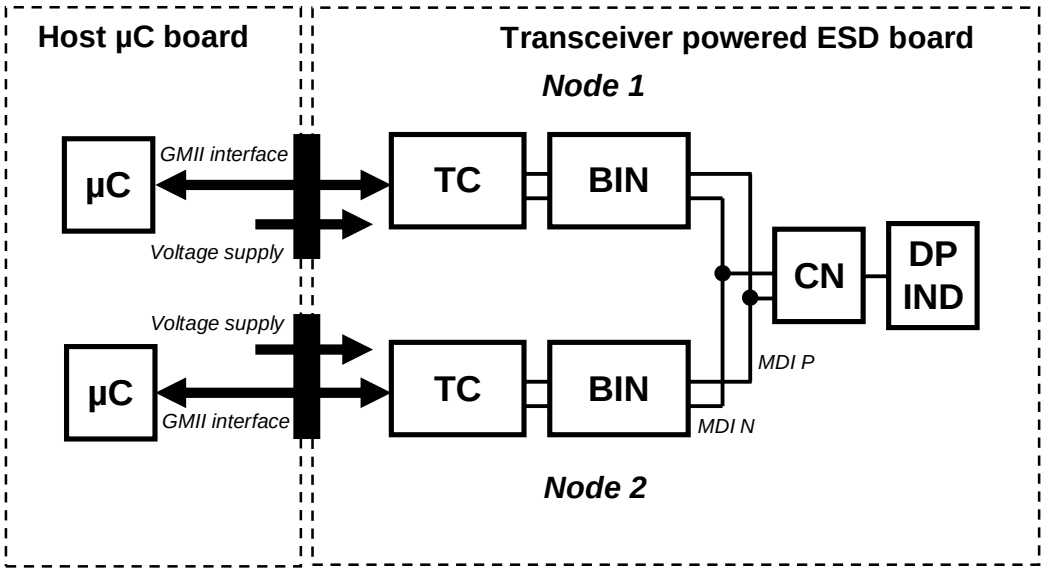
**Table 3-15: Required tests for unpowered ESD**

Recommended limits are given in Appendix C.4.

### 3.2.2 Powered ESD test

#### *3.2.2.1 Test configuration*

For testing the immunity of the powered transceiver against ESD, a combination of damage test and malfunction test of the MDI pins is required. The basic test configuration is given in Figure 3-21.




| | |
|---|---|
| TC | Ethernet transceiver (device under test – DUT) |
| BIN | MDI test network (including CMC, termination, additional filter elements, ESD protection) |
| CN | ESD coupling network |
| DP IND | Indirect ESD discharge point |

**Figure 3-21: Basic test configuration for ESD tests at powered Ethernet transceiver**

For the transceiver and MDI test network the same definitions are valid as stated for RF and transient testing (see section 3.1.1.2).

The symmetrical ESD coupling network given in Figure 3-22 is used when testing the Ethernet link. The difference between symmetrical passive components $C_1$ and $C_2$ must be less than or equal to 1 %. For matching of resistors $R_1$ and $R_2$ must be less than or equal to 0.1 %, which can be confirmed by measurement.

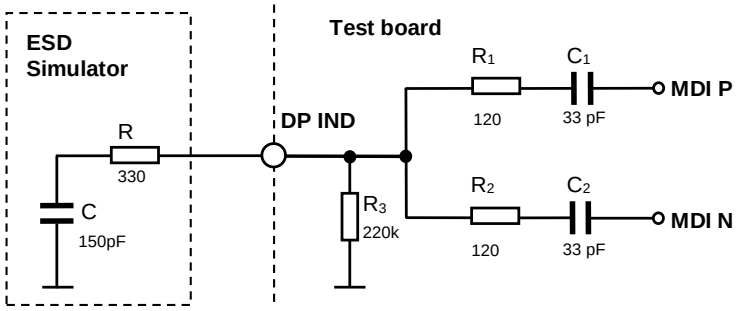



**Figure 3-22: Indirect ESD test network for Ethernet link**

The resistor $R_3$ prevents a static pre-charge of the coupling network to GND. All used resistors of the ESD coupling network shall be specified as ESD-robust up to the maximum used discharge voltage level. The specified peak voltage of used capacitors shall be at least 3 kV.

All other definitions of section 3.2.1.1 are valid.

#### *3.2.2.2 Evaluation of transceiver immunity*

See section 3.1.1.4.2.

### *3.2.2.3 Test setup*

For testing ESD immunity of powered transceiver, tests according to Figure 3-23 and Figure 3-24 shall be performed.

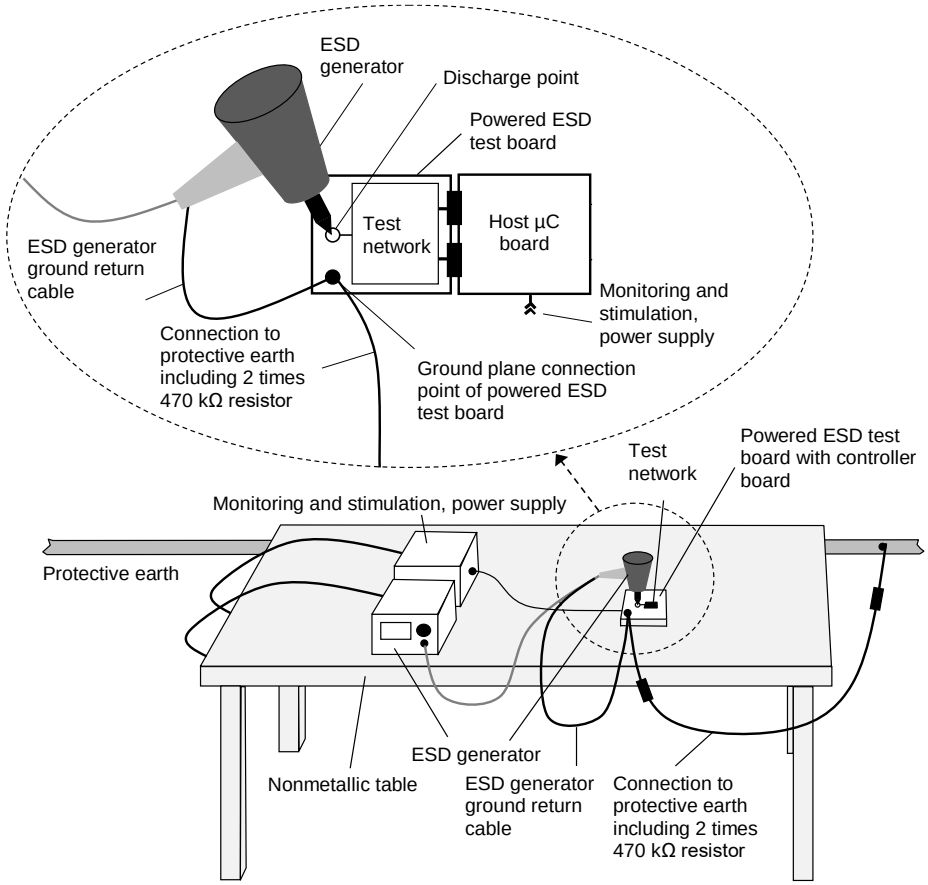



**Figure 3-23: Test setup for powered ESD tests – principle arrangement**

The ESD generator ground return cable shall be directly connected to ground plane of the powered ESD test board. This point shall be connected to protective earth of the electrical grounding system of the test laboratory. An optional ground plane with a minimum size of 0.5 m × 0.5 m can be used but shall be also connected to protective earth.

Test equipment requirements:

| | |
|---|---|
| ESD test generator: | according to [IEC6]; contact discharge module with discharge capacitor 150 pF and discharge resistor 330 Ω |
| ESD test board: | according to Appendix A |
| Host µC board: | according to Appendix A |
| Semiconductor parameter analyzer: | used for I/V measurement after ESD discharge |

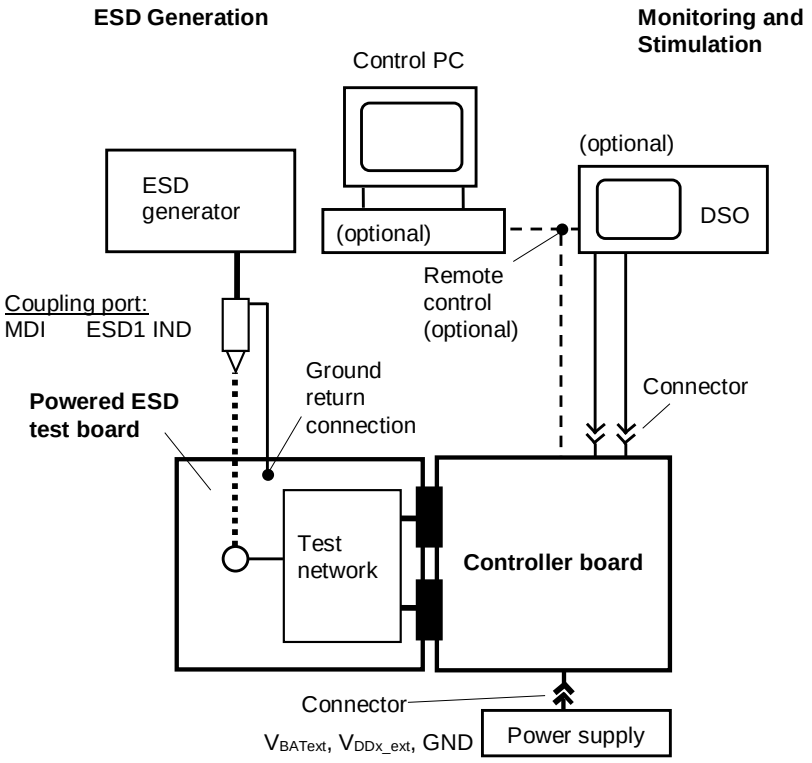



**Figure 3-24: Test setup for powered ESD tests – stimulation and monitoring**

### *3.2.2.4 Test parameters*

To determine the immunity against ESD of the powered transceiver, tests according to [IEC6] shall be done for the MDI pins with the parameters given in Table 3-16.

| | **Parameters** |
|---|---|
| Type of discharge | contact (to indirect ESD discharge point DP IND) |
| Discharge circuit | R = 330 Ω, C = 150 pF [IEC6] |
| Discharge voltage levels | 0.5 kV to 8 kV |
| Discharge voltage steps | 0.5 kV, 1 kV (starting at 1 kV) |
| Test procedure | 1. Disconnect DUT from power supply.<br>2. Perform a reference measurement for the I/V characteristic curve (pin to GND) on all pins to be tested.<br>3. Connect DUT to power supply and set it to low power mode with Ethernet test communication.<br>4. Perform 3 discharges with positive polarity on discharge pad DP IND with 5 s delay between the discharges with evaluation of function status classes according to Table 3-17 during test.<br>5. Send wake-up signal by counterpart node and check for proper wake-up function<br>6. Set DUT to normal mode with Ethernet test communication.<br>7. Perform a reference test for proper function.<br>8. Perform 3 discharges with positive polarity on discharge pad DP IND with 5 s delay between the discharges with evaluation of function status classes according to Table 3-17 during test.<br>9. Disconnect DUT from power supply.<br>10. Connect the pin or discharge pad to the ground reference plane via a 1 MΩ resistor to ensure zero potential on the pin.<br>11. Perform the I/V characteristic curve measurement (tested pin to GND) and failure validation.<br>12. Repeat steps 3 through 11 using a discharge with negative polarity. |

**Table 3-16: Test parameters and required tests for powered ESD**

The test shall be done at the specified ESD test voltages with a minimum of 3 transceivers.

### *3.2.2.5 Test procedure for combined malfunction and damage test*

The tests are to be carried out and documented according to the scheme given in Table 3-17. The fault criteria are evaluated after each single test.

| **Coupling** | | | | **Failure validation class** | |
|---|---|---|---|---|---|
| **Point** | **Pin** | **MDI test network (BIN)** | **Parameter coupling** | **Normal mode** | **Low power mode** |
| DP IND | MDI P / N | standard or optimized | indirect, contact discharge | A1 )1, A2 )2, C or D must be stated as test result | A3 )3 must be stated as test result |

)1 A1: no Link error occurred

)2 A2: no CRC error and DDT error occurred

)3 A3: no unwanted wake-up caused by ESD discharges, proper wake-up functionality and correct change into normal mode on request

**Table 3-17: Required tests for powered ESD**

Recommended limits are given in Appendix C.4.

# Appendix A - Test circuit boards

## A.1 RF and transient tests

A printed circuit board shall be used for RF and transient tests with the used node to node network. To ensure good RF parameters of the coupling and measuring networks, a PCB with at least four layers should be used. The length of the coupling paths on the test board should be kept as short as possible. The insertion losses of the DPI coupling ports as well as the 150 Ohm emission ports to the respective transceiver signal pads of the test board shall be measured and documented in the test report.

## A.2 ESD tests

For powered ESD tests the test circuit board shall be in-line with the definitions of test board for RF and transient tests. It should be modified for the coupling network at MDI to avoid any disruptive discharge from the coupling network to ground plane at a test voltage of 15 kV.

For unpowered ESD tests a printed circuit board shall be used. A four-layer construction of the PCB shall be chosen with extensive ground area. The pads for the discharge points DPx are to be carried out in such a way that a safe contact to the discharge tip of the testing generator is guaranteed. The passive components of the minimal wiring network shall be placed in direct proximity of the transceiver.

The insulation distance between the signal lines and pads of the passive components and the extensive ground area should be chosen in such a way, that a disruptive discharge at a test voltage of 8 kV is impossible at these points.

Further requirements apply to the ESD test board:

| | |
|---|---|
| Trace length between pads MDI test network and discharge point: | 25 mm – 30 mm |
| Track width of the conducting path: | 0.254mm (10 mil) |
| Substrate material: | FR4 |
| Thickness substrate: | 1.5 mm |

The test adapter used for functional and leakage current examination makes direct contacting of the transceiver pins possible.

# Appendix B - Required information from semiconductor manufacturer

The following information is required for setting up and doing the EMC tests at 1000BASE-T1 transceivers and shall be supported by the semiconductor manufacturer:

- test circuit for typical application of transceiver according to section 3.1.1.2 (standard MDI test network)
- software configuration data for setting the transceiver in typical application according to section 3.1.1.3
- detailed information for data transmission and error register read out activity.

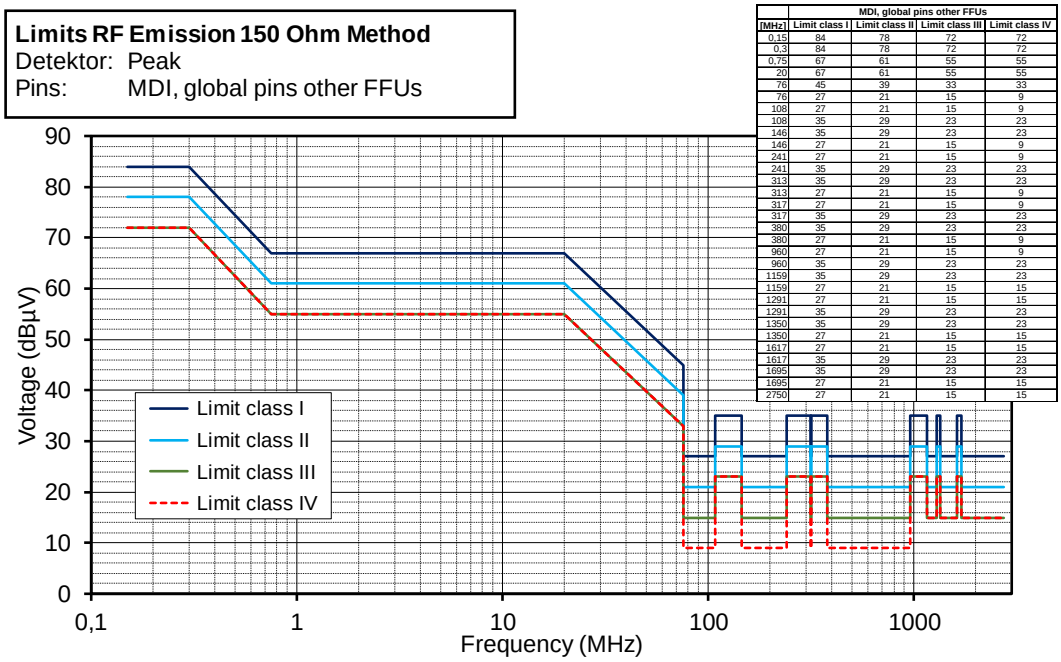
The following additional information should be supported by the semiconductor manufacturer, if available or needed respectively:

- EMC optimized test circuit (optimized MDI test network and optimized filter or supplier specific filter at voltage supply pins)
- information for ESD protection devices
- layout application hints or equivalent layout requirements
- software configuration data for setting the transceiver in EMC optimized state.

# Appendix C – Recommended limits for tests

## C.1 Emission of RF disturbances

For evaluation of RF emissions at the MDI, other global pins and voltage supply pins the limits given in Figure C-1 and Figure C-2are recommended. The required limit class depend on the application conditions (e.g. usage of unshielded twisted pair cable or shielded twisted pair cable for the Ethernet link) and will be defined by the customer.




| | MDI, global pins other FFUs | | | |
|---|---|---|---|---|
| [MHz] | Limit class I | Limit class II | Limit class III | Limit class IV |
| 0,15 | 84 | 78 | 72 | 72 |
| 0,3 | 84 | 78 | 72 | 72 |
| 0,75 | 67 | 61 | 55 | 55 |
| 20 | 67 | 61 | 55 | 55 |
| 76 | 45 | 39 | 33 | 33 |
| 76 | 27 | 21 | 15 | 9 |
| 108 | 27 | 21 | 15 | 9 |
| 108 | 35 | 29 | 23 | 23 |
| 146 | 35 | 29 | 23 | 23 |
| 146 | 27 | 21 | 15 | 9 |
| 241 | 27 | 21 | 15 | 9 |
| 241 | 35 | 29 | 23 | 23 |
| 313 | 35 | 29 | 23 | 23 |
| 313 | 27 | 21 | 15 | 9 |
| 317 | 27 | 21 | 15 | 9 |
| 317 | 35 | 29 | 23 | 23 |
| 380 | 35 | 29 | 23 | 23 |
| 380 | 27 | 21 | 15 | 9 |
| 960 | 27 | 21 | 15 | 9 |
| 960 | 35 | 29 | 23 | 23 |
| 1159 | 35 | 29 | 23 | 23 |
| 1159 | 27 | 21 | 15 | 15 |
| 1291 | 27 | 21 | 15 | 15 |
| 1291 | 35 | 29 | 23 | 23 |
| 1350 | 35 | 29 | 23 | 23 |
| 1350 | 27 | 21 | 15 | 15 |
| 1617 | 27 | 21 | 15 | 15 |
| 1617 | 35 | 29 | 23 | 23 |
| 1695 | 35 | 29 | 23 | 23 |
| 1695 | 27 | 21 | 15 | 15 |
| 2750 | 27 | 21 | 15 | 15 |

**Figure C-1: Recommended limits for RF emission for MDI and other global pins**

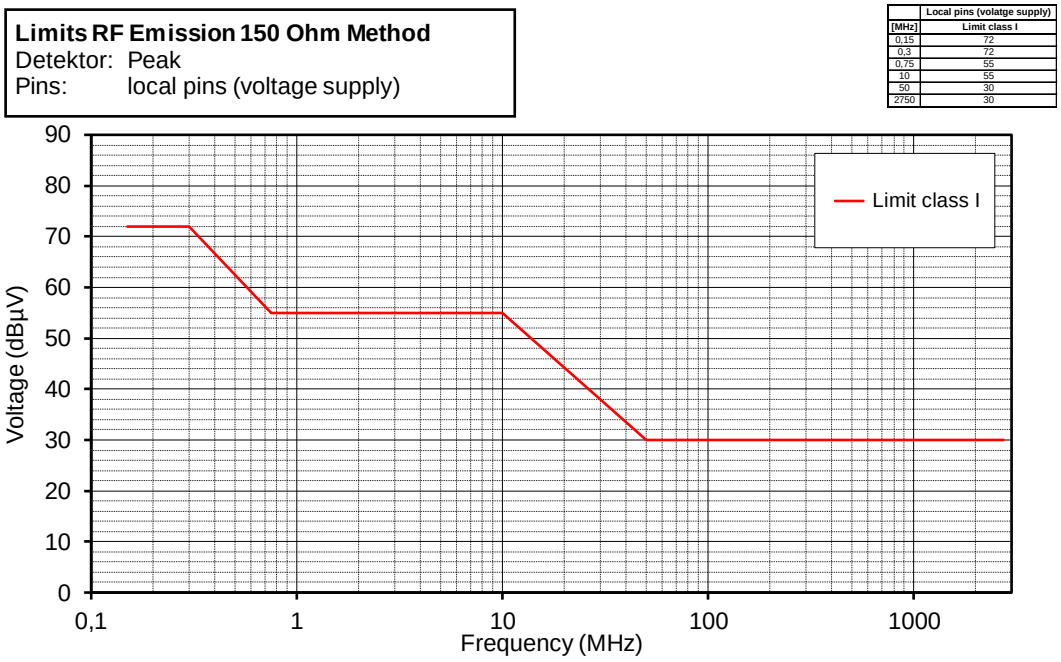



**Figure C-2: Recommended limits for RF emission for local pins**

## C.2 Immunity to RF disturbances

For evaluation of RF immunity of the MDI and other global pins the limits given in Figure C-3 and Figure C-4 for damage tests and Figure C-5 and Figure C-6 for malfunction tests are recommended. The required limit class depend on the application conditions (e.g. usage of unshielded twisted pair cable or shielded twisted pair cable for the Ethernet link) and will be defined by the customer.

**Limits RF Immunity DPI Test Method - Damage**
RF coupling: MDI

| MDI | | | | |
|---|---|---|---|---|
| [MHz] | Limit class I | Limit class II | Limit class III | Limit class IV |
| 1 | 12 | 15 | 18 | 21 |
| 8 | 30 | 33 | 36 | 39 |
| 88 | 30 | 33 | 36 | 39 |
| 1000 | 24 | 27 | 30 | 33 |
| 2000 | 22,25 | 25,25 | 28,25 | 31,25 |

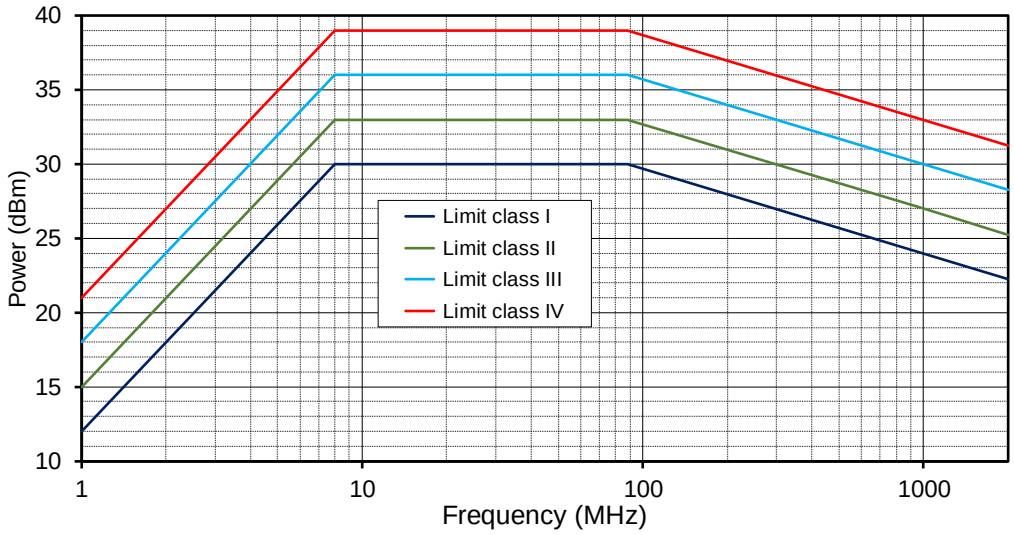



**Figure C-3: Recommended limits for RF immunity damage tests MDI**

**Limits RF Immunity DPI Test Method - Damage**
RF coupling: global pins other FFUs

| Global Pins ander FFUs | |
|---|---|
| [MHz] | Limit class I |
| 1 | 15 |
| 8 | 33 |
| 88 | 33 |
| 1000 | 27 |

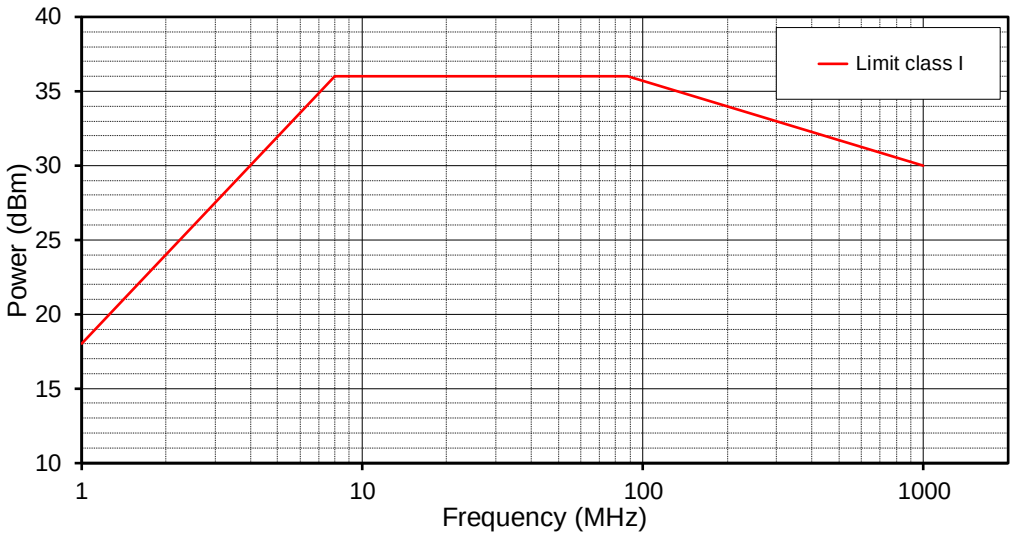



**Figure C-4: Recommended limits for RF immunity damage tests global pins other FFUs**

**Limits RF Immunity DPI Test Method - Malfuntion**
RF coupling: MDI

| MDI | | | | |
|---|---|---|---|---|
| [MHz] | Limit class I | Limit class II | Limit class III | Limit class IV |
| 1 | 12 | 15 | 18 | 21 |
| 8 | 30 | 33 | 36 | 39 |
| 88 | 30 | 33 | 36 | 39 |
| 1000 | 24 | 27 | 30 | 33 |
| 2000 | 22,25 | 25,25 | 28,25 | 31,25 |

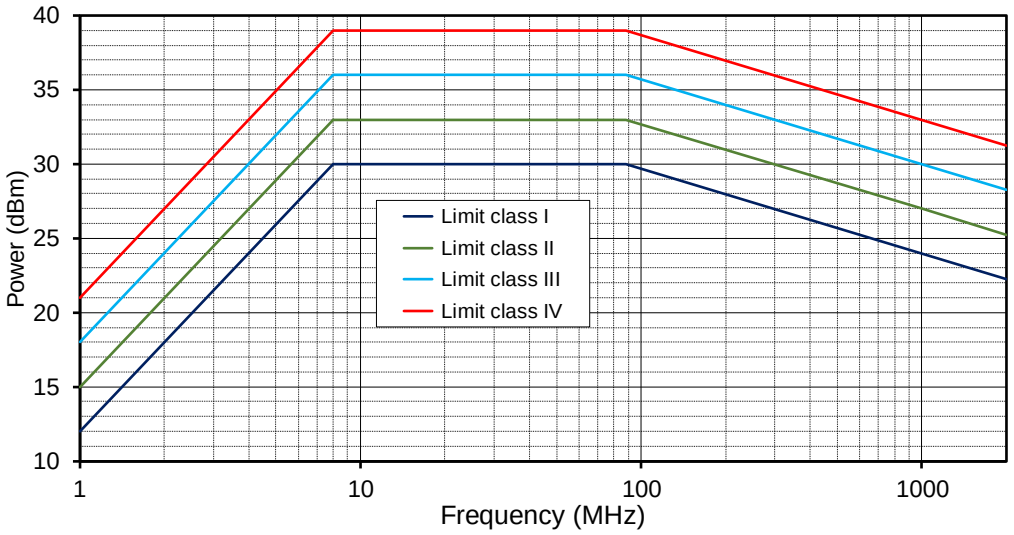



**Figure C-5: Recommended limits for RF immunity malfunction tests MDI**

**Limits RF Immunity DPI Test Method - Malfuntion**
RF coupling: global pins other FFUs

| Global Pins ander FFUs | |
|---|---|
| [MHz] | Limit class I |
| 1 | 15 |
| 8 | 33 |
| 88 | 33 |
| 1000 | 27 |

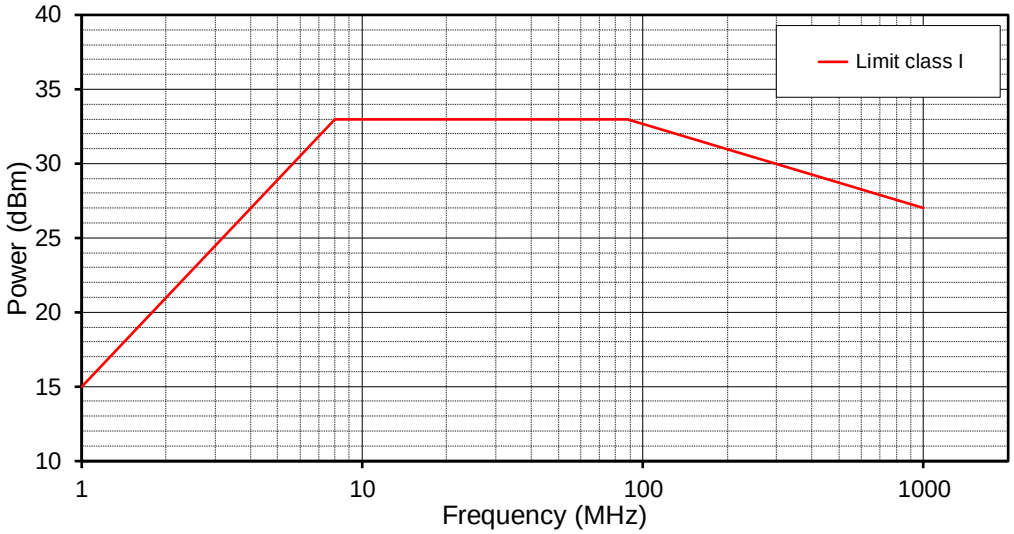



**Figure C-6: Recommended limits for RF immunity malfunction tests global pins other FFUs**

## C.3 Immunity to transients

For evaluation of transient immunity of the MDI and other global pins only limits for damage are recommended:

| Test pulse | $V_s$ [V] |
|---|---|
| 1 | - 100 |
| 2a | + 75 |
| 3a | - 150 |
| 3b | + 100 |

**Table C-1: Recommended voltage levels for transient immunity to damage**

## C.4 ESD

For ESD immunity to damage of the MDI with standard or optimized BIN in powered and unpowered mode and other global pins in unpowered mode +/- 6 kV ESD test voltage is recommended.

For ESD immunity tests of the MDI with standard or optimized BIN in powered mode to function status class A1 (no Link error) and A3 (no unwanted wake-up caused by ESD discharges, proper wake-up functionality and correct change into normal mode on request) +/- 3 kV ESD test voltage is recommended.

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