IEEE 100BASE-T1 System Implementation Specification

Version 1.0

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This specification provides general definitions and requirements for 100BASE-T1 interfaces, which are intended to be used on automotive applications.

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Contents

1 Copyright Notice and Disclaimer

2 Scope

The purpose of this document is to provide general definitions and requirements for 100BASE-T1 interfaces, which are intended to be used on automotive applications. As well the implementation defined in this document shall be used for all tests of transceivers/integrated circuits:

- EMC [8],
- Interoperability [7],
- Conformance (PMA [5], PCS [6] and PHY Control [4]).

Note:
Within the conformance tests there may be tests where the implementation of the Bus Interface Network (BIN) is not relevant. The specified implementation shall be used where necessary.

Communication systems using Power over data line (PoDL) are not related by this specification.

3 Motivation

This document defines implementation of 100BASE-T1 interfaces in automotive applications.

The requirements are valid for all kind of transceivers which are intended to be used in automotive applications:

- Stand-alone transceiver (PHYs),
- Switches with integrated or separated transceiver cells and
- Integrated circuits (e.g. SBCs, ASICs) with integrated transceiver cells.

This document contains requirements applied to passive components used for the BIN.

The respective definitions and requirements for system testing (ECU level qualification) are defined as well.

A Transceiver (PHY or switch port) of a 100BASE-T1 system implemented according to the above defined implementation shall fulfill the following requirements. All tests have to be fulfilled in an identical configuration.

Note:
This means all tests have to be conducted in one configuration, which is according to the defined implementation and with a channel (when needed) according to this specification as well.

In the current document the following defined terminology prescription applies. The usage of

- “Shall” expresses in the text a mandatory requirement.
- “Should” expresses in the text an optional requirement.
- “Must” expresses in the text a normative requirement.
- “Can” expresses in the text a permitted practice or method.

All tolerance values mentioned in this specification include initial tolerance, aging and temperature effects according to the application profile (service life, temperature profile) as specified in the Component Requirement Specifications of the affected components.

4 Normative references

[1] IEEE P802.3bwTM Physical Layer Specifications and Management Parameters for 100 Mb/s Operation over a Single Balanced Twisted Pair Cable (100BASE-T1)

[2] IEEE P802.3bp™: Physical Layer Specifications and Management Parameters for 1 Gb/s Operation over a Single Twisted Pair Copper Cable

[3] IEEE P802.3-2015 IEEE Standard for Ethernet

[4] OPEN ALLIANCE: 100BASE-T1 PHY Control Test Suite – Revision 1.0

[5] OPEN ALLIANCE: 100BASE-T1 Physical Media Attachment Test Suite – Revision 1.0

[6] OPEN ALLIANCE: 100BASE-T1 Physical Coding Sublayer Test Suite – Revision 1.0

[7] OPEN ALLIANCE: 100BASE-T1 Interoperability Test Suite – Revision 1.0

[8] OPEN ALLIANCE: 100BASE-T1 Transceiver EMC Specification – Revision 1.0

[9] OPEN ALLIANCE: Automotive Ethernet ECU Test Specification– Revision 2.0

[10] OPEN ALLIANCE: Switch Semiconductor Test Specification, V1.0

[11] OPEN ALLIANCE: 100BASE-T1 Common Mode Choke Test Specification – Revision 1.0

[12] OPEN ALLIANCE: 100BASE-T1 Definitions for Communication Channel – Revision 1.0

[13] OPEN ALLIANCE: Sleep/Wake-up Specification for Automotive Ethernet – Revision 1.0

[14] OPEN ALLIANCE: Advanced diagnostic features for automotive Ethernet PHYs – Revision 1.0

[15] OPEN ALLIANCE: 100BASE-T1 EMC Test Specification for ESD suppression devices – Revision 1.0

[16] ISO / IEC 11801:2002 Information technology — Generic cabling for customer premises

5 Abbreviation

PHY	PHY is a Physical layer interface device, often called transceiver
ECU	Electronic Control Unit – a device in a vehicle
BIN	Bus Interface Network
OEM	Vehicle Manufacturer / Original Equipment Manufacturer
CIDM	Characteristic Impedance Differential Mode
IL	Insertion Loss
RL	Return Loss
S-Parameter	Scattering Parameter
TDR	Time Domain Reflectometry
SCC	Standalone Communication Channel

6 Overview

This document includes three main chapters:

- Implementation for 100BASE-T1, chapter 7
  This chapter defines the interface implementation for automotive applications together with requirements on components used to realize this Bus Interface Network (BIN).

- 100BASE-T1 testing requirements and system requirements, chapter 8
  This chapter defines further system requirements for systems implemented according to the system implementation.

- System test environment definition, chapter 9
  This chapter defines the system test environment, in which the transceiver as implemented system requirements shall be evaluated.

7 Implementation for 100BASE-T1

7.1 General

For 100BASE-T1 automotive Ethernet the physical layer implementation of a BIN shall be implemented according to the following definitions. All values and requirements listed in this document shall be valid within the specified temperature range (-40°C … +85°C / 105°C / 125°C) of the implemented system.

7.2 Interface circuitry definition

A 100BASE-T1 interface shall be implemented according to the requirements defined in IEEE P802.3bw™ [1] and as shown in Figure 1.

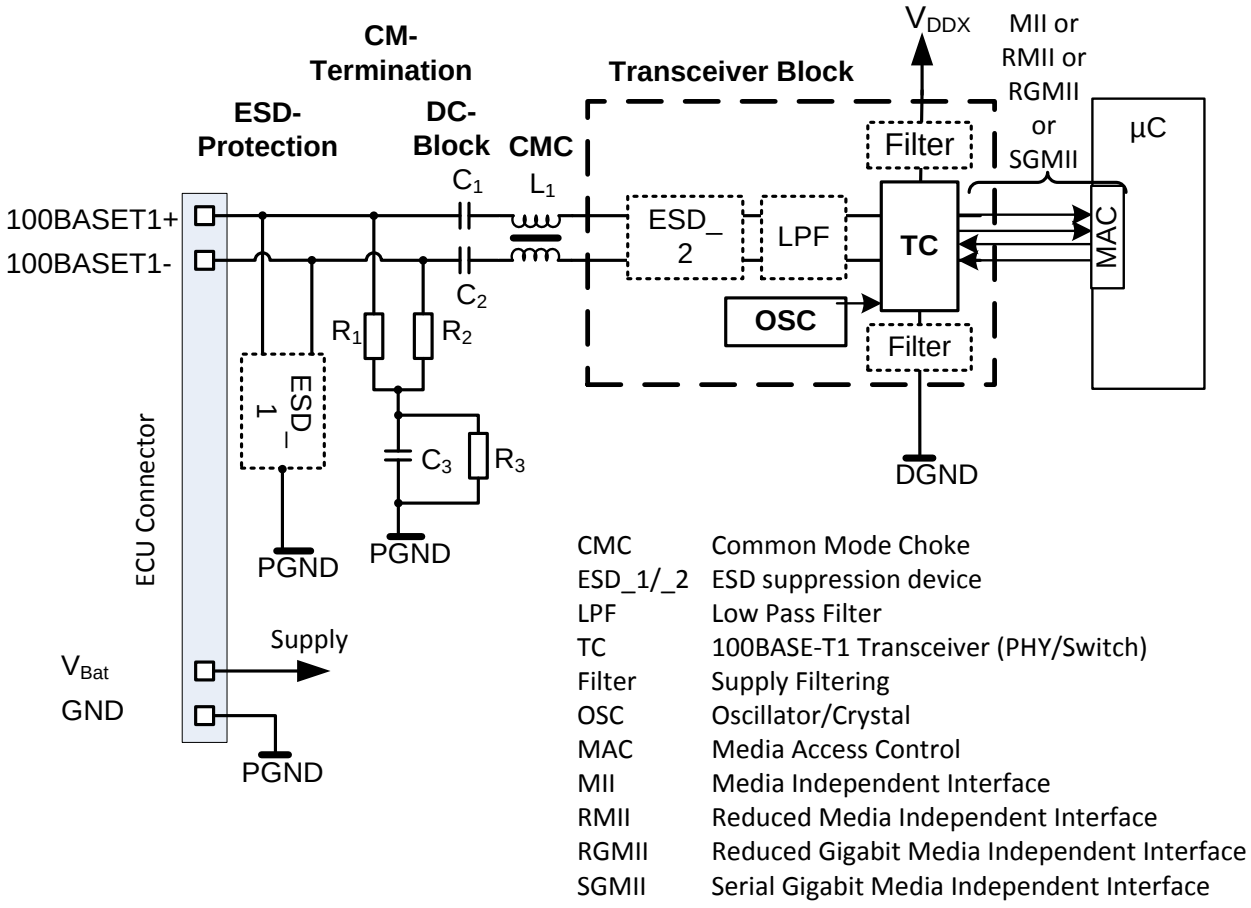
The interface consists of the Transceiver block (which includes the Transceiver, optional low pass filter, optional ESD protection devices and supply filtering; all of that according to the datasheet and application notes of the Transceiver manufacturer), common mode choke (CMC), DC block capacitors (DC), common mode termination network (CMT), an optional ESD position (ESD) and the ECU connector (CON). All passive components of the 100BASE-T1 interface shall be implemented as required in Table 1 and in chapter 7.3.

For layout design information of a specific system implementation the application notes of semiconductor manufacturers shall be considered.

If configuration of the transceiver by software is necessary (i.e. configuration script), this shall also be implemented according to the application notes of the semiconductor manufacturers. The layout and the configuration of the transceiver shall be reviewed by the semiconductor manufacturer.

An exemplary documentation for the used circuitry in a test documentation is provided in appendix chapter 10.1.

Note:
For short start up time it is recommended to e.g. use hardware strap-in pins for PHY configuration.



CMC	Common Mode Choke
ESD_1/_2	ESD suppression device
LPF	Low Pass Filter
TC	100BASE-T1 Transceiver (PHY/Switch)
Filter	Supply Filtering
OSC	Oscillator/Crystal
MAC	Media Access Control
MII	Media Independent Interface
RMII	Reduced Media Independent Interface
RGMII	Reduced Gigabit Media Independent Interface
SGMII	Serial Gigabit Media Independent Interface

PGND is defined as direct connected to external GND connection.

DGND is defined as internal GND for transceiver and/or other digital ICs (e.g. micro controller). It can be decoupled by an inductor from external GND connection.

Figure 1 interface circuitry/schematic for 100BASE-T1.

Ref	Part	Remarks
	Transceiver Block	The transceiver block (transceiver including ESD protection device (ESD_2) and LPF according to application notes) has to fulfill the requirements of the OPEN Alliance specifications (refer to [IEEE802.3bw]). Validated and released recommended transceivers are listed in chapter "100BASE-T1 Transceivers".[2]
L1	**Common mode choke**	Has to fulfill the requirements according to [11].
C_1, C_2	**Capacitor** 100nF **Tolerance** ≤ 10% **voltage range**[1] ≥ 50V	
R_1, R_2	**Resistor** 1kOhm **Tolerance** ≤ 1% (even after ESD test) **Power rating** ≥ 0.4W **ESD resistance** ≥ 6kV	Termination circuitry for common mode RF currents on the data line. Therefore, resistors need sufficient power loss and capacitor need sufficient electrical strength.
C_3	**Capacitor** 4.7 nF **Tolerance** ≤ 10% **Voltage range** [1] ≥ 50V	
R_3	**Resistor** 100kOhm **Tolerance** ≤ 10% **Power rating** ≥ 0.1W **ESD resistance** ≥ 6kV **Voltage range** [1] ≥ 50V	To avoid static charge of the cable harness
ESD_1	**ESD protection device**	Optional. Has to fulfill the requirements according to [15].
	ECU connector	Has to fulfill the requirements according to [12]. Further requirements and information can be found in chapter "ECU Connectors for100BASE-T1 Interfaces (MDI Interface)".

[1]According to car manufacture specifications for supply voltages ≥56V voltage range for 48V electrical systems, typically 100V min. electric strength recommended for ceramic caps. For 12V systems typ. 50V electrical strength is sufficient.

[2]It is required to follow the definitions of semiconductor manufacturer for external passive components and circuit, software configuration (script) and software flow definitions, which are defined in datasheet and application notes. The implementation of ESD protection element is optional, but according layout is mandatory in any case. The implementation of Low Pass Filter for voltage supply is mandatory according to semiconductor manufacturer definition.

Table 1: Interface component requirements.

7.3 Requirements for 100BASE-T1 ECU Interface components

The components used in a 100BASE-T1 interface implementation shall fulfill the following requirements. The according testing requirements are described in chapter 8.2.

7.3.1 100BASE-T1 Transceivers (standalone or integrated in switch)

All Transceivers (PHYs or Switches) used in a 100BASE-T1 interface shall comply with IEEE P802.3bw™ [1].

7.3.1.1 Transceiver functional requirements

All transceivers (PHYs or Switches) used in a 100BASE-T1 interface shall be tested according to the following requirements:

- The PHY/switch shall support test modes acc. to [1].
- The PHY/switch shall support a mode which deactivates all signaling on the BIN, while the BIN termination is still active (e.g. called "TX_off" or "scrambler_off").
- The PHY/switch shall provide link status information via a register, according to [3].
- The PHY/switch shall provide a communication_ready status information via a register, according to [14].
- The PHY/switch shall provide information on CRC or symbol failures on physical layer level via a register.
- The PHY/switch shall be able to detect a short between bus lines and provide this information via a register according to [14].
- The PHY/switch shall be able to detect interruptions of bus lines and provide this information via a register according to [14].
- The PHY/switch shall be able to detect wrong polarity and provide this information via a register.
- The PHY/switch can be able to correct the polarity
- The PHY/switch shall provide link quality information (e.g. SQI based on SNR) via a status register according to [14].

If one of the above is not fulfilled a reason/substitution for this shall be documented. An exemplary documentation is provided in appendix chapter 10.2.

7.3.1.2 Transceiver conformance, EMC and Interoperability requirements

All transceivers (PHYs or Switches) used in a 100BASE-T1 interface shall be conformant to 100BASE-T1 according to the following test specifications:

- OPEN ALLIANCE: 100BASE-T1 PHY Control Test Suite – Revision 1.0 [4]
- OPEN ALLIANCE: 100BASE-T1 Physical Media Attachment Test Suite – Revision 1.0 [5]
- OPEN ALLIANCE: 100BASE-T1 Physical Coding Sublayer Test Suite – Revision 1.0 [6]
- OPEN ALLIANCE: 100BASE-T1 Interoperability Test Suite – Revision 1.0 [7]
- OPEN ALLIANCE: 100BASE-T1 Transceiver EMC Specification – Revision 1.0 [8]

Further details of this test are described in chapter 8.2.

7.3.1.3 Evaluation/Testing Capabilities for integrated circuitries

To allow evaluation, 100BASE-T1 Test Mode functionality with Test Modes 1 to 5 (refer to [1]) shall be implemented for each 100BASE-T1 interface of the tested integrated circuit.

The tested integrated circuit shall be able to deactivate data transmission ("SEND_Z", e.g. "TX off" or "Scrambler off") of each 100BASE-T1 interface. See also chapter 8.4.3 (Evaluation/Testing Capabilities).

Note:
This is to allow MDI return loss and MDI Mode conversion reflection test with proper termination inside the Transceiver (i.e. 100 Ω).

7.3.1.4 Further Transceiver requirements

Further qualification of transceivers on system level shall be done according to chapter 8 and 9.

7.3.2 Common Mode Choke for 100BASE-T1 interfaces

All common mode chokes used in a 100BASE-T1 interface shall be tested according to [9].

The requirements of the CMC Test Specification (recommended values in the appendix C of [9]) are mandatory.

7.3.3 ECU connectors for 100BASE-T1 interfaces (MDI interface)

The complete channel as well as all individual components (cables and connectors as well as assembled cable harness) of a 100BASE-T1 link shall fulfill the channel requirements according to [12]. Therefore all components of the link shall be designed and assembled to ensure the required RF parameters.

The ECU connector implementation shall fulfill the connector requirements of [12].

7.3.4 ESD Elements

A landing pad according to the transceivers application note for an optional ESD element shall be on the interface layout.

The ESD element can either be placed in the transceiver block or directly in front of the common mode choke – as shown in Figure 1.

An ESD element placed between connector and CMC has to fulfill the requirements defined in [15].

7.3.5 Clock tolerance requirements

A typical clock source with 25MHz is used for clock generation, its tolerance shall be less than ±100ppm (±0.01%) (100BASE-T1 link start-up is very sensitive to clock tolerances). For details refer to the Transceiver`s application notes.

The clock tolerance requirement ≤ ±100ppm shall be fulfilled including aging and temperature effects.

8 100BASE-T1 testing requirements and system requirements

8.1 General

A Transceiver (PHY or switch port) of a 100BASE-T1 system implemented according to the above defined implementation shall fulfill the requirements listed in the below chapter. All tests have to be fulfilled in an identical configuration.

Note:
This means all the following tests have to be conducted in one configuration, which is according to chapter 7 and with a channel (when needed) according to chapter 9.

All used information for test ECU design (App Notes, Layout recommendation, configuration etc.) shall be documented in the test reports. There must not be used any further undocumented information (e.g. configuration of undocumented registers). The layout and the used configuration shall be reviewed by the semiconductor manufacturer and the review documentation shall be part of the documentation.

8.2 Transceiver testing requirements

8.2.1 Configuration for testing

The configuration for all the following tests (chapter 8.2.2 to 8.2.4) shall be identical and according to chapter 7. Additionally, the used CMC in the BIN shall be compliant with [9].

The channel types 1, 2 and 3 as defined in chapter 10 shall be used for testing.

8.2.2 Conformance Test requirements

All tests of [4], [5] and [6] shall be conducted. The requirements as defined in [4], [5] and [6] are valid.

8.2.3 Interoperability Test Requirements

All tests of [7] shall be conducted. The requirements as defined in [7] are valid.

8.2.4 EMC Test requirements

All tests of [8] shall be conducted. The requirements as defined in [8] are valid. For the avoidance of doubt all recommended limits shall be met as mandatory.

8.3 Qualification of 100BASE-T1 derivative devices

8.3.1 Scope

These definitions shall be used for a harmonized test approach for derivatives of 100BASE-T1 transceivers devices within the qualification tests according to [4]; [5]; [6]; [7], [8], [9] and [10].

8.3.2 General

In general, all 100BASE-T1 – transceiver devices (transceiver block) must fulfill the requirements of the qualification test specifications listed in 8.3.1 and have to be tested completely and separately against the specifications.

In case of different 100BASE-T1 transceiver devices with common underlying technical implementation and minor differences, the users of this specification may

- define an adoptable 100BASE-T1 transceiver devices family and device derivatives of this family
- agree upon options for reduction of single qualification test cases.

This specification contains requirements for the qualification test plan definition for family of 100BASE-T1 transceiver devices.

In order to minimize the required qualification tests for device derivatives, a common practice for “family plan” qualification, including test planning, execution and reporting shall be established.

8.3.3 Terms and Definitions

In the meaning of the requirements within this document, different transceiver device types may be combined to a 100BASE-T1 transceiver family if their dies, circuitries, setting, functionality ranges / feature set and operation parameters are identical, only. This means, in the context and coverage of these definitions, only the applicable (permitted) differences between transceiver devices within one semiconductor family are different packages and different bonding implementations.

Transceiver derivatives	A transceiver type that belongs to a 100BASE-T1 transceiver family
Transceiver umbrella derivative	100BASE-T1 transceiver which is supposed to cover the maximum critical family implementations
Transceiver root derivative	The chronological first available device derivative

Note:
The transceiver root is not necessarily the umbrella device.

8.3.4 Qualification Test Plan

At least root and umbrella devices have to be tested completely against the specifications listed in 8.3.1.

In certain cases, parts of these qualification tests may be transferred for the qualification of family derivatives which offers options to reduce the test scope. However, such reductions will only be valid, if all qualification tests on the umbrella and on the root derivative have been passed completely.

In general, even in case of similarities between 100BASE-T1 – transceiver devices e.g. of the same semiconductor manufacturer, all have to be tested separately and completely against the specifications listed in 8.3.1.

The adopters of this specification have to agree about the selection of the umbrella devices for establishing the test plans.

If no other definitions are made by the users of these specifications, the device derivatives with the in total maximum function / operating range, number of ports and / or pin are defined to be the most critical ones.

Note:
Based on its technical performances, e.g. because of most critical family implementations, the root derivative can also be defined to be the umbrella devices, too. In this case, at least the root derivative and one additional device have to be tested completely against the specifications listed in 8.3.1.

8.3.5 Qualification Test Performance

For the qualification of 100BASE-T1 transceiver device derivatives, this specification offers the following two options.

8.3.5.1 Case 1: Packaging

a. Derivate description, compared with umbrella / root derivate:
   - Differences: package type, size and / or pinout,
   - Commonalities: implementation of the transceivers die, xMII, MDI-/supply circuitry / filter and settings as well as functionality ranges / feature set and operation parameters (e.g. temperature and voltage range).

b. Options for action:
   - Ensure that device derivatives are subsets of umbrella / root derivative in matters of functionality ranges / feature set and hardware,
   - Migration of all root / umbrella derivative ´s results from qualification tests listed in 8.3.1,
   - Revision / re-run and evaluation of EMC- / ESD – Tests according to OPEN ALLIANCE: IEEE 100BASE-T1 EMC Test Specification for Transceivers
   -

8.3.5.2 Case 2: Bonding

a. Derivate description, compared with umbrella / root derivate:
   - Differences: reduced bonding, e.g. reduced number of MDI – ports,
   - Commonalities: implementation of the transceivers die, xMII, MDI-/supply circuitry / filter and settings as well as, package type, size, pinout as well as remaining functionality ranges / feature set and operation parameters (e.g. temperature and voltage range).

b. Options for action:
   - Ensure that device derivatives are subsets of umbrella / root derivative in matters of functionality ranges / feature set and hardware,
   - Migration of all umbrella / root derivative´s results from qualification tests listed in 8.3.1,
   - Revision / re-run and evaluation of EMC- / ESD – Tests according to OPEN ALLIANCE: IEEE 100BASE-T1 EMC Test Specification for Transceivers.

8.3.6 Documentation

For safeguarding and traceability reasons, all documentation within practical usages has to be binding. First of all, this must be applied for the identification of potential derivate options e.g. by datasheet descriptions.

All affected qualification test reports must document

- technical commonalities of and differences between 100BASE-1 transceiver devices (derivatives) under test and root / umbrella devices,
- motivation for selection derivative and umbrella / root devices,
- references to binding documents
- complete test results of devices (derivatives) under test and umbrella / root devices
- and test setup differences

8.3.7 Practical Usage: PHY, Switch and SOC Device Derivatives

In the following section there are several basic assumptions on the development of the different devices. Based on these assumptions the approaches for the qualification of device derivatives are different.

8.3.7.1 PHY Device Derivatives

The PHY is in most cases the basic device for any semiconductor vendor of Ethernet related products. Once a PHY is realized and about to be introduced on the market, there are almost no major changes encountered. Thus, following table for reduced test shall be used:

Differences between DUT and umbrella device	PCS Test	PHY_ Cont-Test	PMA Test	EMC ESD	IOP	Switch Test	ECU-Test (applicable for Tier1 suppliers)	
Package				X		n/a		-**No** different Feature -**No** new functionality
All other	X	X	X	X	X	n/a	X	

Table 2: PHYs - Tests cases on derivative differences

Note:

Explicitly: All changes to transceiver block including initialization settings (scripts) need a re-run of all tests. Modifying scripts is seen as a major change which requires complete re-testing against the complete specifications.

8.3.7.2 Switch Device Derivatives

The procedure is most important to switch devices. Switch devices have been seen in the past in the form that basically the same product was put on the market in different packages, with different number of ports.

Differences between DUT and umbrella device	PCS Test	PHY_ Cont-Test	PMA Test	EMC ESD	IOP	Switch Test	ECU-Test (applicable for Tier1 suppliers)	
Package				X				-**No** different feature -**No** new functionality
PHY-independent switch features						X	X	Enhancement of networking capabilities, whereas the technology, functionality and IP of the integrated PHYs are the same
Reduced number of ports				X				-**No** different feature -N**o** new functionality
All other	X	X	X	X	X	X	X	

Table 3: Switches - Tests cases on derivative differences

Note:
In case of Switch devices having several PHY instances where all of them are identical (except for the PHY address) and have identical BIN, then the conduction of conformance testing as defined in [4], [5] and [6] shall be required only for one PHY.

Note:
The term networking capability summarizes all switch-dependent features like, VLAN handling, QoS-features, filtering-capabilities, speed of the switching fabric (switching-rate), etc. The technology, functionality and IP of the integrated PHY are to be the same.

Changing the switching fabric (higher switching-rate) might affect the EMC performance of the device.

Note:
An example of this might be a family of products based on a single Silicon device and appear on the market as 7 port, 5 port and 3 port devices.

Here the test of the device which allow the test of all features will be sufficient

Note:
The re-assignment of pins to a different function available in the silicon, but not seen on devices in a previous test will need a complete re-test.

Example: Changing via bond-out or other configuration method other interfaces e.g. MDIO, MII not seen exactly in the same function in a previous test need a complete re-test.

8.3.7.3 SoC Device Derivatives

Systems on Chip (SoC) derivate may appear in very different forms. If SoC derivatives cannot be handled in the same manner as other 100BASE-T1 – transceiver devices, e.g. reduced bonding, all SoC derivatives must be tested completely and evaluated separately.

8.4 System Requirements

An ECU in cooperating one or more 100BASE-T1 interfaces shall fulfill the requirement listed in chapters 8.4.1 to 8.4.3 in terms of functional behavior and diagnostic functionality.

8.4.1 Wake-up Requirements

The system timing requirements provided in [13] (OPEN ALLIANCE: Sleep/Wake-up Specification for Automotive Ethernet – Revision 1.0) are valid.

8.4.2 Diagnostic requirements

The registers defined in [14] shall be accessible and their behavior shall be according to the requirements defined in [14] (OPEN ALLIANCE: Advanced diagnostic features for automotive Ethernet PHYs – Revision 1.0).

8.4.3 Evaluation/Testing Capabilities for ECUs

To allow evaluation of ECUs, the 100BASE-T1 Test Mode functionality with Test Modes 1 to 5 shall be implemented for each 100BASE-T1 interface of the ECU. (Refer to [1], IEEE P802.3bwTM Physical Layer Specifications and Management Parameters for 100 Mb/s Operation over a Single Balanced Twisted Pair Cable (100BASE-T1) for description of the test modes). See also chapter 7.3.1.3 (Evaluation/Testing Capabilities for integrated circuitries)

The ECU shall be able to deactivate data transmission (“SEND_Z”, e.g. “TX off” or “Scrambler off”) of each 100BASE-T1 interface to allow MDI return loss and MDI Mode conversion reflection test with proper termination inside the Transceiver (i.e. 100 Ω).

8.5 Additional tests required on ECU-level

The following tests from [9] (OPEN ALLIANCE: Automotive Ethernet ECU Test Specification– Revision 2.0) shall be conducted for analysis of the physical Layer behavior (Further higher layer test may be required as well):

Reference	Test	Requirement
OABR_PMA_TX1	Check the Transmitter Output Droop	Optional
OABR_PMA_TX2	Check the Transmitter Timing Jitter in MASTER Mode	Mandatory
OABR_PMA_TX3	Check Master Transmit Clock Frequency	Mandatory
OABR_PMA_TX4	Check the Transmitter Power Spectral Density (PSD)	Optional
OABR_PMA_TX5	Check the MDI Return Loss	Mandatory
OABR_PMA_TX6	Check MDI Mode Conversion	Mandatory
OABR_PMA_TX7	Check MDI Common Mode Emission	Optional [1)]
OABR_PMA_TX8	Check the Transmitter Distortion	Optional

Table 4: additional required tests on ECU-level.

1) The common mode emission of the 100BASE-T1 ECU interface is described in [8] (OPEN ALLIANCE: 100BASE-T1 Transceiver EMC Specification – Revision 1.0).

8.6 Cable harness recommendation for 100BASE-T1 Test Links

To allow a proper operation of the implemented interface, all 100BASE-T1 links within a cable harness assembly implementation should fulfill the channel requirements of [12] .

Therefore all components of the link should be designed and assembled to ensure the required RF parameters.

9 System test environment definition

9.1 General

This definition shall be used for defining a test wiring harness that simulates various communication channels according to the channel definitions of IEEE Std. 802.3bw [1] for tests of 100Base-T1 transceivers according to [4], [5],[6], [7] and [9].

The chapters also contain examples for a practical implementation.

9.2 Channel Type 1

9.2.1 General

The parameters of the type 1 channel are derived from the limit definition for a communication channel according to [1] and [12]. For setting up a real test harness upper and lower limits are added for each parameter. The type 1 channel implementation shall fulfill these limits at (23±2)°C ambient temperature (RT).

All tests for validation of the channel characteristics are defined in [12].

9.2.2 Required Parameters

The parameter and limits given in Table 5 are defined for a type 1 channel implementation.

Parameter	Sub clause [IEEE1]	Lower Limit	Upper Limit
CIDM	IEEE 802.3bw, 96.7.1.1	90 Ω	110 Ω
IL	IEEE 802.3bw, 96.7.1.2	1 MHz: 0.7 dB 10 MHz: 1.8 dB 33 MHz: 3.4 dB 66 MHz: 5.0 dB	1 MHz: 1.0 dB 10 MHz: 2.6 dB 33 MHz: 4.9 dB 66 MHz: 7.2 dB
RL)1	IEEE 802.3bw, 96.7.1.3	1 MHz: 18.0 dB 2 MHz: 18.0 dB 2 MHz: 18.0 dB 20 MHz: 18.0 dB 66 MHz: 12.8 dB	1 MHz: 23.0 dB 2 MHz: 23.0 dB 2 MHz: 30.0 dB 20 MHz: 30.0 dB 66 MHz: 24.8 dB
Propagation delay)2	-	2 MHz: 80.5 ns 66 MHz: 80.5ns	2 MHz: 85.5 ns 66 MHz: 85.5 ns

)1 within the limit relevant frequency range the following requirements are defined: all values of RL must be above the lower limit and in minimum 6 of 9 cable resonant caused local minima should be below to upper limit

)2 measurement of propagation delay according to [16]

Table 5: Required parameter and limits for channel type 1 implementations according to [12].

9.2.3 Example for Type 1 Communication Channel implementation

Figure 2 shows the topology of the example type 1 channel implementation. The description of each part of this implementation is given in Figure 3 and Table 6.

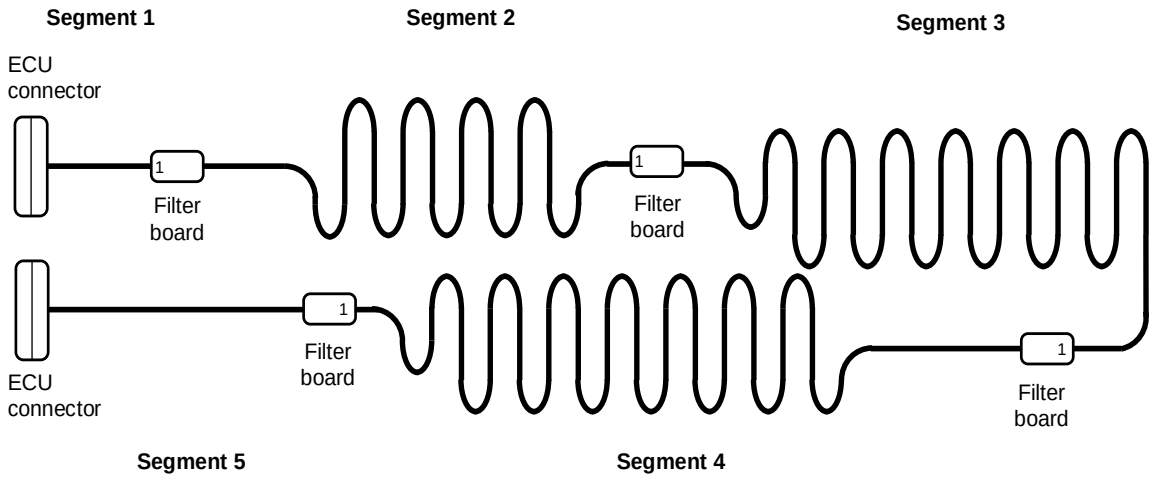
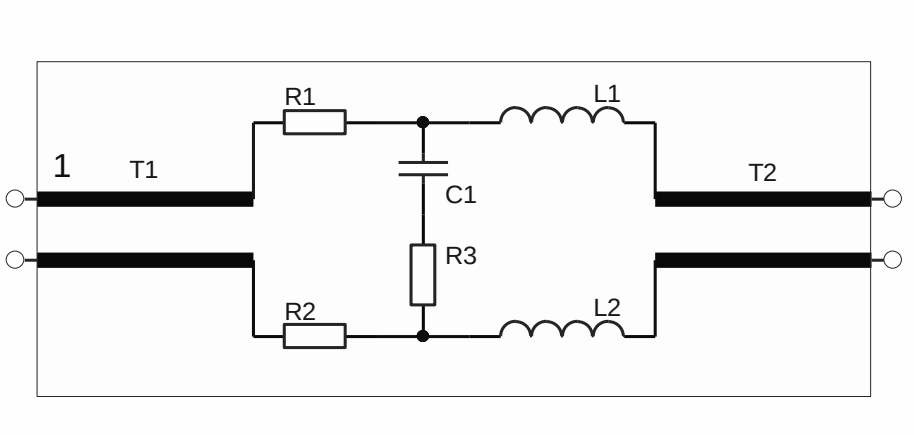


Figure 2 Example for type 1 channel implementation - Topology

Part	Description	Type
ECU connector	2 pin MQS connector or equivalent	-
Segment 1	0.5 m cable	FLKCUMGU9Y-9Y 2x0.13QMM-T105 / Krocar 64996795 or equivalent Jacket cables are recommended due to mechanical stability
Filter board	RLC filter board with line impedance compensation	see Figure 3
Segment 2	3.5 m cable	Same as segment 1
Filter board	RLC filter board with line impedance compensation	see Figure 3
Segment 3	5.0 m cable	Same as segment 1
Filter board	RLC filter board with line impedance compensation	see Figure 3
Segment 4	4.5 m cable	Same as segment 1
Filter board	RLC filter board with line impedance compensation	see Figure 3
Segment 2	1.5 m cable	Same as segment 1
ECU connector	2 pin MQS connector or equivalent	-

Table 6: Example for type1 channel implementation - Parts



Legend:

R1, R1:	1Ω (± 1%)
R3:	100Ω (± 1%)
C1:	4.7pF (± 5%)
L1, L2:	27nH (± 2%)
T1:	matched line 25mm length, $Z_{differential}$ = 80Ω (±5%)
T2:	matched line 25mm length, $Z_{differential}$ = 50Ω (±5%)

Figure 3 Example for type1 channel implementation – Filter board

9.3 Channel Type 2

9.3.1 General

The type 2 channel is derived from a 5.0 m link segment scaled from the type 1 cable.

9.3.2 Required Parameters

The parameter and limits given in Table 7 are defined for a type 2 channel implementation.

Parameter	Sub clause [IEEE1]	Lower Limit	Upper Limit
CIDM	IEEE 802.3bw, 96.7.1.1	95 Ω	110 Ω
IL	IEEE 802.3bw, 96.7.1.2	1 MHz: 0.08 dB 10 MHz: 0.36 dB 33 MHz: 0.70 dB 66 MHz: 1.00 dB	1 MHz: 0.25 dB 10 MHz: 0.65 dB 33 MHz: 1.10 dB 66 MHz: 1.60 dB
RL)$_1$	IEEE 802.3bw, 96.7.1.3	1 MHz: 25.0 dB 66 MHz: 25.0 dB	
Propagation delay)$_1$	-	2 MHz: 25.0 ns 66 MHz: 25.0 ns 66 MHz: 25.0 ns	2 MHz: 30.0 ns 66 MHz: 28.5 ns 66 MHz: 28.5 ns

)$_1$ measurement of propagation delay according to [16]

Table 7: Required parameter and limits for type 2 channel.

9.3.3 Example for Type 2 Channel implementation

The description of each part of this implementation is given in Table 8.

Part	Description	Type
ECU connector	2 pin MQS connector or equivalent	-
Segment 1	5.0 m cable	FLKCUMGU9Y-9Y 2x0.13QMM-T105 / Krocar 64996795 or equivalent Jacket cables are recommended due to mechanical stability
ECU connector	2 pin MQS connector or equivalent	-

Table 8: Example for type2 channel implementation - Parts

9.4 Channel Type 3

9.4.1 General

The Type 3 channel is derived from a 1.5m link segment scaled from the type 1 cable.

9.4.2 Required Parameters

The parameter and limits given in Table 9 are defined for a type 3 channel implementation.

Parameter	Sub clause [IEEE1]	Lower Limit	Upper Limit
CIDM	IEEE 802.3bw, 96.7.1.1	95 Ω	105 Ω
IL	IEEE 802.3bw, 96.7.1.2	1 MHz: 0.03 dB 10 MHz: 0.12 dB 33 MHz: 0.23 dB 66 MHz: 0.33 dB	1 MHz: 0.10 dB 10 MHz: 0.20 dB 33 MHz: 0.35 dB 66 MHz: 0.50 dB
RL)$_1$	IEEE 802.3bw, 96.7.1.3	1 MHz: 30.0 dB 66 MHz: 30.0 dB	
Propagation delay)$_1$	-	2 MHz: 7.5 ns 66 MHz: 7.5 ns 66 MHz: 7.5 ns	2 MHz: 10.5 ns 66 MHz: 8.5 ns 66 MHz: 8.5 ns

)$_1$ measurement of propagation delay according to [16]

Table 9: Required parameter and limits for type 3 channel

9.4.3 Example for Type 3 channel implementation

The description of each part of this implementation is given in Table 10.

Part	Description	Type
ECU connector	2 pin MQS connector or equivalent	-
Segment 1	1.5 m cable	FLKCUMGU9Y-9Y 2x0.13QMM-T105 / Krocar 64996795 or equivalent Jacket cables are recommended due to mechanical stability
ECU connector	2 pin MQS connector or equivalent	-

Table 10: Example for type3 channel implementation - Parts

10 Appendix: Test documentation examples

10.1 Test configuration documentation example

Item	Type	Source	Comment
DUT	PHY -0815 -Test board	Fa. Hell-COM	
Cable	0.35 PP	Longwire&Copper.com	
Transceiver	80-0815	Hell-COM	100BaseT1;
Layout		App-Note AN-12345	Hell-Com.com\Ap_Note.. 24.12.2017
Script	100Base Operation	Script	Hell-Com.com\Ap_Note\Sript\100Base_operation_V.01 22.3.2018
L1	ABG-8147	General Inductors	200µH
R1, R2	1K	Best_Ohm AG, Serie 4711, 0805	100V
C1, C2	100nF		

Table 11: Example for test circuitry documentation

10.2 DUT feature documentation example

DUT Feature	YES	NO	Comment
TEST Mode 1	x		
TEST Mode 2	x		
..		x	See Deactivated short
TEST Mode 6	x		
TEST Mode 7	x		
Deactive signal front end / termination on		x	Allow termination, if.. (explain what to do or why there is an exception..
Ready Status Register		x	Check ..xyz AND abc instead
..			
Detect short		x	Not in this silicon
..			
CRC / symbol failures	x		
..			
Polarity detect		x	Not in this silicon

Table 12: Example for feature availability documentation