# 1000BASE-T1 Interoperability Test Suite

# Interoperability Test Suite Specification



Author & Company David Bollati - C&S Group GmbH			
Title 1000BASE-T1 Interoperability Test Suite			
Version	1.9		
Date	December 3, 2024		
Status	Final		
Restriction Level	Public		

1000BASE-T1 Interoperability Test Suite. This document aims to be a guide to implement and carry out the necessary procedures to test the grade of interoperability between devices with 1000BASET1 capabilities.

#### **Version Control of Document**

Version	Author	Description	Date	
0.1	C&S Group	First draft	05/10/16	
0.2	C&S Group	Second Draft	15/02/17	
0.3	C&S Group	Third draft	13/03/17	
0.4	C&S Group	Fourth draft	20/03/17	
0.5	C&S Group	Fifth draft	27/03/17	
0.6	C&S Group	Sixth draft	10/05/17	
0.7	C&S Group	Seventh draft	01/08/17	
0.8	C&S Group	Eighth draft	19/09/17	
0.9	C&S Group	Ninth draft	11/10/17	
0.91	C&S Group	Tenth draft	13/11/17	
1.0	C&S Group	Release candidate	12/12/17	
1.1	C&S Group	Draft	07/12/18	
1.2	C&S Group	Draft – Change document restriction	03/04/19	
1.3	C&S Group	Draft	29/05/19	
1.4	C&S Group	Draft	07/10/20	
1.5	C&S Group	Draft	22/04/21	
1.6	C&S Group	Draft	30/06/21	
1.7	C&S Group	Draft	02/02/22	
1.7.1	N. Wienckowski (GM)	Draft - updated Disclaimer	04/20/22	
1.8	C&S Group	Change Restriction, version, and date for	09/15/22	
	·	publication		
1.8.1	C&S Group	Change version and date for publication	07/03/23	
1.8.2	C&S Group			
1.9	C&S Group	•		
		version, and date for publication		

#### **Restriction level history of Document**

Version	Restriction Level	Description	Date
0.1	OPEN Technical First Draft Members only		05/10/16
0.2	OPEN Technical Members only	Second Draft, covering most of the feedback	15/02/17
0.3	OPEN Technical Members only	Third Draft, covering further new feedback	10/03/17
0.5	OPEN Technical Members only	Fifth Draft, covering further new feedback	27/03/17
0.6	OPEN Technical Members only	Sixth Draft, covering further new feedback	10/05/17
0.7	OPEN Technical Members only	Seventh Draft, covering further new feedback	01/08/17
0.8	OPEN Technical Members only	Eighth Draft, covering further new feedback and new disclaimer	19/09/17
0.9	OPEN Technical Members only	Ninth Draft, new appendix including the channel requirements created by the subgroup	11/10/17
0.91	OPEN Technical Members only	Tenth Draft, new collected feedback	13/11/17
1.0	OPEN Technical Members only	Update in the definitions of test channels A.1 to A.3	12/12/17
1.1	OPEN Technical Members only	Draft – remove Channel Types description and add references to the respective section in the System Implementation Specification	07/12/18
1.2	OPEN Members only Change document restriction		03/04/19
1.3	OPEN Technical Members only	Draft – first corrections upon issues found during early testing and consideration of mandatory features as defined in Advanced diagnostic features for 1000BASE-T1	29/05/19
1.4	OPEN Technical Members only	IOPT_16, before starts frame transmission wait for <i>Comm_ready</i> [ <i>loc_phy_ready</i> and <i>rem_phy_ready</i> ] condition instead of link-up condition	07/10/20
1.5	OPEN Technical Members only	Including respective chapters for wake-up/sleep interoperability test cases as well as appendix for exemplar xMII/MDIO Interface for PHY Boards used for testing purposes	22/04/21
1.6	OPEN Technical Members only	Updated Wake-up/Sleep chapter	30/06/21
1.7	OPEN Technical Members only	Added references to TC10 Wake-up/Sleep specification. Updated revisions of several referenced specifications.	02/02/22
1.7.1	OPEN Members Only Document for IP Review with updated Disclaimer		04/20/22
1.8	Public		09/15/22
1.8.1	OPEN Members Only Added clarification regarding WAKE_IOP_8		07/03/23
1.8.2			13/02/24
1.9	Public	Update declaimer, change restriction level, version, and date for publication	03/12/24

# Contents

1	OPEN	I Alliance Specification Copyright Notice and Disclaimer	7
	1.1	OPEN Specification Ownership and Usage Rights	7
	1.2	Rights and Usage Restrictions Specific to OPEN Alliance Members	7
	1.2.1	Rights and Usage Restrictions Specific to Non-members of OPEN Alliance	7
	1.3	Terms Applicable to both Members and Non-members of OPEN Alliance	8
	1.3.1	Patents, Trademarks, and other Rights:	8
	1.3.2	Disclaimers and Limitations of Liability:	8
	1.3.3	Compliance with Laws and Regulations:	8
	1.3.4	Automotive Applications Only:	9
	1.3.5	Right to Withdraw or Modify:	9
2	Intro	duction	10
	2.1	Overview	10
	2.2	Normative References	11
	2.3	Abbreviations and definitions	12
	2.4	Organization of Tests	16
	2.4.1	Elementary test structure	16
	2.4.2	Test case instances structure	17
3	Laye	1 Interoperability	
	3.1	General Requirements	
	3.2	Test coverage / variation points	20
	3.3	Channels definition	21
	3.3.1	Channel Type A.1	21
	3.3.2	Channel Type A.2	21
	3.3.3	Channel Type A.3	21
	3.4	Multiple Link Partners	22
4	Inter	operability Test Cases	24
	4.1	Group 1, Link status	24
	4.1.1	Reliability of indicated link status directly after link-up / PHY reset	24
	4.1.2 MAS	Reliability of indicated link status when connected to link partner with same TER/SLAVE configuration	26

	4.1.3	Revoke of link status after link-down	27
	4.2	Group 2, Link-up	28
	4.2.1	Link-up after PHY-reset	28
	4.2.2	Link-up after reset of link partner	
5	1000	BASE-T1 PHY features set tests	32
	5.1	Group 3, Signal Quality	32
	5.1.1	Indicated signal quality for channel with decreasing quality	33
	5.1.2	Indicated signal quality for channel with increasing quality	35
	5.2	Group 4, Cable Diagnosis	37
	5.2.1	Cable diagnostics for error-free channel	37
	5.2.2	Cable diagnostics for near and far end open	
	5.2.3	Cable diagnostics for near and far end short	40
6	Wake	e-up/Sleep	42
	6.1	Group 5, Wake-up reception and signalizing	42
	6.1.1	Reception of a wake-up pulse (WUP)	42
	6.1.2	Reception of a wake-up request (WUR)	44
	6.1.3	Reception of a wake-up pulse (WUP) on an already active DUT	46
	6.2	Group 6, Wake-up transmission	48
	6.2.1	Transmission of a wake-up pulse (WUP)	48
	6.2.2	Transmission of a wake-up pulse after local wake-up (WUP)	50
	6.2.3	Transmission of a wake-up request (WUR)	52
	6.3	Group 7, Wake-up forwarding	54
	6.3.1	Forwarding wake-up request from active to passive link	54
	6.3.2	Forwarding a wake-up request from active to active link	56
	6.3.3	Forwarding a wake-up request from passive to active link	58
	6.3.4	Forwarding a wake-up request from passive to passive link	60
	6.3.5	Forwarding a wake-up request from passive to passive link, DUT in sleep	62
	6.4	Group 8, Sleep	64
	6.4.1	Sleep request after link-up	64
	6.4.2	Remote sleep request after link-up	66
7	Арре	ndix	68
	7.1	Suggested Iterations	68
	7.1.1	Nomenclature	68

7.1.2	Group 1 test cases iterations	69
7.1.3	Group 2 test cases iterations	70
7.1.4	Group 3 test cases iterations	72
7.1.5	Group 4 test cases iterations	72
7.1.6	Group 5 test cases iterations	73
7.1.7	Group 6 test cases iterations	73
7.1.8	Group 7 test cases iterations	74
7.1.9	Group 8 test cases iterations	74
7.2	Artificial degradation of channel quality	75
7.2.1	Description	75
7.3	Exemplar xGMII/SMI Pinout Interface for testing purposes.	76
7.3.1	Connector description	77
7.4	List of tables	78
7.5	List of figures	

# **1** OPEN Alliance Specification Copyright Notice and Disclaimer

# 1.1 OPEN Specification Ownership and Usage Rights

As between OPEN Alliance and OPEN Alliance Members whose contributions were incorporated in this OPEN Specification (the "Contributing Members"), the Contributing Members own the worldwide copyrights in and to their given contributions. Other than the Contributing Members' contributions, OPEN Alliance owns the worldwide copyrights in and to compilation of those contributions forming this OPEN Specification. For OPEN Alliance Members (as that term is defined in the OPEN Alliance Bylaws), OPEN Alliance permits the use of this OPEN Specification on the terms in the OPEN Alliance Intellectual Property Rights Policy and the additional applicable terms below. For non-members of OPEN Alliance, OPEN Alliance permits the use of this OPEN Specification on the terms in the OPEN Alliance Specification License Agreement (available here: http://www.opensig.org/Automotive-Ethernet-Specifications/ )and the additional applicable terms below. The usage permissions referenced and described here relate only to this OPEN Specification. By using this OPEN Specification, you hereby agree to the following terms and usage restrictions:

# **1.2 Rights and Usage Restrictions Specific to OPEN Alliance Members**

FOR OPEN ALLIANCE MEMBERS ONLY: In addition to the usage terms and restrictions granted to Members in the OPEN Alliance Intellectual Property Rights Policy, Members' use of this OPEN Specification is subject this Copyright Notice and Disclaimer. Members of OPEN Alliance have the right to use this OPEN Specification solely (i) during the term of a Member's membership in OPEN Alliance and subject to the Member's continued membership in good standing in OPEN Alliance; (ii) subject to the Member's continued compliance with the OPEN Alliance governance documents, Intellectual Property Rights Policy, and the applicable OPEN Alliance Promoter or Adopter Agreement, as applicable; and (iii) for internal business purposes and solely to use the OPEN Specification for implementation of this OPEN Specification in the Member's products and services, but only so long as Member does not distribute, publish, display, or transfer this OPEN Specification to any third party, except as expressly set forth in Section 11 of the OPEN Alliance Intellectual Property Rights Policy. Except and only to the extent required to use this OPEN Specification internally for implementation of this OPEN Specification in Member's products and services, Member shall not modify, alter, combine, delete portions of, prepare derivative works of, or create derivative works based upon this OPEN Specification. If Member creates any modifications, alterations, or other derivative works of this OPEN Specification as permitted to use the same internally for implementation of this OPEN Specification in Member's products and services, all such modifications, alterations, or other derivative works shall be deemed part of, and licensed to such Member under the same restrictions as, this OPEN Specification. For the avoidance of doubt, Member shall not include all or any portion of this OPEN Specification in any other technical specification or technical material, product manual, marketing material, or any other material without OPEN Alliance's prior written consent. All rights not expressly granted to Member in the OPEN Alliance Intellectual Property Rights Policy are reserved.

#### 1.2.1 Rights and Usage Restrictions Specific to Non-members of OPEN Alliance

FOR NON-MEMBERS OF OPEN ALLIANCE ONLY: Use of this OPEN Specification by anyone who is not a Member in good standing of OPEN Alliance is subject to your agreement to the OPEN Alliance Specification License Agreement (available here: <a href="http://www.opensig.org/Automotive-Ethernet-Specifications/">http://www.opensig.org/Automotive-Ethernet-Specifications/</a> ) and the additional terms in this Copyright Notice and Disclaimer. Non-members have the right to use this OPEN Specification solely (i) subject to the non-member's continued compliance with the OPEN Alliance Specification License Agreement; and (ii) for internal business purposes and solely to use the OPEN Specification for implementation of this OPEN Specification in the non-member's products and services, but only so long as non-member does not distribute, publish, display, or transfer this OPEN Specification to any third party, unless and only to the extent expressly set forth in the OPEN Alliance Specification License Agreement. Except and only to the extent required to use this OPEN Specification internally for implementation of this OPEN Specification in non-member's products and services, non-member shall

not modify, alter, combine, delete portions of, prepare derivative works of, or create derivative works based upon this OPEN Specification. If non-member creates any modifications, alterations, or other derivative works of this OPEN Specification as permitted to use the same internally for implementation of this OPEN Specification in non-member's products and services, all such modifications, alterations, or other derivative works shall be deemed part of, and licensed to such non-member under the same restrictions as, this OPEN Specification. For the avoidance of doubt, non-member shall not include all or any portion of this OPEN Specification in any other technical specification or technical material, product manual, marketing material, or any other material without OPEN Alliance's prior written consent. All rights not expressly granted to non-member in the OPEN Alliance Specification License Agreement are reserved.

# 1.3 Terms Applicable to both Members and Non-members of OPEN Alliance

#### **1.3.1** Patents, Trademarks, and other Rights:

OPEN Alliance has received no Patent Disclosure and Licensing Statements related to this OPEN Specification. Therefore, this OPEN Specification contains no specific disclaimer related to third parties that may require a patent license for their Essential Claims. Having said that, the receipt of this OPEN Specification shall not operate as an assignment of or license under any patent, industrial design, trademark, or other rights as may subsist in or be contained in or reproduced in this OPEN Specification; and the implementation of this OPEN Specification could require such a patent license from a third party. You may not use any OPEN Alliance trademarks or logos without OPEN Alliance's prior written consent.

#### **1.3.2** Disclaimers and Limitations of Liability:

- THIS OPEN SPECIFICATION IS PROVIDED ON AN "AS IS" BASIS, AND ALL REPRESENTATIONS, WARRANTIES, AND GUARANTEES, EITHER EXPLICIT, IMPLIED, STATUTORY, OR OTHERWISE, ARE EXCLUDED AND DISCLAIMED UNLESS (AND THEN ONLY TO THE EXTENT THEY ARE) MANDATORY UNDER LAW. ACCORDINGLY, OPEN ALLIANCE AND THE CONTRIBUTING MEMBERS MAKE NO REPRESENTATIONS OR WARRANTIES OR GUARANTEES WITH REGARD TO THIS OPEN SPECIFICATION OR THE INFORMATION (INCLUDING ANY SOFTWARE) CONTAINED HEREIN. OPEN ALLIANCE AND ALL CONTRIBUTING MEMBERS HEREBY EXPRESSLY DISCLAIM ANY AND ALL SUCH EXPRESS, IMPLIED, STATUTORY, AND ALL OTHER REPRESENTATIONS, WARRANTIES, AND GUARANTEES, INCLUDING WITHOUT LIMITATION ANY AND ALL WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR USE, TITLE, NON-INFRINGEMENT OF OR ABSENCE OF THIRD PARTY RIGHTS, AND/OR VALIDITY OF RIGHTS IN THIS OPEN SPECIFICATION; AND OPEN ALLIANCE AND THE CONTRIBUTING MEMBERS MAKE NO REPRESENTATIONS AS TO THE ACCURACY OR COMPLETENESS OF THIS OPEN SPECIFICATION OR ANY INFORMATION CONTAINED HEREIN. WITHOUT LIMITING THE FOREGOING, OPEN ALLIANCE AND/OR CONTRIBUTING MEMBERS HAS(VE) NO OBLIGATION WHATSOEVER TO INDEMNIFY OR DEFEND YOU AGAINST CLAIMS RELATED TO INFRINGEMENT OR MISAPPROPRIATION OF INTELLECTUAL PROPERTY RIGHTS.
- OPEN ALLIANCE AND CONTRIBUTING MEMBERS ARE NOT, AND SHALL NOT BE, LIABLE FOR ANY LOSSES, COSTS, EXPENSES, OR DAMAGES OF ANY KIND WHATSOEVER (INCLUDING WITHOUT LIMITATION DIRECT, INDIRECT, SPECIAL, INCIDENTAL, CONSEQUENTIAL, PUNITIVE, AND/OR EXEMPLARY DAMAGES) ARISING IN ANY WAY OUT OF USE OR RELIANCE UPON THIS OPEN SPECIFICATION OR ANY INFORMATION HEREIN. NOTHING IN THIS DOCUMENT OPERATES TO LIMIT OR EXCLUDE ANY LIABILITY FOR FRAUD OR ANY OTHER LIABILITY WHICH IS NOT PERMITTED TO BE EXCLUDED OR LIMITED BY OPERATION OF LAW.

#### **1.3.3 Compliance with Laws and Regulations:**

NOTHING IN THIS DOCUMENT OBLIGATES OPEN ALLIANCE OR CONTRIBUTING MEMBERS TO PROVIDE YOU WITH SUPPORT FOR, OR RELATED TO, THIS OPEN SPECIFICATION OR ANY IMPLEMENTED PRODUCTS OR SERVICES. NOTHING IN THIS OPEN SPECIFICATION CREATES ANY WARRANTIES OR GUARANTEES, EITHER EXPRESS OR IMPLIED, STATUTORY OR OTHERWISE, REGARDING ANY LAW OR REGULATION. OPEN ALLIANCE AND CONTRIBUTING MEMBERS EXPRESSLY DISCLAIM ALL LIABILITY, INCLUDING WITHOUT LIMITATION, LIABILITY FOR NONCOMPLIANCE WITH LAWS, RELATING TO USE OF THE OPEN SPECIFICATION OR INFORMATION CONTAINED HEREIN. YOU ARE SOLELY RESPONSIBLE FOR THE COMPLIANCE OF IMPLEMENTED PRODUCTS AND SERVICES WITH ANY SUCH LAWS AND REGULATIONS, AND FOR OBTAINING ANY AND ALL REQUIRED AUTHORIZATIONS, PERMITS, AND/OR LICENSES FOR IMPLEMENTED PRODUCTS AND SERVICES RELATED TO SUCH LAWS AND REGULATIONS WITHIN THE APPLICABLE JURISDICTIONS.

IF YOU INTEND TO USE THIS OPEN SPECIFICATION, YOU SHOULD CONSULT ALL APPLICABLE LAWS AND REGULATIONS. COMPLIANCE WITH THE PROVISIONS OF THIS OPEN SPECIFICATION DOES NOT CONSTITUTE COMPLIANCE TO ANY APPLICABLE LEGAL OR REGULATORY REQUIREMENTS. IMPLEMENTERS OF THIS OPEN SPECIFICATION ARE SOLELY RESPONSIBLE FOR OBSERVING AND COMPLYING WITH THE APPLICABLE LEGAL AND REGULATORY REQUIREMENTS. WITHOUT LIMITING THE FOREGOING, YOU SHALL NOT USE, RELEASE, TRANSFER, IMPORT, EXPORT, AND/OR RE-EXPORT THIS OPEN SPECIFICATION OR ANY INFORMATION CONTAINED HEREIN IN ANY MANNER PROHIBITED UNDER ANY APPLICABLE LAWS AND/OR REGULATIONS, INCLUDING WITHOUT LIMITATION U.S. EXPORT CONTROL LAWS.

#### **1.3.4 Automotive Applications Only:**

Without limiting the foregoing disclaimers or limitations of liability in any way, this OPEN Specification was developed for automotive applications only. This OPEN Specification has neither been developed, nor tested for, non-automotive applications.

#### **1.3.5** Right to Withdraw or Modify:

OPEN Alliance reserves the right to (but is not obligated to) withdraw, modify, or replace this OPEN Specification at any time, without notice.

© 2024 OPEN Alliance. This document also contains contents, the copyrights of which are owned by third parties who are OPEN Alliance Contributing Members. Unauthorized Use Strictly Prohibited. All Rights Reserved.

# 2 Introduction

# 2.1 Overview

The goal of this document is to define a set of tests that on one hand ensure interoperability between multiple devices that use 1000BASE-T1 capable PHYs. In particular, this requires each PHY to be able to establish a stable link within a given time limit, to be able to reliably monitor and signal the current link status to an upper layer and to be able to transmit data with an upper bit error rate limit.

Being in line with [9], following options are not considered within the framework of this specification:

- Communication systems using Power over data line (PoDL) or system implementation using STP cables.
- Energy efficiency functionalities of 1000BASE-T1 PHYs.
- Topics related with transmission speed change from 1Gb/s to 100Mb/s or vice versa are out of the scope of this document. If Auto-Negotiation is supported by the DUT, this option must be disabled.

Furthermore, on the other hand, this document addresses a set of test cases that verify the reliability of important supported features of an automotive Ethernet PHY (often also called transceiver), e.g. for diagnostic purposes for automotive Ethernet PHY's. In particular, signal quality index (SQI) and harness defects detection.

This document shall provide all the necessary technical aspects and detail descriptions in order to guarantee that the same outcome from test cases will be obtained even when running the test suite in different test systems, provided that the particular test suite and the test system are compliant to the content of this document.

Note: The tests do not solely cover the respective PHYs, but also take into account PHY configuration and an external filter, if applicable. The results of the Interoperability Test Suite will not only depend on the PHY, but also on the general configuration of implementation under test; the Link Partner, the chokes and the communication channel conditions.

#### 2.2 Normative References

- [1] IEEE P802.3bp<sup>™</sup>: Physical Layer Specifications and Management Parameters for 1 Gb/s Operation over a Single Twisted Pair Copper Cable
- [2] IEEE P802.3bw<sup>™</sup> Physical Layer Specifications and Management Parameters for 100 Mb/s Operation over a Single Balanced Twisted Pair Cable (100BASE-T1)
- [3] IEEE P802.3-2015 IEEE Standard for Ethernet
- [4] OPEN ALLIANCE: 1000BASE-T1 PHY Control Test Suite Revision 1.0
- [5] OPEN ALLIANCE: 1000BASE-T1 Physical Media Attachment Test Suite Revision 1.3
- [6] OPEN ALLIANCE: 1000BASE-T1 Physical Coding Sublayer Test Suite Revision 1.0
- [7] OPEN ALLIANCE: 1000BASE-T1 EMC Measurement Specification for Transceivers Revision 2.1
- [8] OPEN ALLIANCE: 1000BASE-T1 EMC Test Specification for Common Mode Chokes Revision 2.0
- [9] OPEN ALLIANCE: 1000BASE-T1 System Implementation Specification Revision 1.6
- [10] OPEN ALLIANCE: Advanced diagnostic features for 1000BASE-T1 automotive Ethernet PHYs Revision 2.2
- [11] OPEN ALLIANCE: Sleep/Wake-up Specification Revision 1.0
- [12] OPEN ALLIANCE: Channel and Components Requirements for 1000BASE-T1 Link Segment Type A (UTP) – Revision 2.3

# 2.3 Abbreviations and definitions

ID: 1000BASET1\_L1\_IOP\_1

Type: Information

Abbreviation	Glossary term	Glossary definition		
CRC	Cyclic Redundancy Check			
ISO/OSI		Layer model of communication systems		
MAC Media Access Control		Abbreviation for the sub layer of the data link layer (layer 2) of the OSI model or for the physical device that implements the Media Access Control functions.		
MDI	Media dependent interface			
РНҮ	Physical Layer	Abbreviation for the physical layer (layer 1) of the OSI model or for the device that implements layer 1 of the OSI model.		
DUT	Device under test	Combination of PHY, PHY configuration and filter that is being tested.		
LP	Link partner	see list of definitions (1000BASET1_L1_IOP_2).		
ETH_N		Negative MDI pin or cable connected to a PHY's negative MDI pin.		
ETH_P		Positive MDI pin or cable connected to a PHY's positive MDI pin.		
SQI	Signal quality indicator	The PHY's estimated signal quality of the channel or a comparable value from which a quality indicator for the communication channel can be derived.		
CIDM	Characteristic Impedance Differential Mode			
IL	Insertion Loss			
RL	Return Loss			
ΟΑΜ	Operations, Administration and Management	As defined in IEEE 802.3bp [1]		

Abbreviation	Glossary term	Glossary definition
tO	Timer	A timer which counts upwards from zero for measuring elapsed time.
		In test case IOP_19, the timer t0 is incremented until the DUT's PHY indicated link status changes from link-up to link-drop.
		In test cases IOP_20 and IOP_21, the timer t0 is incremented until the DUT's PHY indicates an active link

Table 1: List of Abbreviations.

# ID: 1000BASET1\_L1\_IOP\_2

#### Type: Information

Glossary term	Glossary definition		
ΜΑΥ	This word or the adjective "OPTIONAL", mean that an item is truly optional. One vendor may choose to include the item because a particular marketplace requires it or because the vendor feels that it enhances the product while another vendor may omit the same item. An implementation which does not include a particular option MUST be prepared to interoperate with another implementation which does include the option, though perhaps with reduced functionality. In the same way an implementation which does include a particular option MUST be prepared to interoperate with another implementation which does not include the option (except, or course, for the feature the option provides.)		
MUST	This word, or the terms "REQUIRED" or "SHALL", mean that the definition is an absolute requirement of the specification.		
MUST NOT	This phrase or the phrase "SHALL NOT", mean that the definition is an absolute prohibition of the specification.		
SHOULD	This word, or the adjective "RECOMMENDED", mean that there may exist valid reasons in particular circumstances to ignore a particular item, but the full implications must be understood and carefully weighed before choosing a different course.		
SHOULD NOT	This phrase, or the phrase "NOT RECOMMENDED" mean that there may exist valid reasons in particular circumstances when the particular behavior is acceptable or even useful, but the full implications should be understood and the case carefully weighed before implementing any behavior described with this label.		
Link status	The link state that is indicated via a PHY's status registers. The link state can be a combination of various PHY status bits.		
Link partner	Device that is connected to a Device under Test to perform the interoperability tests. A link partner must use a well-known PHY, PHY configuration and external PHY filter (if necessary).		
External PHY filter or external filter.	Additional circuit that is connected directly to the PHY and filters the in- and outgoing physical layer signaling. The PHY vendor typically provides a reference filter design.		

Glossary term	Glossary definition	
PHY configuration	Variable settings that affect the PHY's behavior (e.g., sensitivity of internal equalizers, or shaping of outgoing physical layer signaling). The PHY configuration could be set by an upper layer (e.g., by software) or could be hardcoded, e.g., via dedicated PHY configuration pins.	
Test case	Description of one or more test steps and a set of conditions that define whether the observed behavior when executing the test steps matches the expected results.	
Test iteration	The execution of all test steps of a given test case.	
Test instance	A test instance defines different test parameters for a given test case, such as the DUT's PHY MASTER/SLAVE configuration, or used cable to connect the link partner. The test case itself is not altered.	
Soft reset	Reset of a PHY by software, usually triggered by writing to a control register.	
Hard reset	Reset of a PHY via a dedicated reset-pin, or by toggling the PHYs power supply.	
Channel	nnel Synonym for physical layer communication channel (see [4])	

Table 2: List of Definitions.

# **2.4 Organization of Tests**

In this chapter the main structure of the test cases as well as the elementary test cases structure will be introduced.

#### 2.4.1 Elementary test structure

The main structure description of a test case is shown in Table 3. A brief description about the meaning of each field is provided.

Synopsis	A short description of the purpose of the test case is given here.			
Prerequisites	A list of requirements and capabilities needed for a proper test conduction			
Test Setup	The respective test environment setup is specified (e.g. if different test case sequences will require different test system configuration)			
Test procedure	The first note here describes the total sum of test case executions due to setup variations to give the test implementer a first impression of the specific test case. As the second part of the test case execution, the test steps are described dealing with the setup being applied and what is observed and measured at each execution etc. All actions of the test environment shall be described explicitly in this item.			
Pass criteria	In this response cell, a description is given about what is expected as the result. The Pass criteria are also specified in this point.			
Test iterations	Amount of test repetitions. See Appendix - 7.1 Suggested Iterations			
Notes	When necessary a note will be added complementing the information of the test case.			

 Table 3 - Main test structure

#### 2.4.2 Test case instances structure

Together with the test definition and all its parameters, the test case instances will also be defined that are part of each test case.

A test case instance can be defined as a repetition of the same test case modifying certain configurations of the DUT and the test environment without losing focus on the test purpose.

Instan ce Test Case #		Parameter 1	Parameter 2	Parameter 3		Parameter N
	Parameter A	1000BASET1_ IOP_X			:	
	Parameter B		1000BASET1_ IOP_Y			
	•••					
	Parameter Z			1000BASET1_ IOP_Z		

Table 4 - Te	st case instanc	es definition
--------------	-----------------	---------------

An example definition of a test case is shown in Table 5. In this case, first the behavior of the DUT will be tested when acting as a MASTER with the conditions established by the corresponding test case. Next, the test will be performed with the DUT acting as a SLAVE.

Instance Test Case #	DUT / LP configuration	LP as SLAVE	LP as MASTER
X.X.X.#	DUT as MASTER	1000BASET1_ IOP_XX_SR_M_S	
X.X.X.#	DUT as SLAVE		1000BASET1_ IOP_XX_SR_S_M

 Table 5 - Example of test case instances

# 3 Layer 1 Interoperability

#### 3.1 General Requirements

#### ID: 1000BASET1\_L1\_IOP\_3

*Type:* Information

A Device under Test (DUT) consists of the PHY (identified by its manufacturer, model and revision number), the external filter (if required by the PHY vendor) and PHY configuration.

#### ID: 1000BASET1\_L1\_IOP\_4

#### Type: Requirement

The PCB layout of the DUT shall adhere to PHY vendor's reference design. In particular, this includes schematic and specific parts installed, power supply, power decoupling and interface between the PHY and microcontroller.

#### ID: 1000BASET1\_L1\_IOP\_5

#### Type: Requirement

The PHY configuration and software interface used for the IOP tests shall adhere to the specification of the PHY vendor. This requires the PHY vendor to define which registers shall be used, e.g., to evaluate the PHY's link status or estimated signal quality.

Only if PHY is configured according to available datasheet and application notes a "PASS" shall be noted (and the used versions shall be documented). If further register changes are made, a "PASS with REMARK" shall be noted, including the description of what is changed in the registers.

#### ID: 1000BASET1\_L1\_IOP\_6

#### Type: Requirement

All monitoring activities (e.g. register readout for active link) shall be done by an interrupt or periodic polling. To ensure valid results, the polling period must be chosen according to the timing requirements of the test case (e.g., much lower than the timing requirement).

#### *ID:* 1000BASET1\_L1\_IOP\_7

#### Type: Requirement

For all Layer 1 Interoperability test cases defined in chapter 3, the DUT shall be tested against a defined set of link partners, unless explicitly defined otherwise in the test case description. A link partner is defined by the same requirements that apply to the DUT. If multiple qualified link partners are available, the test against multiple link partners is mandatory

#### ID: 1000BASET1\_L1\_IOP\_8

#### Type: Requirement

For all PHY feature set tests defined in chapter 5, the DUT must be tested against a known link partner. The link partner is defined by the same requirements that apply to the DUT. The link partner configuration must be included in the test results. Tests against additional link partners are optional.

#### *ID:* 1000BASET1\_L1\_IOP\_9

#### Type: Requirement

For each test case, the test results shall be documented individually for each combination of DUT and link partner, for each variation point and for each test instance.

#### *ID:* 1000BASET1\_L1\_IOP\_10

#### Type: Information

The tests do not necessarily aim at qualifying a single DUT, but the combination of DUT and link partner. This also means that if a test fails, not the DUT's PHY, but the combination of DUT and link partner is faulty. Other DUT/link partner combinations might be free from defects and may qualify.

#### *ID:* 1000BASET1\_L1\_IOP\_11

#### Type: Requirement

A link-up condition is defined in terms of the following bits:

- Local receiver status (LRS);
- Remote receiver status (RRS);
- Link status bit (LS)

And the PHY status

• PHY\_Status (send\_data, send\_idle,...) - PCS Status of IEEE 802.3 Fig 40-16a

• Link-up-> (LRS==1 AND RRS==1 AND LS==1) AND PHY\_Status==send\_data

*ID:* 1000BASET1\_L1\_IOP\_12

Type: Requirement

A link down condition is defined in terms of the following bits:

- Local receiver status (LRS);
- Remote receiver status (RRS);
- Link status bit (LS)

Link down-> (LRS==0 or RRS==0 or LS==0)

*ID:* 1000BASET1\_L1\_IOP\_13

Type: Requirement

Auto-Negotiation option must be disabled, if it is supported by the DUT, during the conduction of all test cases defined in this specification.

# **3.2** Test coverage / variation points

*ID*: 1000BASET1\_L1\_IOP\_14

Type: Requirement

The tests shall be performed with channels types as defined in section 3.3.

*ID*: 1000BASET1\_L1\_IOP\_15

Type: Requirement

The tests shall be performed at an ambient temperature of - 40°C, at room temperature and at an ambient temperature of either + 105° C or + 125° C, according to the maximum ambient operating temperature specified in the DUT datasheet.

*ID*: 1000BASET1\_L1\_IOP\_16

Type: Requirement

A test instance of a test case shall be considered as passed, if no test iteration failed. The number of suggested test iterations is defined in chapter 7.1.

# 3.3 Channels definition

This definition shall be used for defining a test wiring harness that simulates various communication channels according to the channel definitions of IEEE Std. 802.3bp [1] for interoperability tests of 1000BASE-T1 transceivers.

#### 3.3.1 Channel Type A.1

*ID*: 1000BASET1\_L1\_IOP\_17

Type: Requirement

The parameters of the type A.1 channel are derived from the limit definition for a communication channel according to [1] and [12]. For setting up a real test harness upper and lower limits are added for each parameter. The type A.1 channel implementation shall fulfill these limits at  $(23\pm2)^{\circ}$ C ambient temperature (RT = Room Temperature).

**NOTE**: For cable type reference, *within the body* of this document: "Type A.1" cable refers to automotive grade unshielded twisted pair (UTP) cable, with jacketing considered as a requirement for 1000BASE-T1 Ethernet.

The parameter and limits are defined in section 8.2 of [9].

#### **3.3.2** Channel Type A.2

*ID*: 1000BASET1\_L1\_IOP\_18

*Type*: Requirement

The Type A.2 channel is derived from a **5m** link segment scaled from the type A.1 cable.

The parameter and limits are defined in section 8.3 of [9].

#### 3.3.3 Channel Type A.3

*ID*: 1000BASET1\_L1\_IOP\_19

Type: Requirement

The Type A.3 channel is derived from a **1.5m** link segment scaled from the type A.1 cable.

The parameter and limits are defined in section 8.4 of [9].

## 3.4 Multiple Link Partners

This section describes a concept to adopt multiple link partners, increasing the coverage in terms of diversity of interoperability in the ecosystem without necessarily increasing the test periods and efforts.

#### *ID:* 1000BASET1\_L1\_IOP\_20

Type: Requirement

Each device having passed the tests listed below could be considered as potential link partner candidate

- a) Conformance Tests
  - 1. OA- PHY Control Test Suite
  - 2. OA- Physical Media Attachment Test Suite
  - 3. OA- Physical Coding Sub-layer Test Suite
- b) Interoperability Tests
  - 1. OA- Interoperability Test Suite At least all test cases in groups #1 and # 2; disregarding the *PHY features set tests* chapter (SQI + Diagnostic)

#### *ID:* 1000BASET1\_L1\_IOP\_21

Type: Requirement

The respective silicon vendors should provide enough samples to be placed in the test system as link partners

#### ID: 1000BASET1\_L1\_IOP\_22

Type: Requirement

Following information will be logged during the test execution with a resolution of up to 1ms between each signal change:

- Link-up
- loc\_rcvr\_status
- rem\_rcvr\_status
- PCS Status of IEEE 802.3 (Fig 40-16a)

This information shall be available with no restrictions from LP and DUT side in order to provide additional information when a failure is observed.

#### ID: 1000BASET1\_L1\_IOP\_23

Type: Requirement

The respective silicon vendors must commit to provide support if interoperability issues are identified and the root cause is unclear for their part to be considered as a link partner for this testing.

ID: 1000BASET1\_L1\_IOP\_24

Type: Requirement

A matrix with all LP combination shall be added at the beginning of the report document with a Pass / Fail for each combinations.

# 4 Interoperability Test Cases

*ID:* 1000BASET1\_L1\_IOP\_25

Type: Requirement

The test cases defined in this section are mandatory for all 1000BASE-T1 PHYs.

4.1 Group 1, Link status

*ID:* 1000BASET1\_L1\_IOP\_26

*Type:* Information

The test cases defined in this section shall ensure that the PHY signals the correct link state to upper layers. In particular, a PHY must not signal an active link when no data can be transmitted.

#### 4.1.1 Reliability of indicated link status directly after link-up / PHY reset

*ID:* 1000BASET1\_IOP\_16

*Type:* Requirement

Synopsis	Shall ensure that the data can be transmitted as soon as the PHY signals an active				
591104313					
	link.				
Droroquisitos	1. DUT with the capability to reset and configure its PHY.				
Prerequisites					
	<ol> <li>DUT must be able to detect a link-up within 1ms after the PHY indicates an active link via its status registers.</li> </ol>				
	3. DUT must be able to send frames, for that a xMII interface must be available on the DUT:				
	<ul> <li>a. if Comm_ready is supported (see [10]) within 1ms after comm ready status is met, otherwise</li> </ul>				
	b. within 2ms after detecting a link-up				
	and is able to send a new frame each 1ms. This includes any processing time				
	by the DUT's application software and networking stack.				
	<ol> <li>DUT and link partner must be able to detect any lost frames by the networking stack or by the application.</li> </ol>				
	5. DUT and link partner must be able to detect a link down during a test iteration.				
	6. Link partner, or device that is connected to the link partner, must be able to receive all frames sent by the DUT.				
Test Setup	DUT must be connected to an active link partner with opposite MASTER/SLAVE				
	configuration. Depending on the test instance, the link partner is either				
	connected with correct, or with swapped polarity (i.e., DUT ETH_N $\Leftrightarrow$ LP ETH_P				
	and DUT ETH_P⇔ LP ETH_N).				
Test procedure	<ol> <li>Link partner shall be active and ready to receive frames.</li> <li>DUT shall soft reset and reconfigure its PHY.</li> </ol>				

	3. If required by PHY vendor: DUT must wait until PHY has accepted			
	MASTER/SLAVE configuration.			
	4. The DUT's PHY configuration must be finished within 20ms after reset.			
	5. DUT shall set an internal <i>counter</i> variable to 0.			
	6. If supported, DUT shall wait until the PHY indicates a PHY ready status			
	( <i>Comm_ready</i> or <i>loc_phy_ready</i> and <i>rem_phy_ready</i> ) otherwise until			
	indicates an active link (e.g., by polling the link state or by using an			
	interrupt).			
	7. DUT shall send out a frame with the current counter value 1ms after ,			
	Comm_ready condition is met, if it is supported, otherwise 1ms after link-			
	<i>up</i> is met.			
	8. Every subsequent 1ms, the DUT shall increment its counter variable and			
	send out a frame with the new counter.			
	9. Repeat step 8 until the link partner receives the first frame by the DUT or			
	the link goes down.			
	10. The link partner must store the <i>counter</i> value of the first received frame.			
Pass criteria	Each test iteration shall be classified as passed, if all of the following condition(s)			
	are fulfilled:			
	<ul> <li>Link partner receives the first frame sent by DUT (counter == 0).</li> </ul>			
	$\circ$ Link did not go down after test step 5, i.e., link stayed active for the			
	whole iteration.			
Test	See suggested test iterations in Appendix 7.1 Suggested Iterations			
iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations			
Notes	Test instance 1000BASE-T1_IOP_16_SR_S_M_P are mandatory in 1000BASE-T1			
	since automatic polarity detection and correction should be supported when			
	configured as SLAVE.			

#### Table 6: Main test structure of 1000BASET1\_IOP\_16

Instance Test Case #	DUT / LP configuration	LP as SLAVE	LP as MASTER	LP is MASTER, LP connected with swapped polarity of ETH_N and ETH_P
4.1.1.1	DUT as SLAVE		1000BASE- T1_IOP_16 _SR_S_M	
4.1.1.2	DUT as SLAVE			1000BASE-T1_IOP_16 _SR_S_M_P
4.1.1.3	DUT as MASTER	1000BASE- T1_IOP_16 _SR_M_S		

Table 7: Test case instances of 1000BASET1\_IOP\_16

# 4.1.2 Reliability of indicated link status when connected to link partner with same MASTER/SLAVE configuration

#### *ID:* 1000BASET1\_IOP\_17

Type: Requirement

Synopsis	Shall ensure that the PHY does not signal an active link when connected to a link partner with equal MASTER/SLAVE configuration.
Prerequisites	<ol> <li>DUT with the capability to reset and configure its PHY.</li> <li>DUT is able to detect a link-up</li> </ol>
Test Setup	DUT must be connected to an active link partner with equal MASTER/SLAVE configuration.
Test procedure	<ol> <li>Link partner shall be active.</li> <li>DUT shall soft reset and reconfigure its PHY.</li> <li>If required by PHY vendor: DUT must wait until its PHY has accepted MASTER/SLAVE configuration.</li> <li>The DUT's PHY configuration must be finished within 20ms after reset.</li> <li>DUT shall monitor for an indicated link-up for at least 750ms.</li> </ol>
Pass criteria	Each test iteration shall be classified as passed, if all of the following condition(s) are fulfilled: • DUT does not detect a link-up.
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	-

#### Table 8: Main test structure of 1000BASET1\_IOP\_17

Instance Test Case #	DUT / LP configuration	LP as SLAVE	LP as MASTER
4.1.2.1	DUT as SLAVE	1000BASE-T1_ IOP_17 _SR_S_S	
4.1.2.2	DUT as MASTER		1000BASE-T1_ IOP_17 SR M M

Table 9: Test case instances of 1000BASET1\_IOP\_17

#### 4.1.3 Revoke of link status after link-down

*ID:* 1000BASET1\_IOP\_19

Type: Requirement

Synopsis	Shall ensure that the PHY does detect and signal a link down within a given time limit after the link has been interrupted, e.g., by a reset or power-down of the link partner. The DUT must be tested against at least one known link partner. A test against a complete set of link partners is optional. The link partner configuration must be included in the test results.
Prerequisites	<ol> <li>DUT with the capability to reset and configure its PHY.</li> <li>DUT must be able to read the current link status.</li> </ol>
Test Setup	DUT must be connected to an active link partner with opposite MASTER/SLAVE configuration.
Test procedure	<ol> <li>Link partner shall be active.</li> <li>DUT shall soft reset and reconfigure its PHY.</li> <li>If required by PHY vendor: DUT must wait until its PHY has accepted MASTER/SLAVE configuration.</li> <li>The DUT's PHY configuration must be finished within 20ms after reset.</li> <li>Wait until the DUT's PHY signals an active link.</li> <li>Apply in the link partner a permanent hard reset condition and start timer t0.</li> <li>Wait until the DUT's PHY indicated link status changes from link-up to link- down and stop timer t0.</li> </ol>
Pass criteria	<ul> <li>Each test iteration shall be classified as passed, if all of the following condition(s) are fulfilled.</li> <li>DUT detected the link-down within 5ms. (t0 &lt;= 5ms).</li> </ul>
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	-

Table 10: Main test structure of 1000BASET1\_IOP\_19

Instance Test Case #	DUT / LP configuration	LP as SLAVE	LP as MASTER
4.1.3.1	DUT as SLAVE		1000BASE-T1_ IOP_19 _SR_S_M
4.1.3.2	DUT as MASTER	1000BASE-T1_ IOP_19 _SR_M_S	

Table 11: Test case instances of 1000BASET1\_IOP\_19

# 4.2 Group 2, Link-up

ID: 1000BASET1\_L1\_IOP\_27

Type: Information

The test cases defined in this section shall ensure that the PHY is able to establish an active link after reset and reconfiguration of itself, or of the link partner's PHY.

#### 4.2.1 Link-up after PHY-reset

*ID:* 1000BASET1\_IOP\_21

Type: Requirement

Synopsis	Shall ensure that the PHY is able to establish a link after being reset and				
	reconfigured within a given time limit.				
	ů ů				
Prerequisites	1. DUT with the capability to reset and configure its PHY.				
	2. DUT is able to detect a link-up within 0.5ms after the PHY indicates an active				
	link via its status registers.				
Test Setup	DUT is connected to an active link partner with opposite MASTER/SLAVE				
	configuration. Depending on the test instance, the link partner is either				
	connected with correct, or with swapped polarity (i.e., DUT ETH_N $\Leftrightarrow$ LP ETH_P				
	and DUT ETH_P $\Leftrightarrow$ LP ETH_N).				
Test	1. DUT shall soft-/hard reset and reconfigure its PHY.				
procedure	2. The DUT's PHY configuration must be finished within 20ms after reset.				
	3. After finished configuration, the DUT shall start timer t0.				
	4. DUT shall wait until the PHY indicates an active link and stop timer t0.				
	5. If [LQ.LTT] register, as defined in [10], is supported, once PHY indicates an				
	active link read the Linkup Total Time from [LQ.LTT] register; (Icl_rcv AND				
	rem_rcv).				
	6. DUT shall monitor whether the link status remains active for at least				
	750ms after initial link-up.				
Pass criteria	Each test iteration shall be classified as passed, if all of the following condition(s)				
	are fulfilled.				

	<ul> <li>DUT's PHY achieved link-up within 100ms after finished configuration (t0 &lt;= 100ms).</li> <li>If [LQ.LTT] register is supported, the obtained value should be correlated with t0 counted by the test system.</li> <li>Link did not go down after test step 4.</li> </ul>
	Additionally, for the test instances 1000BASE-T1_IOP_21_SR_S_M_P and 1000BASE-T1_IOP_21_HR_S_M_P <ul> <li>DUT indicates swapped polarity is indicated by status register</li> </ul>
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	Test instances 1000BASE-T1_IOP_21_SR_S_M_P and 1000BASE- T1_IOP_21_HR_S_M_P are mandatory in 1000BASE-T1 since automatic polarity detection and correction should be supported when configured as SLAVE.

 Table 12: Main test structure of 1000BASET1\_IOP\_21

Instance Test Case #	DUT / LP configuration	LP as SLAVE	LP as MASTER	LP is MASTER, LP connected with swapped polarity of ETH_N and ETH_P
4.2.1.	DUT is SLAVE; PHY is soft reset		1000BASE-T1_ IOP_21 _SR_S_M	
4.2.1.	DUT is SLAVE; PHY is soft reset			1000BASE-T1_ IOP_21 _SR_S_M_P
4.2.1.	DUT is MASTER PHY is soft reset	1000BASE-T1_ IOP_21 _SR_M_S		
4.2.1.	DUT is SLAVE; PHY is hard reset		1000BASE-T1_ IOP_21 _HR_S_M	
4.2.1.	DUT is SLAVE; PHY is hard reset			1000BASE-T1_ IOP_21 _HR_S_M_P
4.2.1.	DUT is MASTER PHY is hard reset	1000BASE-T1_ IOP_21 _HR_M_S		

Table 13: Test case instances of 1000BASET1\_IOP\_21

# 4.2.2 Link-up after reset of link partner

*ID:* 1000BASET1\_IOP\_22

Type: Requirement

Synopsis	Shall ensure that the PHY is able to establish a link after the link partner's PHY has been reset and reconfigured within a given time limit.			
Prerequisites	<ol> <li>Link partner with the capability to reset and configure its PHY.</li> <li>DUT must be able to trigger the PHY reset of the link partner or must be able to detect the time of the LP's PHY reset.</li> <li>DUT must be able to detect a link-up within 0.5ms after the PHY indicates an active link via its status registers.</li> </ol>			
Test Setup	DUT must be connected to an active link partner with opposite MASTER/SLAVE configuration.			
Test procedure Pass criteria	<ol> <li>DUT shall wait until the PHY indicates an active link.</li> <li>DUT shall trigger a soft-/hard reset of the link partner's PHY or wait until the link partner has reset its PHY.</li> <li>DUT shall start timer t0 directly after the reset of the LP's PHY.</li> <li>The link partner must configure its PHY within 20ms after the reset.</li> <li>DUT must ignore any indicated active links within 25ms after the reset.</li> <li>25ms after LP's reset: DUT shall wait until the PHY indicates an active link and stop timer t0. The lowest possible indicated link-up time can be 25ms, even if the actual link-up was established quicker.</li> <li>DUT shall monitor whether the link status remains active for at least 750ms after initial link-up.</li> <li>Each test iteration shall be classified as passed, if all of the following condition(s) are fulfilled.</li> <li>DUT's PHY reported link-up within 120ms after reset of the LP's PHY (t0 &lt;= 120ms).</li> <li>Link did not go down after test step 5.</li> <li>Additionally, for the test instances 1000BASE-T1_IOP_22_SR_S_M_P and 1000BASE-T1_IOP_22_HR_S_M_P</li> <li>DUT indicates swapped polarity is indicated by status register</li> </ol>			
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations			
Notes	Test instances IOP_22_SR_S_M_P and IOP_22_HR_S_M_P are mandatory in 1000BASE-T1 since automatic polarity detection and correction should be supported when configured as SLAVE.			

 Table 14: Main test structure of 1000BASET1\_IOP\_22

Instance Test Case #	DUT / LP configuration	LP is SLAVE; PHY is soft reset	LP is MASTER; PHY is soft reset	LP is SLAVE; PHY is hard reset	LP is MASTER; PHY is hard reset
4.2.2.	DUT is SLAVE		1000BASE-T1_ IOP_22 _SR_S_M		
4.2.2.	DUT is SLAVE				1000BASE-T1_ IOP_22 _HR_S_M
4.2.2.	DUT is SLAVE, LP connected with swapped polarity of ETH_N and ETH_P		1000BASE-T1_ IOP_22 _SR_S_M_P		
4.2.2.	DUT is SLAVE, LP connected with swapped polarity of ETH_N and ETH_P				1000BASE-T1_ IOP_22 _HR_S_M_P
4.2.2.	DUT is MASTER	1000BASE-T1_ IOP_22 _SR_M_S			
4.2.2.	DUT is MASTER			1000BASE-T1_ IOP_22 _HR_M_S	

Table 15: Test case instances of 1000BASET1\_IOP\_22

# 5 1000BASE-T1 PHY features set tests

*ID*: 1000BASET1\_L1\_IOP\_28

#### *Type*: Information

The test cases defined in this chapter shall ensure that optional PHY features, such as an estimation of the channel quality or cable diagnostics, provide expected and comparable results under known test conditions. If a PHY supports a given feature, the associated test cases are mandatory. Else, the test case shall be ignored.

# 5.1 Group 3, Signal Quality

*ID*: 1000BASET1\_L1\_IOP\_29

*Type*: Information

The tests in this section are only applicable for 1000BASE-T1 PHYs that support an estimation of the signal quality of the communication channel. The signal quality can either be read directly from a PHY register, or may be derived based on one or more PHY register values.

# 5.1.1 Indicated signal quality for channel with decreasing quality

*ID:* 1000BASET1\_IOP\_24a

Type: Requirement

Synopsis	Shall ensure that the PHY's indicated signal quality decreases for a channel with decreasing channel quality.		
Prerequisites	<ol> <li>Test system that allows varying and determining the quality of the communication channel that connects the DUT and LP.</li> <li>DUT must be able to monitor the signal quality indicated by the PHY.</li> </ol>		
Test Setup	DUT must be connected to an active link partner with opposite MASTER/SLAVE configuration. Test setup shall be able to apply artificial noise to communication channel.		
Test procedure	<ol> <li>DUT shall soft reset and reconfigure its PHY.</li> <li>Remove any artificial channel degradation, to ensure that the highest possible signal quality is reached on both the DUT and LP.</li> <li>Measure the PHY's SQI value for at least 100 times. Determine and store the minimum and maximum SQI read values. Store all Forward Error Correction counters and additionally PHY Health (SNR) indicated in OAM read in parallel with the SQI values.</li> <li>Increase artificial noise level by one step, i.e. by 0.1dB Gaussian noise generator output.</li> <li>Repeat steps 3 and 4 for ten additional noise levels after the PHY can no longer establish a link.</li> </ol>		
Pass criteria	<ul> <li>Each test iteration shall be classified as passed, if all of the following condition(s) are fulfilled.</li> <li>SQI value: <ul> <li>Steadily and monotonically decreased by one step each</li> <li>SQI values are only valid if link-up condition is present</li> </ul> </li> <li>Link status <ul> <li>Link-up status remains for SQI values higher than 0</li> <li>Link-up status shall be reached from the highest SQI value that corresponds to a BER&lt;10<sup>-10</sup></li> <li>No link instabilities with intermittently link drops should be observed between SQI values higher than 0.</li> </ul> </li> </ul>		
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations		
Notes	To guarantee comparability of the results, a graphic disclosing SQI value (y-axis) vs. associated noise level on the network [ <i>dB</i> ] (x axis) shall be given in the test report for each test iteration. The noise level seen by the DUT is relevant; this means the noise source level weighed by the coupling factor of the differential directional		

	coupler. To ensure a valid SQI value in each reading, the supplier should provide
	documentation regarding the required wait time between measurements or
	indicate that a new valid SQI value is available to be read.

Table 16: Main test structure of 1000BASET1\_IOP\_24a

Instance Test Case #	DUT / LP configuration	LP is SLAVE; PHY is soft reset	LP is MASTER; PHY is soft reset
5.1.1.	DUT is SLAVE		1000BASE-T1_ IOP_24a _SR_S_M
5.1.1.	DUT is MASTER	1000BASE-T1_ IOP_24a _SR_M_S	

Table 17: Test case instances of 1000BASET1\_IOP\_24a

# 5.1.2 Indicated signal quality for channel with increasing quality

ID: 1000BASET1\_L1\_IOP\_24b

*Type:* Requirement

Synopsis	Shall ensure that the PHY's indicated signal quality increases for a channel with increasing channel quality.			
Prerequisites	<ol> <li>Test system that allows varying and determining the quality of the communication channel that connects the DUT and LP.</li> <li>DUT must be able to monitor the signal quality indicated by the PHY.</li> </ol>			
Test Setup	DUT must be connected to an active link partner with opposite MASTER/SLAVE configuration. Test setup shall be able to apply artificial noise to communication channel.			
Test procedure	<ol> <li>Start with the highest artificial noise channel degradation The DUT's PHY can no longer establish a link.</li> <li>DUT shall soft reset and reconfigure its PHY.</li> <li>Measure the PHY's SQI value at least 100 times. Determine and store the minimum and maximum SQI read values. Store all Forward Error Correction counters and additionally PHY Health (SNR) indicated in OAM read in parallel with the SQI values.</li> <li>Decrease artificial noise by one step, i.e. by 0.1 dB Gaussian noise generator output.</li> <li>Repeat steps 3 and 4 until no artificial noise is applied.</li> </ol>			
Pass criteria	<ul> <li>Each test iteration shall be classified as passed, if all of the following condition(s) are fulfilled.</li> <li>SQI value <ul> <li>Steadily and monotonically increased by one step each</li> <li>SQI values are only valid if link-up condition is present</li> </ul> </li> <li>Link Status <ul> <li>Link-up status remains for SQI values higher than 0.</li> <li>Link-up status shall be reached from the lowest SQI value that corresponds to a BER&lt;10<sup>-10</sup></li> <li>No link instabilities with intermittently link drops should be observed between SQI values higher than 0.</li> </ul> </li> </ul>			
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations			
Notes	To guarantee comparability of the results, a graphic disclosing SQI value (y-axis) vs. associated noise level on the network [ <i>dB</i> ] (x axis) shall be given in the test report for each test iteration. The noise level seen by the DUT is relevant; this means the noise source level weighed by the coupling factor of the differential directional coupler. To ensure a valid SQI value in each reading, the supplier			

	should provide documentation regarding the required wait time between
	measurements or indicate that a new valid SQI value is available to be read.

Table 18: Main test structure of 1000BASET1\_IOP\_24b

Instance Test Case #	DUT / LP configuration	LP is SLAVE	LP is MASTER
5.1.2.1	DUT is SLAVE		1000BASE-T1_ IOP_24b _SR_S_M
5.1.2.2	DUT is MASTER	1000BASE-T1_ IOP_24b _SR_M_S	

Table 19: Test case instances of 1000BASET1\_IOP\_24b

### 5.2 Group 4, Cable Diagnosis

## 5.2.1 Cable diagnostics for error-free channel

### *ID:* 1000BASET1\_IOP\_31

### *Type:* Requirement

Synopsis Prerequisites	<ul> <li>Shall ensure that the PHY's cable diagnostic does not indicate a short or open for an error-free channel.</li> <li>1. DUT must be able to trigger the PHY's cable diagnostic feature.</li> </ul>
	<ol> <li>The link partner shall terminate the channel properly. The link partner should not be transmitting any signal (typically "SEND_Z" or as SLAVE)</li> </ol>
Test Setup	DUT is connected to a properly terminated link partner.
Test procedure	<ol> <li>DUT shall soft reset and reconfigure its PHY.</li> <li>DUT shall start cable diagnostic of its PHY.</li> <li>DUT shall wait until the PHY finished cable diagnostics.</li> <li>DUT shall read out the indicated result.</li> </ol>
Pass criteria	<ul> <li>Each test iteration shall be classified as passed, if all of the following condition(s) are fulfilled.</li> <li>Cable diagnostic reported no errors (i.e., no short / open of the bus lines).</li> </ul>
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	-

#### Table 20: Main test structure of 1000BASET1\_IOP\_31

Instance Test Case #	Error-free Channel
	1000BASE-
5.2.1.	T1_IOP_31_SR_C1S_M
	1000BASE-
5.2.1.	T1_IOP_31_SR_C2S_M

Table 21: Main test structure of 1000BASET1\_IOP\_31

### 5.2.2 Cable diagnostics for near and far end open

*ID:* 1000BASET1\_IOP\_32

Type: Requirement

Synopsis	Shall ensure that the PHY's cable diagnostic reliably detects an open of one or both of the bus lines. The test shall be performed for both a near end open at the connector of the DUT, and for a far end open at the connector of the LP.
Prerequisites	<ol> <li>DUT must be able to trigger the PHY's cable diagnostic feature.</li> <li>The link partner shall terminate the channel properly. The link partner should not be transmitting any signal (typically "SEND_Z" or as SLAVE)</li> </ol>
Test Setup	DUT is connected to a properly terminated link partner. One or both of the bus lines have a near or far end open.
Test procedure	<ol> <li>DUT shall soft reset and reconfigure its PHY.</li> <li>DUT shall start cable diagnostic of its PHY.</li> <li>DUT shall wait until the PHY finished cable diagnostics.</li> <li>DUT shall read out the indicated result.</li> </ol>
Pass criteria	<ul> <li>Each test iteration shall be classified as passed, if all of the following condition(s) are fulfilled.</li> <li>Cable diagnostic reported an open of the bus line(s).</li> <li>The cable fault locations shall be reported starting with a minimum distance of approx. 1 meter, with a resolution of 1 meter</li> </ul>
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	For a near end open, one or both bus lines shall be disconnected directly at the connector of the DUT. For a far end open, one or both bus lines shall be disconnected directly at the connector of the LP.

Table 22: Main test structure of 1000BASET1\_IOP\_32

Instance Test Case #	DUT / LP configuration	Test setup	Open is on ETH_N or ETH_P	Open on both ETH_N and ETH_P
5.2.2.1	DUT is SLAVE	Near-end open (on connector of DUT).	1000BASET1_IOP_32 _SR_C2_O1_NEAR_S_ M	
5.2.2.2	DUT is SLAVE	Near-end open (on connector of DUT).		1000BASET1_IOP_32 _SR_C2_O2_NEAR_S_ M
5.2.2.3	DUT is SLAVE	Far-end open (on connector of LP).	1000BASET1_IOP_32 _SR_C2_O1_FAR_S_M	
5.2.2.4	DUT is SLAVE	Far-end open (on connector of LP).		1000BASET1_IOP_32 _SR_C2_O2_FAR_S_M
5.2.2.5	DUT is MASTER	Near-end open (on connector of DUT).	1000BASET1_IOP_32 _SR_C2_O1_NEAR_M_ 	
5.2.2.6	DUT is MASTER	Near-end open (on connector of DUT).		1000BASET1_IOP_32 _SR_C2_O2_NEAR_M_ S
5.2.2.7	DUT is MASTER	Far-end open (on connector of LP).	1000BASET1_IOP_32 _SR_C2_O1_FAR_M_S	
5.2.2.8	DUT is MASTER	Far-end open (on connector of LP).		1000BASET1_IOP_32 _SR_C2_O2_FAR_M_S

Table 23: Test case instances of 1000BASET1\_IOP\_32

### 5.2.3 Cable diagnostics for near and far end short

#### *ID:* 1000BASET1\_IOP\_33

Type: Requirement

Synopsis	• Shall ensure that the PHY's cable diagnostic reliably detects a short between both bus wires. The test shall be performed for both a near end short at the connector of the DUT, and for a far end short at the connector of the LP.
Prerequisites	<ol> <li>DUT must be able to trigger the PHY's cable diagnostic feature.</li> <li>The link partner shall terminate the channel properly. The link partner should not be transmitting any signal (typically "SEND_Z" or as SLAVE)</li> </ol>
Test Setup	DUT is connected to a properly terminated link partner. The bus lines are connected via a <= 1 Ohm resistor.
Test procedure	<ol> <li>DUT shall soft reset and reconfigure its PHY.</li> <li>DUT shall start cable diagnostic of its PHY.</li> <li>DUT shall wait until the PHY finished cable diagnostics.</li> <li>DUT shall read out the indicated result.</li> </ol>
Pass criteria	<ul> <li>Each test iteration shall be classified as passed, if all of the following condition(s) are fulfilled.</li> <li>Cable diagnostic reported a short between the bus lines.</li> <li>The cable fault locations shall be reported starting with a minimum distance of approx. 1 meter, with a resolution of 1 meter</li> </ul>
Test iterations	See suggested test iterations in Appendix – 7.1 Suggested Iterations
Notes	For a near end short, both bus lines shall be connected via a <= 1 Ohm resistor directly at the connector of the DUT. For a far end short, both bus lines shall be connected via a <= 1 Ohm resistor directly at the connector of the LP.

Table 24: Main test structure of 1000BASET1\_IOP\_33

Instance Test Case #	DUT / LP configuration	Test setup	SHORT on both ETH_N and ETH_P
5.2.3.1	DUT is SLAVE	Near-end short (on connector of DUT).	1000BASET1_IOP_33 _SR_C2_S2_NEAR_S_M
5.2.3.2	DUT is SLAVE	Far-end short (on connector of LP).	1000BASET1_IOP_33 _SR_C2_S2_FAR_S_M
5.2.3.3	DUT is SLAVE	Near-end short (on connector of DUT).	1000BASET1_IOP_33 _SR_C2_S2_NEAR_GND_S_ M
5.2.3.4	DUT is SLAVE	Far-end short (on connector of LP).	1000BASET1_IOP_33 _SR_C2_S2_FAR_GND_S_M
5.2.3.5	DUT is SLAVE	Near-end short (on connector of DUT).	1000BASET1_IOP_33 _SR_C2_S2_NEAR_VBAT_S_ M
5.2.3.6	DUT is SLAVE	Far-end short (on connector of LP).	1000BASET1_IOP_33 _SR_C2_S2_FAR_VBAT_S_M
5.2.3.7	DUT is MASTER	Near-end short (on connector of DUT).	1000BASET1_IOP_33 _SR_C2_S2_NEAR_M_S
5.2.3.8	DUT is MASTER	Far-end short (on connector of LP).	1000BASET1_IOP_33 _SR_C2_S2_FAR_M_S
5.2.3.9	DUT is MASTER	Near-end short (on connector of DUT).	1000BASET1_IOP_33 _SR_C2_S2_NEAR_GND_M_ S
5.2.3.10	DUT is MASTER	Far-end short (on connector of LP).	1000BASET1_IOP_33 _SR_C2_S2_FAR_GND_M_S
5.2.3.11	DUT is MASTER	Near-end short (on connector of DUT).	1000BASET1_IOP_33 _SR_C2_S2_NEAR_VBAT_M_ S
5.2.3.12	DUT is MASTER	Far-end short (on connector of LP).	1000BASET1_IOP_33 _SR_C2_S2_FAR_VBAT_M_S

Table 25: Test case instances of 1000BASET1\_IOP\_33

### 6 Wake-up/Sleep

ID: WAKE\_IOP\_1

Type: Requirement

The test cases defined in this section except WAKE\_IOP\_8 are mandatory for all 1000BASE-T1 devices supporting the wake-up/sleep functionality defined in [11]. WAKE\_IOP\_8 is mandatory if the PHY supporting wakeup and sleep signaling over dedicated I/O pins.

# 6.1 Group 5, Wake-up reception and signalizing *ID:* WAKE\_IOP\_2

Type: Information

The test cases defined in this section shall ensure that a wake-up (WUP/WUR) can be received and signalized to the upper layer as described in [11].

## 6.1.1 Reception of a wake-up pulse (WUP)

ID: WAKE\_IOP\_3

Synopsis	Shall ensure that a DUT is able to receive a WUP over a passive link, signalize the		
Synopsis			
	wake-up event and upon this to establish a link within an expected time.		
	Parameters to be measured:		
	• t_wkp_unpwrd: Time between wake-up request on the LP and DUT wake- up signalization.		
	• t wkp link-up: Time between DUT wake-up signalization and link-up.		
	<ul> <li>Link stability after a wake-up condition.</li> </ul>		
Prerequisites	1. DUT with the capability to reset and configure its PHYs.		
	<ol> <li>DUT with the capability to set its PHYs into sleep mode.</li> </ol>		
	<ol> <li>Link partner, or device that is connected to the DUT, shall be able to send a</li> </ol>		
	wake-up pulse (WUP).		
	<ol> <li>The test system shall be able of providing time measurement capabilities</li> </ol>		
	synchronized with the test steps events.		
Tables	synchronized with the test steps events.		
Test Setup	DUT DUT_P1 Passive link LP1_P1 LP1		
	<ul> <li>DUT shall be connected to a link partner (LP1) with a passive link with opposite MASTER/SLAVE configuration.</li> <li>DUT shall be in sleep state.</li> <li>LP1 including LP1_P1 shall be powered and connected to the DUT with a passive link.</li> </ul>		

Test	1. Reset timer $t_0$
procedure	2. Trigger a wake-up request on LP1
	3. Start timer $t_0$
	4. Wait until the DUT signalizes a wake-up condition
	5. Readout timer value ( <i>t_wkp_unpwrd</i> = <i>t</i> <sub>0</sub> )
	6. Configuration of the DUT must be finished within 20ms after wake-up.
	7. Wait until DUT signalizes a link-up condition
	8. Readout timer value $(t_wkp_link-up = t_0 - t_wkp_unpwrd - 20ms$
	(configuration time))
	9. Monitor the link status for additional 750ms
Pass criteria	For all the executed iterations the following pass criterion shall be fulfilled:
	<ul> <li>t_wkp_unpwrd &lt; TWU_Link_Passive + T_Powersupply_Stable + T_PHY_Initialization t_wkp_unpwrd &lt; 17 ms</li> <li>t_wkp_link-up ≤ 100 ms</li> <li>No link drop is observed after link-up condition has been reached.</li> </ul>
Test iterations	See suggested test iterations in Appendix- 7.1 Suggested Iterations
Notes	

Table 26: Main test structure of WAKE\_IOP\_3

Instance Test Case #	DUT / LP configuration	LP as SLAVE	LP as MASTER	LP is MASTER, LP connected with swapped polarity of ETH_N and ETH_P
6.1.1.1	DUT as SLAVE		WAKE_IOP_ 3_S_M	
6.1.1.2	DUT as MASTER	WAKE_IOP_ 3_M_S		
6.1.1.3	DUT as SLAVE			WAKE_IOP_ 3_S_M_P

Table 27: Test case instances of WAKE\_IOP\_3

### 6.1.2 Reception of a wake-up request (WUR) ID: WAKE\_IOP\_4

*Type:* Requirement

Synopsis	Shall ensure that DUT is able to receive a WUR over an active link and to signalize		
391104313			
	it.		
	Parameter to be measured:		
	• TWU_Link_active: Wake-up transmission time over an active link.		
	<ul> <li>Link stability during and after WUR event.</li> </ul>		
Prerequisites	1. DUT with the capability to reset and configure its PHYs.		
	2. Link partner, or device that is connected to the DUT, shall be able to send a		
	wake-up request (WUR).		
	3. The test system shall be able of providing time measurement capabilities		
	synchronized with the test steps events.		
Test Setup			
	DUT DUT_P1 Active link LP1_P1 LP1		
	• DUT shall be connected to an active link partner (LP1) with opposite		
	MASTER/SLAVE configuration.		
	<ul> <li>A stable link-up condition shall be present at the moment of starting the</li> </ul>		
	test execution.		
Test	1. Reset timer $t_0$		
procedure	2. Trigger a wake-up request on LP1		
	3. Start timer $t_0$		
	4. Wait until the DUT signalizes a wake-up condition		
	<ol> <li>Readout timer value (<i>TWU_Link_active</i> = t<sub>0</sub>)</li> <li>Monitor the link status for additional 750ms</li> </ol>		
Pass criteria			
Pass criteria	For all the executed iterations the following pass criterion shall be fulfilled:		
	• <i>TWU_Link_active</i> < 2 ms		
	<ul> <li>No link drop is observed during the test execution.</li> </ul>		
Test			
iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations		
Notes			

Table 28: Main test structure of WAKE\_IOP\_4

Instance Test Case #	DUT / LP configuration	LP as SLAVE	LP as MASTER
6.1.2.1	DUT as SLAVE		WAKE_ IOP_4_S_M
6.1.2.2	DUT as MASTER	WAKE_IOP_4_M_S	

Table 29: Test case instances of WAKE\_IOP\_4

# 6.1.3 Reception of a wake-up pulse (WUP) on an already active DUT *ID:* WAKE\_IOP\_5

Synopsis	Shall ensure that a DUT is able to receive a WUP over a passive link, signalize the wake-up event and upon this to establish a link while another DUT's port link is		
	already established.		
	Parameters to be measured:		
	<ul> <li><i>TWU_Link_passive</i>: Wake-up transmission time over a passive link.</li> <li><i>t_wkp_link-up</i>: Time between DUT wake-up signalization and link-up.</li> <li>Link stability after a wake-up condition.</li> </ul>		
Prerequisites	<ol> <li>DUT shall have more than one port.</li> <li>DUT with the capability to reset and configure its PHYs.</li> <li>DUT with the capability to set its PHYs into sleep mode.</li> <li>Link partner, or device that is connected to the DUT, shall be able to send a</li> </ol>		
	<ul><li>wake-up pulse (WUP).</li><li>5. Link partner shall have local wake-up input available.</li><li>6. The test system shall be able of providing time measurement capabilities synchronized with the test steps events.</li></ul>		
Test Setup	<ul> <li>DUT ports shall be connected to their LPs with opposite MASTER/SLAVE configuration.</li> <li>DUT port DUT_P1 shall be connected to LP1.</li> <li>LP1 including LP1_P1 shall be powered and the link between DUT_P1 and LP1_P1 shall be passive at the moment of starting the test execution.</li> <li>DUT port DUT_P2 shall be connected to LP2.</li> <li>LP2 shall be in normal mode and the link between DUT_P2 and LP2_P1 shall be active at the moment of starting the test execution.</li> </ul>		
Test procedure	<ol> <li>Reset timer t<sub>0</sub></li> <li>Trigger a wake-up request on LP1</li> <li>Start timer t<sub>0</sub></li> <li>Wait until the DUT signalizes a wake-up condition</li> <li>Readout timer value (<i>TWU_Link_passive = t<sub>0</sub></i>)</li> <li>Configuration of the DUT must be finished within 20ms after wake-up.</li> <li>Wait until DUT signalizes a link-up condition</li> </ol>		

	<ol> <li>Readout timer value (t_wkp_link-up = t<sub>0</sub>-TWU_Link_passive - 20ms (configuration time))</li> <li>Configuration of the DUT must be finished within 20ms after wake-up.</li> <li>Monitor the link status for additional 750ms</li> </ol>
Pass criteria	<ul> <li>For all the executed iterations the following pass criterion shall be fulfilled:</li> <li><i>TWU_Link_passive</i> &lt; 2 ms</li> <li><i>t_wkp_link-up</i> ≤ 100 ms</li> <li>No link drop is observed after link-up condition has been reached.</li> </ul>
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	Test can be skipped for DUTs with one port.

Table 30: Main test structure of WAKE\_IOP\_5

Instance Test Case #	DUT / LP configuration	LP as SLAVE	LP as MASTER
6.1.3.1	DUT as SLAVE		WAKE_IOP_ 5_S_M
6.1.3.2	DUT as MASTER	WAKE_IOP_ 5_M_S	

Table 31: Test case instances of WAKE\_IOP\_5

# 6.2 Group 6, Wake-up transmission *ID:* WAKE\_IOP\_6

*Type:* Information

The test cases defined in this section shall ensure that a wake-up (WUP/WUR) can be transmitted and signaled to the upper layer as described in [11].

### 6.2.1 Transmission of a wake-up pulse (WUP) ID: WAKE\_IOP\_7

Synopsis	Shall ensure that the DUT is able to send a WUP over a passive link within an
, .	expected time and to properly signalize the action.
	Parameters to be measured:
	TW/// femuend, receiver Time between levely unkeying event on the DUT and
	<ul> <li>TWU_forward_passive: Time between local wake-up event on the DUT and LP1 wake-up signalization.</li> </ul>
	<ul> <li>t_wkp_link-up: Time between DUT wake-up signalization and link-up.</li> </ul>
	<ul> <li>Link stability after a wake-up condition.</li> </ul>
Prerequisites	1. DUT with the capability to reset and configure its PHYs.
	2. DUT with the capability to set its PHYs into sleep mode.
	3. Link partner, or device that is connected to the DUT, shall be able to receive a
	wake-up pulse (WUP).
	4. DUT implementation shall have local wake-up input available.
	<ol><li>The test system shall be able of providing time measurement capabilities synchronized with the test steps events.</li></ol>
Tost Satur	synchronized with the test steps events.
Test Setup	DUT DUT_P1 Passive link LP1_P1 LP1
	• DUT shall be connected to a link partner (LP1) with a passive link with
	opposite MASTER/SLAVE configuration.
	<ul> <li>LP1 including LP1_P1 shall be powered and connected to the DUT with a</li> </ul>
	passive link.
	<ul> <li>DUT including DUT_P1 shall be powered and connected to the LP1 with a passive link.</li> </ul>
Test	1. Reset timer $t_0$
procedure	2. Trigger a wake-up request on DUT
	3. Start timer $t_0$
	<ol> <li>Wait until LP1 signalizes a wake-up condition</li> <li>Readout timer value (TWU link passive = t<sub>0</sub>)</li> </ol>
	5. Readout timer value (TWU_link_passive = t <sub>0</sub> )

	<ul> <li>6. Configuration of the DUT must be finished within 20ms after wake-up.</li> <li>7. Wait until DUT signalizes a link-up condition</li> <li>8. Readout timer value (t_wkp_link-up = t<sub>0</sub>-TWU_link_passive-20ms (configuration time))</li> <li>9. Monitor the link status for additional 750ms</li> </ul>
Pass criteria	<ul> <li>For all the executed iterations the following pass criterion shall be fulfilled:</li> <li>TWU_link_passive &lt; 2 ms</li> <li>t_wkp_link-up ≤ 100 ms</li> <li>No link drop is observed after link-up condition has been reached.</li> </ul>
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	

Table 32: Main test structure of WAKE\_IOP\_7

Instance Test Case #	DUT / LP configuration	LP as SLAVE	LP as MASTER	LP is MASTER, LP connected with swapped polarity of ETH_N and ETH_P
6.2.1.1	DUT as SLAVE		WAKE_IOP_ 7_S_M	
6.2.1.2	DUT as MASTER	WAKE_IOP_ 7_M_S		
6.2.1.3	DUT as SLAVE			WAKE_IOP_ 7_S_M_P

Table 33: Test case instances of WAKE\_IOP\_7

### 6.2.2 Transmission of a wake-up pulse after local wake-up (WUP) ID: WAKE\_IOP\_8

Synopsis	Shall ensure that the DUT is able to send a WUP over a passive link within an		
	expected time and to properly signalize the action.		
	Parameters to be measured:		
	t when we are a time between least we have the put and 101		
	<ul> <li>t_wkp_unpwrd: Time between local wake-up event on the DUT and LP1 wake-up signalization.</li> </ul>		
	<ul> <li>t_wkp_link-up: Time between DUT wake-up signalization and link-up.</li> </ul>		
	Link stability after a wake-up condition.		
Prerequisites	<ol> <li>DUT with the capability to reset and configure its PHYs.</li> <li>DUT with the capability to set its PHYs into sleep mode.</li> </ol>		
	<ol> <li>Link partner, or device that is connected to the DUT, shall be able to receive a</li> </ol>		
	wake-up pulse (WUP).		
	<ol> <li>DUT implementation shall have local wake-up input available.</li> <li>The test system shall be able of providing time measurement capabilities</li> </ol>		
	synchronized with the test steps events.		
To at Cataon	6. The DUT provides a local wake-up pin.		
Test Setup	Local_Wkp DUT DUT_P1 Passive link LP1_P1 LP1		
	• DUT shall be connected to a link partner (LP1) with a passive link with		
	<ul><li>opposite MASTER/SLAVE configuration.</li><li>DUT shall be in sleep state.</li></ul>		
	<ul> <li>LP1 including LP1_P1 shall be powered and connected to the DUT with a</li> </ul>		
	passive link.		
Test	<ol> <li>Reset timer t<sub>0</sub></li> <li>Apply a local wake pulse to DUT for at least 50us</li> </ol>		
procedure	3. Start timer $t_0$		
	4. Wait until LP1 signalizes a wake-up condition		
	<ol> <li>Readout timer value (t_wkp_unpwrd = t<sub>0</sub>)</li> <li>Configuration of the DUT must be finished within 20ms after wake-up.</li> </ol>		
	7. Wait until DUT signalizes a link-up condition		
	8. Readout timer value $(t_wkp_link-up = t_0 - t_wkp_unpwrd - 20ms$		
	<ul><li>(configuration time))</li><li>9. Monitor the link status for additional 750ms</li></ul>		
Pass criteria	For all the executed iterations the following pass criterion shall be fulfilled:		
	<ul> <li>t_wkp_unpwrd &lt; TWU_WakeIO + TWU_Link_passive +</li> </ul>		
	<ul> <li>t_wkp_unpwrd &lt; two_waketo + two_Link_passive + (T_Powersupply_Stable + T_PHY_Initialization)</li> </ul>		
	$t_wkp_unpwrd < 1ms + 2ms + (15ms)$		
	$t_wkp_unpwrd < 18 \text{ ms}$		
	• $t_wkp_link-up \le 100 \text{ ms}$		

	<ul> <li>No link drop is observed after link-up condition has been reached.</li> </ul>
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	

Table 34: Main test structure of WAKE\_IOP\_8

Instance Test Case #	DUT / LP configuration	LP as SLAVE	LP as MASTER
6.2.2.1	DUT as SLAVE		WAKE_IOP_ 8_S_M
6.2.2.2	DUT as MASTER	WAKE_IOP_ 8_M_S	

Table 35: Test case instances of WAKE\_IOP\_8

### 6.2.3 Transmission of a wake-up request (WUR) ID: WAKE\_IOP\_9

*Type:* Requirement

	Challes and the DUT is the research MUD as a second of the
Synopsis	Shall ensure that the DUT is able to send a WUR over an active link.
	Parameters to be measured:
	• <i>TWU_Link_active</i> : Wake-up transmission time over an active link.
	• Link stability after a wake-up condition.
Prerequisites	1. DUT with the capability to reset and configure its PHYs.
	2. Link partner, or device that is connected to the DUT, shall be able to receive a
	wake-up request (WUR).
	3. The test system shall be able of providing time measurement capabilities
	synchronized with the test steps events.
Test Setup	
Test procedure	<ul> <li>DUT but_P1 Active link [LP1_P1] LP1</li> <li>DUT shall be connected to an active link partner (LP1) with opposite MASTER/SLAVE configuration.</li> <li>A link-up condition shall be present at the moment of starting the test execution.</li> <li>Reset timer t<sub>0</sub></li> <li>Trigger a WUR on the DUT</li> <li>Start timer t<sub>0</sub></li> <li>Wait until the LP1 signalizes a wake-up condition</li> <li>Readout timer value (TWU_Link_active = t<sub>0</sub>)</li> </ul>
Pass criteria	For all the executed iterations the following pass criterion shall be fulfilled:
rass criteria	Tor an the executed iterations the following pass chienon shall be fulfilled.
	<ul> <li>TWU_Link_active &lt; 2 ms</li> </ul>
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	

Table 36: Main test structure of WAKE\_IOP\_9

Instance Test Case #	DUT / LP configuration	LP as SLAVE	LP as MASTER
6.2.3.1	DUT as SLAVE		WAKE_ IOP_9_S_M
6.2.3.2	DUT as MASTER	WAKE_IOP_9_M_S	

Table 37: Test case instances of WAKE\_IOP\_9

## 6.3 Group 7, Wake-up forwarding

ID: WAKE\_IOP\_10

Type: Information

The test cases defined in this section shall ensure that a wake-up request can be forwarded as described in [11].

This section applies for multi-port DUTs.

# 6.3.1 Forwarding wake-up request from active to passive link ID: WAKE\_IOP\_11

Synopsis	Shall ensure that a wake-up request received by a DUT over an active link can be		
591100515			
	forwarded within the expected time to a LP via a passive link.		
	Parameters to be measured:		
	Parameters to be measured.		
	• t who fud: Time between triggering the WILP on LP2 and LP1 wake up		
	<ul> <li>t_wkp_fwd: Time between triggering the WUR on LP2 and LP1 wake-up signalization</li> </ul>		
	signalization.		
Prerequisites	1. DUT shall have more than one port.		
	2. DUT with the capability to reset and configure its PHYs.		
	3. DUT with the capability to set its PHYs into sleep mode.		
	4. Link partner, or device that is connected to the DUT, shall be able to send and		
	receive a wake-up pulse (WUP).		
	5. The test system shall be able of providing time measurement capabilities		
	synchronized with the test steps events.		
Test Setup			
	DUT_P1 DUT_P2 Active link		
	LP1_P1 LP2_P1		
	LP1 IP2		
	LP1 LP2		
	• DUT ports shall be connected to their LPs with opposite MASTER/SLAVE		
	configuration.		
	<ul> <li>DUT port <i>DUT P1</i> shall be connected to LP1.</li> </ul>		
	<ul> <li>LP1 including LP1_P1 shall be powered and the link between DUT_P1 and</li> </ul>		
	LP1_P1 shall be passive at the moment of starting the test execution.		
	<ul> <li>DUT port <i>DUT_P2</i> shall be connected to LP2.</li> </ul>		
	<ul> <li>LP2 shall be in normal mode and the link between DUT_P2 and LP2_P1</li> <li>shall be active at the moment of starting the test everytion</li> </ul>		
	shall be active at the moment of starting the test execution.		

Test	1. Reset timer $t_0$
procedure	2. Trigger a WUR on LP2
	3. Start timer $t_0$
	4. Wait until the LP1 signalizes a wake-up condition
	5. Readout timer value $(t_wkp_fwd = t_0)$
Pass criteria	<ul> <li>Each test iteration shall be classified as pass, if all of the following condition(s) are fulfilled:</li> <li>t_wkp_fwd &lt; TWU_Link_active + TWU_Forwarding + TWU_Link_passive t_wkp_fwd &lt; 2ms + 1ms + 2ms t_wkp_fwd &lt; 5ms</li> </ul>
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	

#### Table 38: Main test structure of WAKE\_IOP\_11

Instance Test Case #	DUT / LP configuration	LP1 as SLAVE, LP2 as SLAVE	LP1 as MASTER, LP2 as MASTER	LP1 as MASTER, LP2 as SLAVE	LP1 as SLAVE, LP2 as MASTER
	DUT_P1 as SLAVE, DUT_P2 as MASTER			WAKE_ IOP_11_SM_MS	
	DUT_P1 as MASTER, DUT_P2 as SLAVE				WAKE_ IOP_11_MS_SM
	DUT_P1 as MASTER, DUT_P2 as MASTER	WAKE_ IOP_11_MM_S S			
	DUT_P1 as SLAVE, DUT_P2 as SLAVE		WAKE_ IOP_11_SS_MM		

Table 39: Test case instances of WAKE\_IOP\_11

# 6.3.2 Forwarding a wake-up request from active to active link *ID:* WAKE\_IOP\_12

Suparaia	Chall ansure that a wake up request received by a DUT over an active link can be				
Synopsis	Shall ensure that a wake-up request received by a DUT over an active link can be				
	forwarded within the expected time to a LP via an active link.				
	Parameters to be measured:				
	<ul> <li>t_wkp_fwd: Time between triggering the WUR on LP2 and LP1 wake-up</li> </ul>				
	signalization.				
Prerequisites	6. DUT shall have more than one port.				
	7. DUT with the capability to reset and configure its PHYs.				
	8. DUT with the capability to set its PHYs into sleep mode.				
	9. Link partner, or device that is connected to the DUT, shall be able to receive a				
	wake-up request (WUR).				
	10. The test system shall be able of providing time measurement capabilities				
	synchronized with the test steps events.				
Test Setup	DUT				
	Active link				
	Aui				
	LP1_P1				
	LP1_P1 LP2_P1				
	LP1 LP2				
	DUT parts shall be connected to their LDs with appacite MASTER/SLAVE				
	<ul> <li>DUT ports shall be connected to their LPs with opposite MASTER/SLAVE configuration</li> </ul>				
	<ul> <li>configuration.</li> <li>DUT port <i>DUT_P1</i> test shall be connected to LP1.</li> </ul>				
	<ul> <li>LP1 shall be powered and the link between DUT_P1 and LP1_P1 shall be</li> </ul>				
	active at the moment of starting the test execution.				
	<ul> <li>DUT port <i>DUT_P2</i> test shall be connected to LP2.</li> </ul>				
	<ul> <li>LP2 shall be in normal mode and the link between DUT_P2 and LP2_P1</li> </ul>				
	shall be active at the moment of starting the test execution.				
Test	1. Reset timer $t_0$				
procedure	2. Trigger a WUR on LP2				
Procedure	3. Start timer $t_0$				
	4. Wait until the LP1 signalizes a wake-up condition				
	5. Readout timer value $(t_wkp_fwd = t_0)$				
Pass criteria	Each test iteration shall be classified as pass, if all of the following condition(s) are				
	fulfilled:				
	<ul> <li>t_wkp_fwd &lt; TWU_Link_active + TWU_Forwarding + TWU_Link_active</li> </ul>				
	t_wkp_fwd < 2ms + 1ms + 2ms				

	<i>t_wkp_fwd</i> < 5ms
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	
	Table 40: Main test structure of WAKE_IOP_12

DUT / LP Instance LP1 as SLAVE, LP1 as MASTER, LP1 as MASTER, LP1 as SLAVE, LP2 as SLAVE LP2 as MASTER LP2 as SLAVE LP2 as MASTER configuration Test Case # DUT\_P1 as SLAVE, WAKE\_ DUT\_P2 as IOP\_12\_SM\_MS MASTER DUT\_P1 as WAKE\_ MASTER, IOP\_12\_MS\_SM DUT\_P2 as SLAVE DUT\_P1 as WAKE\_ MASTER, IOP\_12\_MM\_S DUT\_P2 as S MASTER DUT\_P1 as SLAVE, WAKE\_ DUT\_P2 as SLAVE IOP\_12\_SS\_MM

Table 41: Test case instances of WAKE\_IOP\_12

# 6.3.3 Forwarding a wake-up request from passive to active link *ID:* WAKE\_IOP\_13

Synopsis	Shall ensure that a wake-up request received by a DUT over a passive link can be				
5911005313	forwarded within the expected time to a LP via an active link.				
	Parameters to be measured:				
	<ul> <li>t_wkp_fwd: Time between triggering the WUR on LP1 and LP2 wake-up signalization</li> </ul>				
Duouonuisitoo	signalization.				
Prerequisites	<ol> <li>DUT shall have more than one port.</li> <li>DUT with the capability to reset and configure its PHYs.</li> </ol>				
	<ol> <li>DUT with the capability to set its PHYs into sleep mode.</li> </ol>				
	4. Link partner, or device that is connected to the DUT, shall be able to receive a				
	wake-up request (WUR).				
	5. The test system shall be able of providing time measurement capabilities				
L	synchronized with the test steps events.				
Test Setup					
	LP1_P1				
	LP1 LP2				
	<ul> <li>DUT ports shall be connected to their LPs with opposite MASTER/SLAVE configuration</li> </ul>				
	configuration.				
	<ul> <li>DUT port <i>DUT_P1</i> test shall be connected to LP1.</li> <li>LP1 including LP1_P1 shall be powered and the link between DUT_P1 and</li> </ul>				
	LP1_P1 shall be passive at the moment of starting the test execution.				
	<ul> <li>DUT port <i>DUT_P2</i> test shall be connected to LP2.</li> </ul>				
	<ul> <li>LP2 shall be in normal mode and the link between DUT_P2 and LP2_P1</li> </ul>				
	shall be active at the moment of starting the test execution.				
Test	1. Reset timer $t_0$				
procedure	2. Trigger a wake-up request on LP1				
	3. Start timer $t_0$				
	<ol> <li>Wait until the LP2 signalizes a wake-up condition</li> <li>Readout timer value (t_wkp_fwd = t_0)</li> </ol>				
Pass criteria	Each test iteration shall be classified as pass, if all of the following condition(s) are				
i ass criteria	fulfilled:				
	<ul> <li>t_wkp_fwd &lt; TWU_Link_passive + TWU_Forwarding + TWU_Link_active</li> </ul>				
	t_wkp_fwd < 2ms + 1ms + 2ms				

	t_wkp_fwd < 5ms
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	

Table 42: Main test structure of WAKE\_IOP\_13

Instance Test Case #	DUT / LP configuration	LP1 as SLAVE, LP2 as SLAVE	LP1 as MASTER, LP2 as MASTER	LP1 as MASTER, LP2 as SLAVE	LP1 as SLAVE, LP2 as MASTER
	DUT_P1 as SLAVE, DUT_P2 as MASTER			WAKE_ IOP_13_SM_MS	
	DUT_P1 as MASTER, DUT_P2 as SLAVE				WAKE_ IOP_13_MS_SM
	DUT_P1 as MASTER, DUT_P2 as MASTER	WAKE_ IOP_13_MM _SS			
	DUT_P1 as SLAVE, DUT_P2 as SLAVE		WAKE_ IOP_13_SS_MM		

Table 43: Test case instances of WAKE\_IOP\_13

# 6.3.4 Forwarding a wake-up request from passive to passive link *ID:* WAKE\_IOP\_14

Synopsis	Shall ensure that a wake-up request received by a DUT over a passive link can be			
Synopsis				
	forwarded within the expected time to a LP via a passive link.			
	Parameters to be measured:			
	<ul> <li>t_wkp_fwd: Time between triggering the WUR on LP1 and LP2 wake-up</li> </ul>			
	signalization.			
Prerequisites	1. DUT shall have more than one port.			
	2. DUT with the capability to reset and configure its PHYs.			
	3. DUT with the capability to set its PHYs into sleep mode.			
	4. Link partner, or device that is connected to the DUT, shall be able to receive a			
	<ul><li>wake-up pulse (WUP).</li><li>5. The test system shall be able of providing time measurement capabilities</li></ul>			
	<ol><li>The test system shall be able of providing time measurement capabilities synchronized with the test steps events.</li></ol>			
Test Setup				
i est setup				
	LP1_P1 LP2_P1			
	LP1 LP2			
	DUT ports shall be connected to their LPs with opposite MASTER/SLAVE			
	configuration.			
	• DUT port <i>DUT_P1</i> test shall be connected to LP1.			
	<ul> <li>LP1 including LP1_P1 shall be powered and the link between DUT_P1 and LP1_P1 shall be passive at the moment of starting the test execution</li> </ul>			
	LP1_P1 shall be passive at the moment of starting the test execution.			
	<ul> <li>DUT port <i>DUT_P2</i> test shall be connected to LP2.</li> <li>LP1 including LP1 P2 shall be powered and the link between DUT P1 and</li> </ul>			
	• LP1 including LP1_P2 shall be powered and the link between DO1_P1 and LP1_P1 shall be passive at the moment of starting the test execution.			
	LFI_FI Shan be passive at the moment of starting the test execution.			
Test	1. Reset timer $t_0$			
procedure	<ol> <li>Trigger a wake-up request on LP1</li> </ol>			
Procedure	3. Start timer $t_0$			
	<ol> <li>Wait until the LP2 signalizes a wake-up condition</li> </ol>			
	5. Readout timer value $(t_wkp_fwd = t_0)$			
Pass criteria	Each test iteration shall be classified as pass, if all of the following condition(s) are			
	fulfilled:			
	<ul> <li>t_wkp_fwd &lt; TWU_Link_passive + TWU_Forwarding + TWU_Link_passive</li> </ul>			
	<i>t_wkp_fwd</i> < 2ms + 1ms + 2ms			

	<i>t_wkp_fwd</i> < 5 ms
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	

Table 44: Main test structure of WAKE\_IOP\_14

Instance Test Case #	DUT / LP configuration	LP1 as SLAVE, LP2 as SLAVE	LP1 as MASTER, LP2 as MASTER	LP1 as MASTER, LP2 as SLAVE	LP1 as SLAVE, LP2 as MASTER
	DUT_P1 as SLAVE, DUT_P2 as MASTER			WAKE_ IOP_14_SM_MS	
	DUT_P1 as MASTER, DUT_P2 as SLAVE				WAKE_ IOP_14_MS_SM
	DUT_P1 as MASTER, DUT_P2 as MASTER	WAKE_ IOP_14_MM _SS			
	DUT_P1 as SLAVE, DUT_P2 as SLAVE		WAKE_ IOP_14_SS_MM		

Table 45: Test case instances of WAKE\_IOP\_14

# 6.3.5 Forwarding a wake-up request from passive to passive link, DUT in sleep *ID:* WAKE\_IOP\_15

Synopsis	Shall ansure that a wake-up request received by a DLIT over a passive link can be				
Synopsis	Shall ensure that a wake-up request received by a DUT over a passive link can be				
	forwarded within the expected time to a LP via a passive link.				
	Parameters to be measured:				
	<ul> <li>t_wkp_fwd: Time between triggering the WUR on LP1 and LP2 wake-up</li> </ul>				
	signalization.				
Prerequisites	1. DUT shall have more than one port.				
	2. DUT with the capability to reset and configure its PHYs.				
	3. DUT with the capability to set its PHYs into sleep mode.				
	4. Link partner, or device that is connected to the DUT, shall be able to receive a				
	<ul><li>wake-up pulse (WUP).</li><li>5. The test system shall be able of providing time measurement capabilities</li></ul>				
	<ol><li>The test system shall be able of providing time measurement capabilities synchronized with the test steps events.</li></ol>				
Test Setup					
iest setup					
	LP1_P1 LP2_P1				
	LP1 LP2				
	DUT ports shall be connected to their LPs with opposite MASTER/SLAVE				
	configuration.				
	<ul> <li>DUT port DUT_P1 test shall be connected to LP1.</li> <li>LP1 including LP1. P1 shall be recurred and the link between DUT_P1 and</li> </ul>				
	<ul> <li>LP1 including LP1_P1 shall be powered and the link between DUT_P1 and</li> <li>LP1_P1 shall be passive at the moment of starting the test execution</li> </ul>				
	LP1_P1 shall be passive at the moment of starting the test execution.				
	<ul> <li>DUT port <i>DUT_P2</i> test shall be connected to LP2.</li> <li>LP1 including LP1_P2 shall be powered and the link between DUT_P1 and</li> </ul>				
	<ul> <li>LP1 including LP1_P2 shall be powered and the link between DUT_P1 and LP1_P1 shall be passive at the moment of starting the test execution.</li> </ul>				
	Li 1 1 shan be passive at the moment of starting the test execution.				
Test	1. Reset timer $t_0$				
procedure	<ol> <li>Trigger a wake-up request on LP1</li> </ol>				
12.000.0010	3. Start timer t0				
	4. Wait until the LP2 signalizes a wake-up condition				
	5. Readout timer value (t_wkp_fwd = t0)				
Pass criteria	Each test iteration shall be classified as pass, if all of the following condition(s) are				
	fulfilled:				
	<ul> <li>t_wkp_fwd &lt; TWU_Link_Passive + (T_Powersupply_Stable +</li> </ul>				
	T_PHY_Initialization) + TWU_Forwarding + TWU_Link_Passive				

	t_wkp_fwd < 2ms + (15ms) + 1ms + 2ms t_wkp_fwd < 20 ms
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	

#### Table 46: Main test structure of WAKE\_IOP\_15

Instance Test Case #	DUT / LP configuration	LP1 as SLAVE, LP2 as SLAVE	LP1 as MASTER, LP2 as MASTER	LP1 as MASTER, LP2 as SLAVE	LP1 as SLAVE, LP2 as MASTER
	DUT_P1 as SLAVE, DUT_P2 as MASTER			WAKE_ IOP_15_SM_MS	
	DUT_P1 as MASTER, DUT_P2 as SLAVE				WAKE_ IOP_15_MS_SM
	DUT_P1 as MASTER, DUT_P2 as MASTER	WAKE_ IOP_15_MM_S S			
	DUT_P1 as SLAVE, DUT_P2 as SLAVE		WAKE_ IOP_15_SS_MM		

Table 47: Test case instances of WAKE\_IOP\_15

## 6.4 Group 8, Sleep

ID: WAKE\_IOP\_16

Type: Requirement

The test cases defined in this section shall ensure that the PHY is able to make the transition to sleep as requested.

# 6.4.1 Sleep request after link-up ID: WAKE\_IOP\_17

Synopsis	Shall ensure that the DUT is able to enter the sleep mode and remain in this state		
o y nopolo	after link-up was established when the sleep request is issued on the DUT side.		
	after link-up was established when the sleep request is issued on the DOT side.		
Prerequisites	1. DUT with the capability to reset and configure its PHYs.		
rielequisites	<ol> <li>DUT with the capability to set its PHYs into sleep mode.</li> </ol>		
	<ol> <li>The test system shall be able of providing time measurement capabilities</li> </ol>		
	synchronized with the test steps events.		
Test Setup			
Test Setup			
	DUT DUT_P1 Active link LP1_P1 LP1		
	DUT shall be connected to an active link partner (LP1) with eppecite		
	<ul> <li>DUT shall be connected to an active link partner (LP1) with opposite MASTER/SLAVE configuration.</li> </ul>		
	<ul> <li>A stable link-up condition shall be present at the moment of starting the</li> </ul>		
	test execution.		
Test	1. Trigger a sleep request on the DUT		
procedure	2. Start timer $t_0$		
procedure	<ol> <li>Wait until the DUT signalizes a sleep condition</li> </ol>		
	4. Readout timer value $(t_sleep = t_0)$		
	<ol> <li>DUT and LP shall monitor whether the sleep condition remains for at least</li> </ol>		
	750ms.		
Pass criteria	Each test iteration shall be classified as pass, if all of the following condition(s) are		
	fulfilled:		
	i annea.		
	<ul> <li>t_sleep &lt; sleep_req_timer</li> </ul>		
	<i>t_sleep</i> < 16ms		
	Both the DUT and the LP must not leave the sleep condition after the		
	SLEEP state has been entered.		

Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	
	Table 49: Main test structure of WAKE IOD 17

 Table 48: Main test structure of WAKE\_IOP\_17

Instance Test Case #	DUT / LP configuration	LP as SLAVE	LP as MASTER
6.4.1.1	DUT as SLAVE		WAKE_IOP_17_S_M
6.4.1.2	DUT as MASTER	WAKE_IOP_17_M_S	

Table 49: Test case instances of WAKE\_IOP\_17

## 6.4.2 Remote sleep request after link-up

ID: WAKE\_IOP\_18

Type: Requirement

Cumonolo	Chall answer that the DUT is able to option the class made and remain in this state		
Synopsis	Shall ensure that the DUT is able to enter the sleep mode and remain in this state		
	after link-up was established when the sleep request is issued on the LP side.		
Prerequisites	1. DUT with the capability to reset and configure its PHYs.		
	2. DUT with the capability to set its PHYs into sleep mode.		
	3. The test system shall be able of providing time measurement capabilities		
	synchronized with the test steps events.		
Test Setup			
	DUT DUT_P1 Active link LP1_P1 LP1		
	• DUT shall be connected to an active link partner (LP1) with opposite		
	MASTER/SLAVE configuration.		
	• A stable link-up condition shall be present at the moment of starting the		
	test execution.		
Test	1. Trigger a sleep request on the LP1		
procedure	2. Start timer $t_0$		
	3. Wait until the DUT signalizes a sleep condition		
	4. Readout timer value $(t_sleep = t_0)$		
	5. DUT and LP shall monitor whether the sleep condition remains for at least		
	750ms.		
Pass criteria	Each test iteration shall be classified as pass, if all of the following condition(s) are		
	fulfilled:		
	runneu.		
	<ul> <li>t_sleep &lt; sleep_req_timer + sleep_ack_timer</li> </ul>		
	$t_sleep < 16ms + 8ms$		
	$t \ sleep < 24 ms$		
	<ul> <li>Both the DUT and the LP shall not leave the sleep condition after the</li> </ul>		
	SLEEP state has been entered.		
Test			
iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations		
Notes			
NULES			

 Table 50: Main test structure of WAKE\_IOP\_18

Instance Test Case #	DUT / LP configuration	LP as SLAVE	LP as MASTER
6.4.2.1	DUT as SLAVE		WAKE_IOP_18_S_M
6.4.2.2	DUT as MASTER	WAKE_IOP_18_M_S	

Table 51: Test case instances of WAKE\_IOP\_18

## 7 Appendix

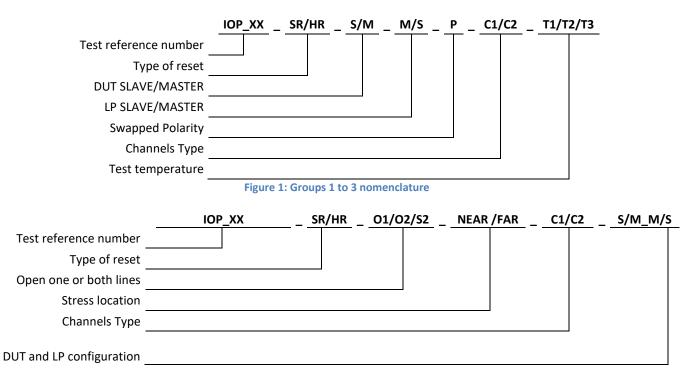
### 7.1 Suggested Iterations

### 7.1.1 Nomenclature

The following parameters are to describe the test environment and if applicable the kind of stress and its location.

Reference name	Description
1000BASE-T1_IOP_XX	Test reference
SR	Soft Reset
HR	Hard Reset
01	Open is on ETH_N or ETH_P
02	Open on both ETH_N and ETH_P
S2	Short on both ETH_N and ETH_P
NEAR	Open/Short near to DUT
FAR	Open/Short near to LP
М	MASTER
S	SLAVE
Р	Swapped Polarity
C1	Type A.3 Channel
C2	Type A.1 Channel or a combination of Type A.2 and A.3 Channels
T1	Room Temperature
T2	-40°C
Т3	105°C /125°C

#### Table 52: Nomenclature of test environment variables



#### Figure 2: Group 4 nomenclature

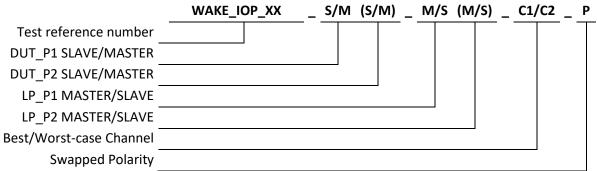


Figure 3: Group 5-8 nomenclature

Group	Test Case	Minimal amount of iterations per LP*
	IOP_16_SR_M_S_C1_T1	500.000
	IOP_16_SR_M_S_C2_T1	500.000
	IOP_16_SR_S_M_C1_T1	500.000
	IOP_16_SR_S_M_P_C1_T1	8.000
Group 1:	IOP_16_SR_S_M_C2_T1	500.000
Link Status	IOP_16_SR_S_M_P_C2_T1	18.000
	IOP_17_SR_M_M_C2_T1	50.000
	IOP_17_SR_S_S_C2_T1	50.000
	IOP_19_SR_M_S_C2_T1	125.000
	IOP_19_SR_S_M_C2_T1	125.000

### 7.1.2 Group 1 test cases iterations

Table 53: Group 1 test cases suggested iterations

\*When considering multiple link partners tests.

### 7.1.3 Group 2 test cases iterations

		Data tara l
		Minimal
Group	Test Case	amount of
		iterations per LP*
	IOP_21_HR_M_S_C1_T1	200
	IOP_21_HR_M_S_C1_T2	25
	IOP_21_HR_M_S_C1_T3	25
	IOP_21_HR_M_S_C2_T1	1.800
	IOP_21_HR_M_S_C2_T2	225
	IOP_21_HR_M_S_C2_T3	225
	IOP_21_HR_S_M_C1_T1	200
	IOP_21_HR_S_M_C1_T2	25
	IOP_21_HR_S_M_C1_T3	25
	IOP_21_HR_S_M_C2_T1	1.800
	IOP_21_HR_S_M_C2_T2	225
	IOP_21_HR_S_M_C2_T3	225
	IOP_21_HR_S_M_P_C1_T1	200
	IOP_21_HR_S_M_P_C1_T2	25
	IOP_21_HR_S_M_P_C1_T3	25
	IOP_21_HR_S_M_P_C2_T1	1.800
	IOP_21_HR_S_M_P_C2_T2	225
	IOP_21_HR_S_M_P_C2_T3	225
	IOP_21_SR_M_S_C1_T1	250.000
Group 2:	IOP_21_SR_M_S_C1_T2	25.000
Link-Up	IOP_21_SR_M_S_C1_T3	25.000
Link-Op	IOP_21_SR_M_S_C2_T1	500.000
	IOP_21_SR_M_S_C2_T2	25.000
	IOP_21_SR_M_S_C2_T3	25.000
	IOP_21_SR_S_M_C1_T1	250.000
	IOP_21_SR_S_M_C1_T2	24.750
	IOP_21_SR_S_M_C1_T3	24.750
	IOP_21_SR_S_M_C2_T1	500.000
	IOP_21_SR_S_M_C2_T2	25.000
	IOP_21_SR_S_M_C2_T3	25.000
	IOP_21_SR_S_M_P_C1_T1	8.000
	IOP_21_SR_S_M_P_C1_T2	250
	IOP_21_SR_S_M_P_C1_T3	250
	IOP_21_SR_S_M_P_C2_T1	72.000
	IOP_21_SR_S_M_P_C2_T2	2.250
	IOP_21_SR_S_M_P_C2_T3	2.250
	IOP_22_HR_M_S_C1_T1	800
	IOP_22_HR_M_S_C1_T2	25
	IOP_22_HR_M_S_C1_T3	25
	IOP 22 HR M S C2 T1	7.200
		,.200

Group	Test Case	Minimal amount of iterations per LP*
	IOP_22_HR_M_S_C2_T2	225
	IOP_22_HR_M_S_C2_T3	225
	IOP_22_HR_S_M_C1_T1	800
	IOP_22_HR_S_M_C1_T2	25
	IOP_22_HR_S_M_C1_T3	25
	IOP_22_HR_S_M_C2_T1	7.200
	IOP_22_HR_S_M_C2_T2	225
	IOP_22_HR_S_M_C2_T3	225
	IOP_22_HR_S_M_P_C1_T1	800
	IOP_22_HR_S_M_P_C1_T2	25
	IOP_22_HR_S_M_P_C1_T3	25
	IOP_22_HR_S_M_P_C2_T1	7.200
	IOP_22_HR_S_M_P_C2_T2	225
	IOP_22_HR_S_M_P_C2_T3	225
	IOP_22_SR_M_S_C1_T1	20.000
	IOP_22_SR_M_S_C1_T2	625
	IOP_22_SR_M_S_C1_T3	625
	IOP_22_SR_M_S_C2_T1	180.000
	IOP_22_SR_M_S_C2_T2	5.625
	IOP_22_SR_M_S_C2_T3	5.625
	IOP_22_SR_S_M_C1_T1	20.000
	IOP_22_SR_S_M_C1_T2	625
	IOP_22_SR_S_M_C1_T3	625
	IOP_22_SR_S_M_C2_T1	180.000
	IOP_22_SR_S_M_C2_T2	5.625
	IOP_22_SR_S_M_C2_T3	5.625
	IOP_22_SR_S_M_P_C1_T1	4.000
	IOP_22_SR_S_M_P_C1_T2	125
	IOP_22_SR_S_M_P_C1_T3	125
	IOP_22_SR_S_M_P_C2_T1	36.000
	IOP_22_SR_S_M_P_C2_T2	1.125
	IOP_22_SR_S_M_P_C2_T3	1.125

Table 54: Group 2 test cases suggested iterations

\*When considering multiple link partners tests.

### 7.1.4 Group 3 test cases iterations

Group	Test Case	Suggested amount of iterations	Minimal amount of iterations per LP*
Group 3:	IOP_24a_SR_M_S_C1_T1	1	n.a.
	IOP_24a_SR_S_M_C1_T1	1	n.a.
Signal	IOP_24b_SR_M_S_C1_T1	1	n.a.
Quality	IOP_24b_SR_S_M_C1_T1	1	n.a.

Table 55: Group 3 test cases suggested iterations

\*When considering multiple link partners tests.

### 7.1.5 Group 4 test cases iterations

Group	Test Case	Suggested amount of iterations	Minimal amount of iterations per LP*
	IOP_31_SR_C1_T1**	50	50
	IOP_31_SR_C2_T1**	450	450
	IOP_32_SR_O1_FAR_M_C2_T1	500	n.a.
	IOP_32_SR_O1_FAR_S_C2_T1	500	n.a.
	IOP_32_SR_O1_NEAR_M_C2_T1	500	n.a.
	IOP_32_SR_O1_NEAR_S_C2_T1	500	n.a.
	IOP_32_SR_O2_FAR_M_C2_T1	500	n.a.
	IOP_32_SR_O2_FAR_S_C2_T1	500	n.a.
	IOP_32_SR_O2_NEAR_M_C2_T1	500	n.a.
Group 4:	IOP_32_SR_O2_NEAR_S_C2_T1	500	n.a.
	IOP_33_SR_S2_FAR_M_C2_T1	500	n.a.
Cable	IOP_33_SR_S2_FAR_S_C2_T1	500	n.a.
Diagnostics	IOP_33_SR_S2_NEAR_M_C2_T1	500	n.a.
	IOP_33_SR_S2_NEAR_S_C2_T1	500	n.a.
	IOP_33_SR_S2_FAR_GND_M_C2_T1	500	n.a.
	IOP_33_SR_S2_FAR_GND_S_C2_T1	500	n.a.
	IOP_33_SR_S2_NEAR_GND_M_C2_T1	500	n.a.
	IOP_33_SR_S2_NEAR_GND_S_C2_T1	500	n.a.
	IOP_33_SR_S2_FAR_VBAT_M_C2_T1	500	n.a.
	IOP_33_SR_S2_FAR_VBAT_S_C2_T1	500	n.a.
	IOP_33_SR_S2_NEAR_VBAT_M_C2_T1	500	n.a.
	IOP_33_SR_S2_NEAR_VBAT_S_C2_T1	500	n.a.

Table 56: Group 4 test cases suggested iterations

\*When considering multiple link partners tests.

\*\*Only Diagnostic test case (IOP 31)

### 7.1.6 Group 5 test cases iterations

Group	Test Case	Suggested amount of iterations
	WAKE_IOP_3_S_M_C1	2500
	WAKE_IOP_3_M_S_C1	2500
Group 5:	WAKE_IOP_3_S_M_C2	2500
Group 5.	WAKE_IOP_3_M_S_C2	2500
	WAKE_IOP_3_S_M_C1_P	2500
Wake-up	WAKE_IOP_4_S_M_C1	5000
reception and	WAKE_IOP_4_M_S_C1	5000
signalizing	WAKE_IOP_5_S_M_C1	2500
	WAKE_IOP_5_M_S_C1	2500
	WAKE_IOP_5_S_M_C2	2500
	WAKE_IOP_5_M_S_C2	2500

Table 57: Group 5 test cases suggested iterations

### 7.1.7 Group 6 test cases iterations

Group	Test Case	Suggested amount of iterations
	WAKE_IOP_7_M_S_C1	2500
	WAKE_IOP_7_S_M_C1	2500
	WAKE_IOP_7_M_S_C2	2500
Group 6:	WAKE_IOP_7_S_M_C2	2500
	WAKE_IOP_7_M_S_C1_P	2500
Wake-up	WAKE_IOP_8_S_M_C1	2500
transmission	WAKE_IOP_8_M_S_C1	2500
	WAKE_IOP_8_S_M_C2	2500
	WAKE_IOP_8_M_S_C2	2500
	WAKE_IOP_9_S_M_C1	5000
	WAKE_IOP_9_M_S_C1	5000

Table 58: Group 6 test cases suggested iterations

### 7.1.8 Group 7 test cases iterations

Group	Test Case	Suggested amount of iterations
	WAKE_IOP_11_MM_SS_C1	5000
	WAKE_IOP_11_SS_MM_C1	5000
	WAKE_IOP_11_MS_SM_C1	5000
	WAKE_IOP_11_SM_MS_C1	5000
	WAKE_IOP_12_MM_SS_C1	5000
	WAKE_IOP_12_SS_MM_C1	5000
	WAKE_IOP_12_MS_SM_C1	5000
Group 7:	WAKE_IOP_12_SM_MS_C1	5000
Group 7.	WAKE_IOP_13_MM_SS_C1	5000
	WAKE_IOP_13_SS_MM_C1	5000
Wake-up	WAKE_IOP_13_MS_SM_C1	5000
forwarding	WAKE_IOP_13_SM_MS_C1	5000
	WAKE_IOP_14_MM_SS_C1	5000
	WAKE_IOP_14_SS_MM_C1	5000
	WAKE_IOP_14_MS_SM_C1	5000
	WAKE_IOP_14_SM_MS_C1	5000
	WAKE_IOP_15_MM_SS_C1	5000
	WAKE_IOP_15_SS_MM_C1	5000
	WAKE_IOP_15_MS_SM_C1	5000
	WAKE_IOP_15_SM_MS_C1	5000

Table 59: Group 7 test cases suggested iterations

### 7.1.9 Group 8 test cases iterations

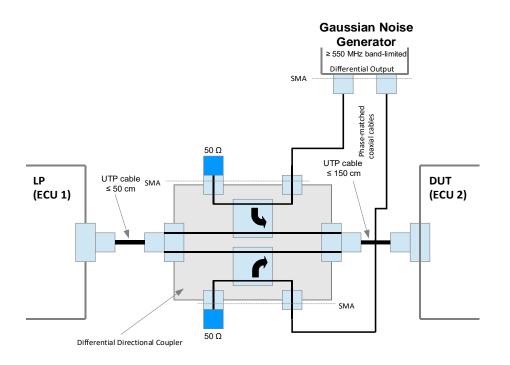
Group	Test Case	Suggested amount of iterations
Group 8:	WAKE_IOP_17_S_M_C1	5000
	WAKE_IOP_17_M_S_C1	5000
Sleep	WAKE_IOP_18_S_M_C1	5000
	WAKE_IOP_18_M_S_C1	5000

Table 60: Group 8 test cases suggested iterations

## 7.2 Artificial degradation of channel quality

### 7.2.1 Description

Figure 4 shows an example approach to artificially reduce the quality of the communication channel with a differential directional coupler whose parameters are defined in Table 61.



#### Figure 4: Example for artificial degradation of channel quality

Differential Directional Coupler			
Parameter	Value	Frequency	
Insertion Loss	≤ 1 dB	1 – 600 MHz	
Return Loss	$\geq \begin{pmatrix} 19 & 1 \le f < 10 \\ 24 - 5\log f & 10 \le f < 40 \\ 16 & 40 \le f < 130 \\ 37 - 10\log f & 130 \le f < 400 \\ 11 & 400 \le f \le 600 \end{pmatrix} dB$	1 – 600 MHz	
Coupling Flatness	± 1 dB	1 – 600 MHz	
Coupling Attenuation Forward	20 dB ± 1 dB		
Coupling Attenuation Backward	21 dB ± 1 dB		

Table 61: Example for Differential Directional Coupler Parameters

## 7.3 Exemplar xGMII/SMI Pinout Interface for testing purposes.

Following figure shows an example of an xGMII/SMI Pinout Interface for PHY Board used for testing purposes. The aim of this example is the benefits of 'requiring' PHY silicon vendors to support similar pinout interface for testing with xGMII/MDIO access, due to the re-use factor if this pinout interface is aligned between different test houses. This example in particular covers the requirements for interoperability testing, it may be the case that other testing services, like conformance or EMC, require additional signals, if these have been omitted, any test house is free to enhance this pinout interface -- for example, TX\_TCLK is not currently present on this example, this signal could be added (at least optionally).

Pin	Signal	Signal	Pin
1	GND	VCC (3.3V)	2
3	GND	VCC (3.3V)	4
5	GND	GND	6
7	GND	MDC	8
9	GND	MDIO	10
11	IN1	GND	12
13	GND	NC	14
15	GND	NC	16
17	INH	GND	18
19	GND	RGMII_RXD3	20
21	GND	RGMII_RXD2	22
23	GND	RGMII_RXD1	24
25	GND	RGMII_RXD0	26
27	OUT1	GND	28
29	GND	RGMII_RXC	30
31	GND	RGMII_RX_CTL	32
33	WAKE	GND	34
35	GND	RGMII_TXC	36
37	SGMII_RXN	GND	38
39	SGMII_RXP	RGMII_TXD3 *	40
41	GND	RGMII_TXD2 *	42
43	GND	RGMII_TXD1 *	44
45	SGMII_TXN	RGMII_TXD0 *	46
47	SGMII_TXP	GND	48
49	GND	RGMII_TX_CTL	50
51	GND	GND	52
53	SPI_MOSI	TX_ER	54
55	SPI_MISO	RX_ER	56
57	SPI_CS1	GND	58
59	SPI_CLK	RESET	60
	BOTTOM	ТОР	

#### Table 62: Example for xGMII / SMI Pinout

#### 7.3.1 Connector description

Manufacturer: Samtec

Description: Conn Edge Rate Socket Strip SKT 60 POS 0.8mm Solder ST Edge Mount T/R

Part number: ERF8-030-01-L-D-EM2

## 7.4 List of tables

Table 1: List of Abbreviations	13
Table 2: List of Definitions	15
Table 3 - Main test structure	16
Table 4 - Test case instances definition	
Table 5 - Example of test case instances	
Table 6: Main test structure of 1000BASET1_IOP_16	25
Table 7: Test case instances of 1000BASET1_IOP_16	25
Table 8: Main test structure of 1000BASET1_IOP_17	26
Table 9: Test case instances of 1000BASET1_IOP_17	26
Table 10: Main test structure of 1000BASET1_IOP_19	27
Table 11: Test case instances of 1000BASET1_IOP_19	28
Table 12: Main test structure of 1000BASET1_IOP_21	29
Table 13: Test case instances of 1000BASET1_IOP_21	29
Table 14: Main test structure of 1000BASET1_IOP_22	30
Table 15: Test case instances of 1000BASET1_IOP_22	31
Table 16: Main test structure of 1000BASET1_IOP_24a	34
Table 17: Test case instances of 1000BASET1_IOP_24a	34
Table 18: Main test structure of 1000BASET1_IOP_24b	36
Table 19: Test case instances of 1000BASET1_IOP_24b	36
Table 20: Main test structure of 1000BASET1_IOP_31	37
Table 21: Main test structure of 1000BASET1_IOP_31	37
Table 22: Main test structure of 1000BASET1_IOP_32	38
Table 23: Test case instances of 1000BASET1_IOP_32	39
Table 24: Main test structure of 1000BASET1_IOP_33	
Table 25: Test case instances of 1000BASET1_IOP_33	41
Table 26: Main test structure of WAKE_IOP_3	43
Table 27: Test case instances of WAKE_IOP_3	43
Table 28: Main test structure of WAKE_IOP_4	44
Table 29: Test case instances of WAKE_IOP_4	
Table 30: Main test structure of WAKE_IOP_5	
Table 31: Test case instances of WAKE_IOP_5	47
Table 32: Main test structure of WAKE_IOP_7	49
Table 33: Test case instances of WAKE_IOP_7	49
Table 34: Main test structure of WAKE_IOP_8	51
Table 35: Test case instances of WAKE_IOP_8	51
Table 36: Main test structure of WAKE_IOP_9	52
Table 37: Test case instances of WAKE_IOP_9	53
Table 38: Main test structure of WAKE_IOP_11	55
Table 39: Test case instances of WAKE_IOP_11	55
Table 40: Main test structure of WAKE_IOP_12	57

Table 41: Test case instances of WAKE_IOP_12	57
Table 42: Main test structure of WAKE_IOP_13	59
Table 43: Test case instances of WAKE_IOP_13	59
Table 44: Main test structure of WAKE_IOP_14	61
Table 45: Test case instances of WAKE_IOP_14	61
Table 46: Main test structure of WAKE_IOP_15	63
Table 47: Test case instances of WAKE_IOP_15	63
Table 48: Main test structure of WAKE_IOP_17	65
Table 49: Test case instances of WAKE_IOP_17	65
Table 50: Main test structure of WAKE_IOP_18	66
Table 51: Test case instances of WAKE_IOP_18	67
Table 52: Nomenclature of test enviroment variables	68
Table 53: Group 1 test cases suggested iterations	69
Table 54: Group 2 test cases suggested iterations	71
Table 55: Group 3 test cases suggested iterations	72
Table 56: Group 4 test cases suggested iterations	72
Table 57: Group 5 test cases suggested iterations	73
Table 58: Group 6 test cases suggested iterations	73
Table 59: Group 7 test cases suggested iterations	74
Table 60: Group 8 test cases suggested iterations	74
Table 61: Example for Differential Directional Coupler Parameters	
Table 62: Example for xGMII / SMI Pinout	77

## 7.5 List of figures

Figure 1: Groups 1 to 3 nomenclature	68
Figure 2: Group 4 nomenclature	69
Figure 3: Group 5-8 nomenclature	69
Figure 4: Example for artificial degradation of channel quality	75