100BASE-T1 Interoperability Test Suite

Interoperability Test Suite Specification



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Title	100BASE-T1 Interoperability Test Suite
Version	1.2
Date	December 3, 2024
Status	Final
Restriction Level	Public

100BASE-T1 Interoperability Test Suite. This document aims to be a guide to implement and carry out the necessary procedures to test the grade of interoperability between devices with 100BASE-T1 capabilities.

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2 Introduction

2.1 Overview

The goal of this document is to define a set of tests that on one hand ensure interoperability between multiple devices that use 100BASE-T1 capable PHYs. In particular, this requires each PHY to be able to establish a stable link within a given time limit, to be able to reliably monitor and signal the current link status to an upper layer and to be able to transmit data with an upper bit error rate limit.

Furthermore, on the other hand, this document addresses a set of test cases that verify the reliability of important supported features of an automotive Ethernet PHY (often also called transceiver), e.g. for diagnostic purposes for automotive Ethernet PHY's. In particular, signal quality index (SQI) and harness defects detection.

Finally this test specification defines a set of tests that ensure the wake-up/sleep interoperability between IEEE802.3bw (100BASE_T1) PHYs and Switches.

Note: The tests do not solely cover the respective PHYs/Switches, but also takes into account PHY/Switches configuration and an external filter, if applicable. The results of the Interoperability Test Suite will not only depend of the PHY/switches, but also from the general configuration of Implementation Under Test, the Link Partner, the chokes and the communication channel conditions.

2.2 Normative References

- [1] IEEE P802.3bw[™] Physical Layer Specifications and Management Parameters for 100 Mb/s Operation over a Single Balanced Twisted Pair Cable (100BASE-T1)
- [2] IEEE P802.3bp[™]: Physical Layer Specifications and Management Parameters for 1 Gb/s Operation over a Single Twisted Pair Copper Cable
- [3] IEEE P802.3-2015 IEEE Standard for Ethernet
- [4] OPEN ALLIANCE: 100BASE-T1 PHY Control Test Suite Revision 1.0
- [5] OPEN ALLIANCE: 100BASE-T1 Physical Media Attachment Test Suite Revision 1.0
- [6] OPEN ALLIANCE: 100BASE-T1 Physical Coding Sublayer Test Suite Revision 1.1
- [7] OPEN ALLIANCE: 100BASE-T1 EMC Test Specification for Transceivers Revision 2.0
- [8] OPEN ALLIANCE: 100BASE-T1 EMC Test Specification for Common Mode Chokes Revision 2.0
- [9] OPEN ALLIANCE: 100BASE-T1 Definitions for Communication Channel Revision 1.0
- [10] OPEN ALLIANCE: 100BASE-T1 system implementation specification Revision 1.0
- [11] OPEN ALLIANCE: Advanced diagnostic features for 100BASE-T1 automotive Ethernet PHYs - Revision 1.0
- [12] OPEN ALLIANCE: Automotive Ethernet ECU Test Specification- Revision 3.0
- [13] OPEN ALLIANCE: 100BASE-T1 EMC Test Specification for ESD suppression devices Revision 2.0
- [14] OPEN ALLIANCE: Sleep/Wake-up Specification for Automotive Ethernet Revision 2.0

2.3 Abbreviations and definitions

ID: 100BASET1_L1_IOP_1

Type: Information

Abbreviation	Glossary term	Glossary definition	
CRC	Cyclic Redundancy Check		
ISO/OSI		Layer model of communication systems	
MAC	Media Access Control	Abbreviation for the sub layer of the data link layer (layer 2) of the OSI model or for the physical device that implements the Media Access Control functions.	
MDI	Media dependent interface		
РНҮ	Physical Layer	Abbreviation for the physical layer (layer 1) of the OSI model or for the device that implements layer 1 of the OSI model.	
100BASE-T1	Open Alliance 100BASE-T1		
DUT	Device under test	Combination of uC, PHY/Switch component, PHY/Switch configuration and filter that is being tested.	
LP	Link partner	cf. list of definitions (100BASET1_L1_IOP_2).	
ETH_N		Negative MDI pin or cable connected to a PHY's negative MDI pin.	
ETH_P		Positive MDI pin or cable connected to a PHY's positive MDI pin.	
SQI	Signal quality indicator	The PHY's estimated signal quality of the channel or a comparable value from which a quality indicator for the communication channel can be derived. The SQI value shall be stored in a register. In general it should be composed by 8 levels (between "000" = worst value and "111" = 7 = best value).	
CIDM	Characteristic Impedance Differential mode		
IL	Insertion Loss		
RL	Return Loss		

Abbreviation Glossary term		Glossary definition		
S-Parameter	Scattering Parameter			
TDR	Time domain reflection			
SCC	Standalone Communication Channel			
WUR	R Wake-up Request The Wake-Up Request (WUR to indicate a wake-up request partner. It can be sent by a r switch PHY to distribute the over a link, which is already a is unique as it may be recogn independently of other defin like loc_rcvr_status as specif IEEE802.3bw. The WUR is en scrambler stream as defined [14]. The WUR command mu minimum of 64 bits. The det command is left to the imple			
WUP	Wake-up Pulse	The Wake-up pulses (WUP) indicate a wake- up request to the link partner. WUP are link training codes transmitted on the network by a node in tx_mode=SEND_I or switch PHY to distribute the wake-up request over a link, which is down. The activity on the twisted- pair lines will be detected by the partner PHY as a remote wake-up. The wake-up pulse has a minimum duration of 1ms (+/-0.3ms) to allow reliable detection. The energy detection of a WUP command is left to the implementer.		
LPS	Low Power Sleep	The Low Power Sleep (LPS) is a command to indicate a sleep request to the link partner. It is sent by a node requesting a transition to SLEEP, while the link is up. The LPS is encoded in the scrambler stream as defined in section 7.3 of [14]. The LPS command must be send for a minimum of 64 bits. The detection of a LPS command is left to the implementer.		
INH	Inhibit	The high level Inhibit variable describes the state of the inhibit pin.		

Table 1: List of Abbreviations.

ID: 100BASET1_L1_IOP_2

Type: Information

Glossary term	Glossary definition
MAY	This word or the adjective "OPTIONAL", mean that an item is truly optional. One vendor may choose to include the item because a particular marketplace requires it or because the vendor feels that it enhances the product while another vendor may omit the same item. An implementation which does not include a particular option MUST be prepared to interoperate with another implementation which does include the option, though perhaps with reduced functionality. In the same way an implementation which does include a particular option MUST be prepared to interoperate with another implementation which does not include the option (except, of course, for the feature the option provides.)
MUST	This word, or the terms "REQUIRED" or "SHALL", mean that the definition is an absolute requirement of the specification.
MUST NOT	This phrase or the phrase "SHALL NOT", mean that the definition is an absolute prohibition of the specification.
SHOULD	This word, or the adjective "RECOMMENDED", mean that there may exist valid reasons in particular circumstances to ignore a particular item, but the full implications must be understood and carefully weighed before choosing a different course.
SHOULD NOT	This phrase, or the phrase "NOT RECOMMENDED" mean that there may exist valid reasons in particular circumstances when the particular behavior is acceptable or even useful, but the full implications should be understood and the case carefully weighed before implementing any behavior described with this label.
Link status	The link state that is indicated via a PHY's status registers. The link state can be a combination of various PHY status bits.
Link partner	Device that is connected to a Device under Test to perform the interoperability tests. A link partner must use a well-known PHY, PHY configuration and external PHY filter (if necessary).
External PHY filter or external filter.	Additional circuit that is connected directly to the PHY and filters the in- and outgoing physical layer signaling. The PHY vendor typically provides a reference filter design.
PHY configuration	Variable settings that affect the PHY's behavior (e.g., sensitivity of internal equalizers, or shaping of outgoing physical layer signaling). The PHY configuration could be set by an upper layer

Glossary term	Glossary definition
	(e.g., by software) or could be hardcoded, e.g., via dedicated PHY configuration pins.
Test case	Description of one or more test steps and a set of conditions that define whether the observed behavior when executing the test steps matches the expected results.
Test iteration	The execution of all test steps of a given test case.
Test instance	A test instance defines different test parameters for a given test case, such as the DUT's PHY MASTER/SLAVE configuration, or used cable to connect the link partner. The test case itself is not altered.
Soft reset	Reset of a PHY by software, usually triggered by writing to a control register.
Hard reset	Reset of a PHY via a dedicated reset-pin, or by toggling the PHYs power supply.
Channel	Synonym for physical layer communication channel (cf. [4]).
Passive link	Connection between 100BASE-T1 devices without established link-up condition.
Active link	Connection between 100BASE-T1 devices with established link- up condition.

Table 2: List of Definitions.

2.4 Organization of Tests

In this chapter the main structure of the test cases as well as the elementary test cases structure will be introduced.

2.4.1 Elementary test structure

The main structure description of a test case is shown in Table 3. A brief description about the meaning of each field is provided.

Synopsis	A short description of the purpose of the test case is given here.		
Prerequisites A list of requirements and capabilities needed for a proper tests conduction			
Test Setup	The respective test environment setup is specified (e.g. if different test case sequences will require different test system configuration)		
Test procedure	The first note here describes the total sum of test case executions due to setup variations to give the test implementer a first impression of the specific test case. As the second part of the test case execution, the test steps are described dealing with the setup being applied and what is observed and measured at each execution etc. All actions of the test environment shall be described explicitly in this item.		
Pass criteria	In this response cell, a description is given about what is expected as the result. The Pass criteria are also specified in this point.		
Test iterations	Amount of test repetitions. See Appendix - 7.1 Suggested Iterations		
Notes	When necessary a note will be added complementing the information of the test case.		

Table 3 - Main test structure

2.4.2 Test case instances structure

Together with the test definition and all its parameters, the test case instances will also be defined that are part of each test case.

A test case instance can be defined as a repetition of the same test case modifying certain configurations of the DUT and the test environment without losing focus on the test purpose.

Instance Test Case #		Parameter 1	Parameter 2	Parameter 3	 Parameter N
	Parameter A	<label>_IOP_X</label>			
	Parameter B		<label>_IOP_Y</label>		
	Parameter Z			<label>_IOP_Z</label>	

An example definition of a test case is shown in Table 5. In this case, first the behavior of the DUT will be tested when acting as a MASTER with the conditions established by the corresponding test case. Next, the test will be performed with the DUT acting as a SLAVE.

Instance Test Case #	DUT / LP configuration	LP as SLAVE	LP as MASTER
X.X.X.#	DUT as MASTER	100BASET1_L1_IO P_XX_SR_M_S	
X.X.X.#	DUT as SLAVE		100BASET1_L1_IO P_XX_SR_S_M

Table 5 - Example of test case instances

3 Layer 1 Interoperability

3.1 General Requirements

ID: 100BASET1_L1_IOP_3

Type: Information

A Device under Test (DUT) shall be defined by the used PHY/Switch (identified by its manufacturer, model and revision number), the used external filter (if required by the PHY/Switch vendor) and used PHY/Switch configuration.

ID: 100BASET1_L1_IOP_4

Type: Requirement

The PCB layout of the DUT shall adhere to PHY vendor's reference design. In particular, this includes schematic and specific parts installed, power supply, power decoupling and interface between the PHY and microcontroller.

ID: 100BASET1_L1_IOP_5

Type: Requirement

The DUT configuration and software interface used for the IOP tests shall adhere to the specification of the DUT vendor. This requires the DUT vendor to define which registers shall be used, e.g., to evaluate the DUT's link status, to enter in SLEEP mode, to send wake-up requests or to detect the wake-up source.

ID: 100BASET1_L1_IOP_6

Type: Requirement

All monitoring activities (e.g. register readout for active link, wake-up and sleep) shall be done by an interrupt or periodic polling. To ensure to get valid results, the polling period has to be chosen according to the timing requirements of the test case (e.g., much lower than the timing requirement).

ID: 100BASET1_L1_IOP_7

Type: Requirement

For all Layer 1 Interoperability test cases defined in chapter 4 and 6, the DUT shall be tested against a defined set of link partners, unless explicitly defined otherwise in the test case description. A link partner is defined by the same requirements that apply to the DUT. If multiple qualified link partners are available, the test against multiple link partners is mandatory.

ID: 100BASET1_L1_IOP_8

Type: Requirement

For all PHY feature set tests defined in chapter 5, the DUT must be tested against a known link partner. The link partner is defined by the same requirements that apply to the DUT. The link partner configuration must be included in the test results. Tests against additional link partners are optional.

ID: 100BASET1_L1_IOP_9

Type: Requirement

For each test case, the test results shall be documented individually for each combination of DUT and link partner, for each variation point and for each test instance.

ID: 100BASET1_L1_IOP_10

Type: Information

The tests do not necessarily aim at qualifying a single DUT, but the combination of DUT and link partner. This also means that if a test fails, not the DUT's PHY, but the combination of DUT and link partner is faulty. Other DUT/link partner combinations might be free from defects and may qualify.

ID: 100BASET1_L1_IOP_11

Type: Requirement

A link-up condition is defined in terms of the following bits:

- Scrambler Locked (SL);
- Local receiver status (LRS);
- Remote receiver status (RRS);
- Link status bit (LS)

And the PHY status

• PHY_Status (SEND IDLE OR DATA) - PCS Status of IEEE 802.3 Fig 96-18

Link-up-> (SL==1 AND LRS==1 AND RRS==1 AND LS==1) AND PHY_Status == SEND IDLE OR DATA

ID: 100BASET1_L1_IOP_12

Type: Requirement

A link-down condition is defined in terms of the following bits:

- Scrambler Locked (SL);
- Local receiver status (LRS);
- Remote receiver status (RRS);
- Link status bit (LS)

Link-down-> (SL==0 or LRS==0 or RRS==0 or LS==0)

ID: 100BASET1_L1_IOP_13

Type: Requirement

A wake-up condition could be verified by using the service primitive Wake-up.indication.

ID: 100BASET1_L1_IOP_14

Type: Requirement

A sleep condition could be verified by the following two options:

- The INH pin changes its status from one (1) to zero (0).
- Polling the PHYs identification register or any other well known register until its value is no longer available.

3.2 Test coverage / variation points

ID: 100BASET1_L1_IOP_15

Type: Requirement

The tests shall be performed with a "Channel Type 1" and with a "Channel Type 2" as set forth in section 9 of [10]..

ID: 100BASET1_L1_IOP_16

Type: Requirement

The tests shall be performed at an ambient temperature of - 40°C, at room temperature and at an ambient temperature of either + 105°C or + 125°C, according to the maximum ambient operating temperature specified in the DUT datasheet.

ID: 100BASET1_L1_IOP_17

Type: Requirement

A test instance of a test case shall be considered as passed, if no test iteration failed. The number of suggested test iterations is defined in chapter 7.1.

3.3 Channels definition

This definition shall be used for defining a test wiring harness that simulates various communication channels according to the channel definitions of IEEE Std. 802.3bw [1] for interoperability tests of 100Base-T1 transceivers.

3.3.1 Channel Type 1

ID: 100BASET1_L1_IOP_18

Type: Requirement

The parameters of the type 1 channel are derived from the limit definition for a communication channel according to. the channel definitions of [1] and [10].

For setting up a real test harness upper and lower limits are added for each parameter. The type 1 channel implementation shall fulfill these limits at (23±2)°C ambient temperature (RT).

All parameters are defined in Section 9.2 of [10].

3.3.1 Channel Type 2

ID: 100BASET1_L1_IOP_19

Type: Requirement

The Type 2 channel is derived from a 5m link segment scaled from the type 1 cable.

All parameters are defined in Section 9.3 of [10].

3.3.2 Channel Type 3

ID: 100BASET1_L1_IOP_20

Type: Requirement

The Type 3 channel is derived from a 1.5m link segment scaled from the type 1 cable.

All parameters are defined in Section 9.4 of [10].

3.4 Artificial degradation of channel quality

ID: 100BASET1_L1_IOP_21

Type: Requirement

In order to artificially reduce the quality of the communication channel a differential directional coupler shall be inserted between the DUT and the LP introducing differential bandlimited level adjustable Gaussian noise into DUT direction.

On section 7.2 an example for practical implementation can be found.

3.5 Multiple Link Partners

This section describes a concept to adopt multiple link partners, increasing the coverage in terms of diversity of interoperability in the ecosystem without necessarily increasing the test periods and efforts.

ID: 100BASET1_L1_IOP_22

Type: Requirement

Each device having passed the tests listed below could be considered as potential link partner candidate

a) Conformance Tests

- 1. OA- PHY Control Test Suite
- 2. OA- Physical Media Attachment Test Suite
- 3. OA- Physical Coding Sub-layer Test Suite
- b) Interoperability Tests
 - 1. OA- Interoperability Test Suite At least all test cases in groups #1 and # 2; disregarding the *PHY features set tests* chapter (SQI + Diagnostic)

ID: 100BASET1_L1_IOP_23

Type: Requirement

The respective silicon vendors should provide enough samples to be placed in the test system as link partners

ID: 100BASET1_L1_IOP_24

Type: Requirement

"Link-up for starting communication" .

Communication_Link-up_DUT -> (SL_DUT==1 AND LRS_DUT==1 AND RRS_DUT==1 AND LS_DUT==1)

Following information will be logged during the test execution with a resolution of up to 1ms between each signal change:

- Link-up
- scr_status
- loc_rcvr_status
- rem_rcvr_status
- PCS Status of IEEE 802.3 (Fig 40-16a)

This information shall be available with no restrictions from LP and DUT side in order to provide additional information when a failure is observed.

ID: 100BASET1_L1_IOP_25

Type: Requirement

The respective silicon vendors must commit to provide support if interoperability issues are identified and the root cause is unclear for their part to be considered as a link partner for this testing.

ID: 100BASET1_L1_IOP_26

Type: Requirement

A matrix with all LP combination shall be added at the beginning of the report document with a Pass / Fail for each combinations.

4 Test Cases

ID: 100BASET1_L1_IOP_27

Type: Requirement

The test cases defined in this section are mandatory for all 100BASE-T1 PHYs.

4.1 Group 1, Link status *ID:* 100BASET1_L1_IOP_28

Type: Information

The test cases defined in this section shall ensure that the PHY signals the correct link state to upper layers. In particular, a PHY must not signal an active link when no data can be transmitted.

4.1.1 Reliability of indicated link status directly after link-up / PHY reset

ID: 100BASET1_IOP_16

Type: Requirement

Superais	Shall ansure that the data can be transmitted as seen as the DUV signals as estimated
Synopsis	Shall ensure that the data can be transmitted as soon as the PHY signals an active
	link.
Prerequisites	1. DUT with the capability to reset and configure its PHY.
	 DUT is able to indicate a link-up condition via its status registers within 0.5ms after having detected an active link.
	3. DUT must be able to send frames, for that a xMII interface must be available on the DUT:
	 a. if Comm_ready is supported (see [11]) within 1ms after comm ready status is met, otherwise
	 b. within 2ms after detecting a link-up
	and is able to send a new frame each 1ms. This includes any processing time by
	the DUT's application software and networking stack.
	4. DUT and link partner must be able to detect any lost frames by the networking
	stack or by the application.
	The test system must be able to monitor the link status of the DUT and LP during the test iterations.
	6. Link partner, or device that is connected to the link partner, must be able to
	receive all frames sent by the DUT.
Test Setup	DUT must be connected to an active link partner with opposite MASTER/SLAVE
	configuration. Depending on the test instance, the link partner is either connected
	with correct, or with swapped polarity (i.e., DUT ETH_N 🗇 LP ETH_P and DUT
	ETH P \Leftrightarrow LP ETH N).
	LIII_F 🖘 LF LIII_INJ.
Test	1. Link partner shall be active and ready to receive frames.
	 DUT shall soft reset and reconfigure its PHY.
procedure	 If required by PHY vendor: DUT must wait until PHY has accepted
	MASTER/SLAVE configuration.
	4. The DUT's PHY configuration must be finished within 20ms after reset.

	5. DUT shall set an internal <i>counter</i> variable to 0.				
	6. DUT shall wait until the PHY indicates an active link (e.g., by polling the link				
	state or by using an interrupt).				
	7. DUT shall send out a frame with the current counter value 2ms after link-up.				
	Or, if implemented, right after Communication_ready (Comm_ready) status				
	switches from NOT_OK to OK status.				
	8. Every subsequent 1ms, the DUT shall increment its counter variable and				
	send out a frame with the new counter.				
	9. Repeat step 8 until the link partner receives the first frame by the DUT or the				
	link goes down.				
	10. The link partner must store the <i>counter</i> value of the first received frame.				
Pass criteria	If any frames have been lost or discarded above layer 1 (e.g., in the receive/send				
	buffer of the link partner or if the MAC has discarded a frame because of a CRC				
	error), the result of the test iteration must be ignored.				
	Each test iteration shall be classified as passed, if all of the following condition(s) are				
	fulfilled :				
	a = 1 ink partner receives the first frame cent by DUT (counter $= 0$)				
	 Link partner receives the first frame sent by DUT (<i>counter</i> == 0). Link does not go down after test step 5, i.e., link stayed active for the 				
	 Link does not go down after test step 5, i.e., link stayed active for the whole iteration. 				
Test					
iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations				
Notes	Test instance 100BASET1_ IOP_16_SR_S_M_P is only applicable if the DUT's PHY				
	supports automatic polarity detection when configured as SLAVE.				
	· · · · · · · · · · · · · · · · · · ·				

Table 6: Main test structure of 100BASET1_IOP_16

Instance Test Case #	DUT / LP configuration	LP as SLAVE	LP as MASTER	LP is MASTER, LP connected with swapped polarity of ETH_N and ETH_P
4.1.1.1	DUT as SLAVE		100BASET1_IOP_ 16 _SR_S_M	
4.1.1.2	DUT as SLAVE			100BASET1_IOP_16 _SR_S_M_P
4.1.1.3	DUT as MASTER	100BASET1_IOP_16 _SR_M_S		

Table 7: Test case instances of 100BASET1_IOP_16

4.1.2 Reliability of indicated link status when connected to link partner with same MASTER/SLAVE configuration

ID: 100BASET1_IOP_17

Type: Requirement

Synopsis	Shall ensure that the PHY does not signal an active link when connected to a link partner with equal MASTER/SLAVE configuration.
Prerequisites	 DUT with the capability to reset and configure its PHY. DUT is able to detect a link-up
Test Setup	DUT must be connected to an active link partner with equal MASTER/SLAVE configuration.
Test procedure	 Link partner shall be active. DUT shall soft reset and reconfigure its PHY. If required by PHY vendor: DUT must wait until its PHY has accepted MASTER/SLAVE configuration. The DUT's PHY configuration must be finished within 20ms after reset. DUT shall monitor the link status condition for at least 750ms.
Pass criteria	Each test iteration shall be classified as passed, if all of the following condition(s) are fulfilled: • DUT does not detect any link-up condition.
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	-

Table 8: Main test structure of 100BASET1_IOP_17

Instance Test Case #	DUT / LP configuration	LP as SLAVE	LP as MASTER
4.1.2.1	DUT as SLAVE	100BASET1_ IOP_17 _SR_S_S	
4.1.2.2	DUT as MASTER		100BASET1_ IOP_17 _SR_M_M

Table 9: Test case instances of 100BASET1_IOP_17

4.1.3 Reliability of indicated link status when connected to link partner with swapped polarity for PHYs without automatic polarity correction

ID: 100BASET1_IOP_18

Type: Requirement

Synopsis	Shall ensure that the PHY does not signal an active link when connected to a link partner with swapped polarity (i.e., DUT ETH_N ⇔ LP ETH_P and DUT ETH_P ⇔ LP ETH_N). This test is only applicable for PHYs without automatic polarity correction. The test must not be performed for PHYs with automatic polarity correction or for combinations where the LP's PHY supports automatic polarity correction.
Prerequisites	 DUT's PHY has no automatic polarity correction. DUT with the capability to reset and configure its PHY. DUT is able to detect a link-up.
Test Setup	DUT must be connected to an active link partner with opposite MASTER/SLAVE configuration.
Test procedure	 Swap polarity of bus lines (i.e., DUT ETH_N ⇔ LP ETH_P and DUT ETH_P ⇔ LP ETH_N). Link partner shall be active. DUT shall soft reset and reconfigure its PHY. If required by PHY vendor: DUT must wait until its PHY has accepted MASTER/SLAVE configuration. The DUT's PHY configuration must be finished within 20ms after reset. DUT shall monitor the link status condition for at least 750ms.
Pass criteria	 Each test iteration shall be classified as passed, if all of the following condition(s) are fulfilled. DUT does not detect any link-up condition. DUT shall indicate the swapped polarity detection via its registers
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	-

Table 10: Main test structure if 100BASET1_IOP_18

Instance Test Case #	DUT / LP configuration	LP as SLAVE	LP as MASTER
4.1.3.1	DUT as SLAVE		100BASET1_ IOP_18 _SR_S_M_P
4.1.3.2	DUT as MASTER	100BASET1_ IOP_18 _SR_M_S_P	

Table 11: Test case instances of 100BASET1_IOP_18

4.1.4 Revoke of link status after link-down

ID: 100BASET1_IOP_19

Type: Requirement

Synopsis	Shall ensure that the PHY does detect and signal a link-down within a given time limit after the link has been interrupted, e.g., by a reset or power-down of the link partner. The DUT must be tested against at least one known link partner. A test against a complete set of link partners is optional. The link partner configuration must be included in the test results.
Prerequisites	 DUT with the capability to reset and configure its PHY. DUT must be able to read the current link status.
Test Setup	DUT must be connected to an active link partner with opposite MASTER/SLAVE configuration.
Test procedure	 Link partner shall be active. DUT shall soft reset and reconfigure its PHY. If required by PHY vendor: DUT must wait until its PHY has accepted MASTER/SLAVE configuration. The DUT's PHY configuration must be finished within 20ms after reset. Wait until the DUT's PHY signals an active link. Apply in the link partner a permanent hard reset condition and start timer t0. Wait until the DUT's PHY indicated link status changes from link-up to link-down and stop timer t0.
Pass criteria	 Each test iteration shall be classified as passed, if all of the following condition(s) are fulfilled. DUT detected the link-down within 5ms after applying a permanent hard reset condition in the link partner. (t0 <= 5ms).
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	-

Table 12: Main test structure of 100BASET1_IOP_19

Instance Test Case #	DUT / LP configuration	LP as SLAVE	LP as MASTER
4.1.4.1	DUT as SLAVE		100BASET1_ IOP_19 _SR_S_M
4.1.4.2	DUT as MASTER	100BASET1_ IOP_19 _SR_M_S	

Table 13: Test case instances of 100BASET1_IOP_19

4.2 Group 2, Link-up

ID: 100BASET1_L1_IOP_29

Type: Information

The test cases defined in this section shall ensure that the PHY is able to establish an active link after reset and reconfiguration of itself, or of the link partner's PHY.

4.2.1 Link-up after PHY-reset

ID: 100BASET1_IOP_21

Type: Requirement

Synopsis	Shall ensure that the PHY is able to establish a link after being reset and reconfigured
	within a given time limit.
Prerequisites	1. DUT with the capability to reset and configure its PHY.
	2. DUT is able to indicate a link-up condition via its status registers within 0.5ms
	after having detected an active link.
Test Setup	DUT is connected to an active link partner with opposite MASTER/SLAVE
	configuration. Depending on the test instance, the link partner is either connected
	with correct, or with swapped polarity (i.e., DUT ETH_N \Leftrightarrow LP ETH_P and DUT ETH_P
	⇔ LP ETH_N).
Test	1. DUT shall soft-/hard reset and reconfigure its PHY.
procedure	2. The DUT's PHY configuration must be finished within 20ms after reset.
-	3. After finished configuration, the DUT shall start timer t0.
	4. DUT shall wait until the PHY indicates an active link and stop timer t0.
	5. If [LQ.LTT] register, as defined in [11], is supported, once PHY indicates an
	active link read the Linkup Total Time from [LQ.LTT] register; (lcl_rcv AND
	rem rcv).
	6. DUT shall monitor whether the link status remains active for at least 750ms
	after initial link-up.
Pass criteria	Each tast iteration shall be classified as passed, if all of the following condition(s) are
	Each test iteration shall be classified as passed, if all of the following condition(s) are fulfilled.
	runnied.
	 DUT's PHY achieved link-up within 100ms after finished configuration (t0
	c = 100ms).
	 Link did not go down after test step 4.
Test	
iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
iterations	
Notes	Test instances 100BASET1_IOP_21_SR_S_M_P and 100BASET1_IOP_21_HR_S_M_P
140103	
	are only applicable if the DUT's PHY supports automatic polarity detection when
	configured as SLAVE.

Table 14: Main test structure of 100BASET1_IOP_21

Instance Test Case #	DUT / LP configuration	LP as SLAVE	LP as MASTER	LP is MASTER, LP connected with swapped polarity of ETH_N and ETH_P
4.2.1.1	DUT is SLAVE; PHY is soft reset		100BASET1_ IOP_21 _SR_S_M	
4.2.1.2	DUT is SLAVE; PHY is soft reset			100BASET1_ IOP_21 _SR_S_M_P
4.2.1.3	DUT is MASTER PHY is soft reset	100BASET1_ IOP_21 _SR_M_S		
4.2.1.4	DUT is SLAVE; PHY is hard reset		100BASET1_ IOP_21 _HR_S_M	
4.2.1.5	DUT is SLAVE; PHY is hard reset			100BASET1_ IOP_21 _HR_S_M_P
4.2.1.6	DUT is MASTER PHY is hard reset	100BASET1_ IOP_21 _HR_M_S		

Table 15: Test case instances of 100BASET1_IOP_21

4.2.2 Link-up after reset of link partner

ID: 100BASET1_L1_IOP_22

Type: Requirement

Synopsis	Shall ensure that the PHY is able to establish a link after the link partner's PHY has
	been reset and reconfigured within a given time limit.
Prerequisites	 Link partner with the capability to reset and configure its PHY. DUT must be able to trigger the PHY reset of the link partner, or must be able to detect the time of the LP's PHY reset. DUT must be able to detect a link-up within 0.5ms after the PHY indicates an active link via its status registers.
Test Setup	DUT must be connected to an active link partner with opposite MASTER/SLAVE configuration.
Test procedure	 DUT shall soft-/hard reset and reconfigure its PHY. DUT shall trigger a soft-/hard reset of the link partner's PHY or wait until the link partner has reset its PHY. DUT shall start timer t0 directly after the reset of the LP's PHY. The link partner must configure its PHY within 20ms after the reset. DUT must ignore any indicated active links within 25ms after the reset. 25ms after LP's reset: DUT shall wait until the PHY indicates an active link and stop timer t0. The lowest possible indicated link-up time can be 25ms, even if the actual link-up was established quicker. DUT shall monitor whether the link status remains active for at least 750ms after initial link-up.
Pass criteria	 Each test iteration shall be classified as passed, if all of the following condition(s) are fulfilled. DUT's PHY reported link-up within 120ms after reset of the LP's PHY (t0 <= 120ms). Link did not go down after test step 5.
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	Test instances IOP_22_SR_S_M_P and IOP_22_HR_S_M_P are only applicable if the DUT's PHY supports automatic polarity detection when configured as SLAVE.

 Table 16: Main test structure of 100BASET1_IOP_22

Instance Test Case #	DUT / LP configuration	LP is SLAVE; PHY is soft reset	LP is MASTER; PHY is soft reset	LP is SLAVE; PHY is hard reset	LP is MASTER; PHY is hard reset
4.2.2.1	DUT is SLAVE		100BASET1_ IOP_22 _SR_S_M		
4.2.2.2	DUT is SLAVE				100BASET1_ IOP_22 _HR_S_M
4.2.2.3	DUT is SLAVE, LP connected with swapped polarity of ETH_N and ETH_P		100BASET1_ IOP_22 _SR_S_M_P		
4.2.2.4	DUT is SLAVE, LP connected with swapped polarity of ETH_N and ETH_P				100BASET1_ IOP_22 _HR_S_M_P
4.2.2.5	DUT is MASTER	100BASET1_ IOP_22 _SR_M_S			
4.2.2.6	DUT is MASTER			100BASET1_ IOP_22 _HR_M_S	

Table 17: Test case instances of 100BASET1_IOP_22

5 100BASE-T1 PHY features set tests

ID: 100BASET1_L1_IOP_30

Type: Information

The test cases defined in this chapter shall ensure that optional PHY features, such as an estimation of the channel quality or cable diagnostics, provide expected and comparable results under known test conditions. If a PHY supports a given feature, the associated test cases are mandatory. Else, the test case shall be ignored.

5.1 Group 3, Signal Quality

ID: 100BASET1_L1_IOP_31

Type: Information

The tests in this section are only applicable for 100BASE-T1 PHYs that support an estimation of the signal quality of the communication channel. The signal quality can either be read directly from a PHY register, or may be derived based on one or more PHY register values.

5.1.1 Indicated signal quality for channel with decreasing quality

ID: 100BASET1_IOP_24a

Type: Requirement

Synopsis	Shall ensure that the PHY's indicated signal quality decreases for a channel with decreasing channel quality.
Prerequisites	 Test system that allows varying and determining the quality of the communication channel that connects the DUT and LP. DUT must be able to monitor the signal quality indicated by the PHY.
Test Setup	DUT must be connected to an active link partner with opposite MASTER/SLAVE configuration. Test setup shall be able to apply artificial noise to communication channel.
Test procedure	 Remove any artificial channel degradation, to ensure that the highest possible signal quality is reached on both the DUT and LP. DUT shall soft reset and reconfigure its PHY. Measure the PHY's SQI value for at least 100 times. Determine and store the minimum and maximum read values. Increase artificial noise level by one step, i.e. by 100mV Gaussian noise generator amplitude. Repeat steps 3 and 4 until ten additional noise levels after the PHY can no longer establish a link. Draw minimum and maximum curves with the values obtained in each artificial noise step

Pass criteria	 Each test iteration shall be classified as passed, if all of the following condition(s) are fulfilled. SQI values Steadily and monotonic decreased by one step each SQI values are only valid if link-up condition is present Link status Link-up status remains for SQI values higher than 0 No link instabilities with intermittently link drops should be observed between SQI values higher than 0.
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	To guarantee comparability of the results, a graphic disclosing SQI value (y-axis) vs. associated noise level on the network [<i>Vpp</i>] (x axis) shall be given in the test report for each test iteration. The noise level seen by the DUT is relevant; this means the noise source level divided by the coupling factor of the differential directional coupler.

 Table 18: Main test structure of 100BASET1_IOP_24a

Instance Test Case #	DUT / LP configuration	LP is SLAVE; PHY is soft reset	LP is MASTER; PHY is soft reset
	DUT is SLAVE		100BASET1_
5.1.1.1			IOP_24a
			_SR_S_M
	DUT is	100BASET1_	
5.1.1.2	MASTER	IOP_24a	
		_SR_M_S	

Table 19: Test case instances of 100BASET1_IOP_24a

5.1.2 Indicated signal quality for channel with increasing quality

ID: 100BASET1_IOP_24b

Type: Requirement

Synopsis	Shall ensure that the PHY's indicated signal quality increases for a channel with increasing channel quality.		
Prerequisites	 Test system that allows varying and determining the quality of the communication channel that connects the DUT and LP. DUT must be able to monitor the signal quality indicated by the PHY. 		
Test Setup	DUT must be connected to an active link partner with opposite MASTER/SLAVE configuration. Test setup shall be able to apply artificial noise to communication channel.		
Test procedure Pass criteria	 Start with the highest artificial noise channel degradation The DUT's PHY can no longer establish a link. DUT shall soft reset and reconfigure its PHY. Decrease artificial noise level until link can be established. Measure the PHY's SQI value for at least 100 times. Determine and store the minimum and maximum read values. Decrease artificial noise by one step, i.e. by 100mV Gaussian noise generator amplitude. Repeat steps 4 and 5 until no artificial noise is applied. Draw minimum and maximum curves with the values obtained in each artificial noise step. Each test iteration shall be classified as passed, if all of the following condition(s) are fulfilled. 		
	 SQI values Steadily and monotonic increased by one step each SQI values are only valid if link-up condition is present Link Status Link-up status remains for SQI values higher than 0 No link instabilities with intermittently link drops should be observed between SQI values higher than 0. 		
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations		
Notes	To guarantee comparability of the results, a graphic disclosing SQI value (y-axis) vs. associated noise level on the network [Vpp] (x axis) shall be given in the test report for each test iteration. The noise level seen by the DUT is relevant; this means the noise source level divided by the coupling factor of the differential directional coupler.		

Table 20: Main test structure of 100BASET1_IOP_24b

Instance Test Case #	DUT / LP configuration	LP is SLAVE	LP is MASTER
5.1.2.1	DUT is SLAVE		100BASET1_ IOP_24b _SR_S_M
5.1.2.2	DUT is MASTER	100BASET1_ IOP_24b _SR_M_S	

Table 21: Test case instances of 100BASET1_IOP_24b

5.2 Group 4, Cable Diagnosis

5.2.1 Cable diagnostics for error-free channel

ID: 100BASET1_IOP_31

Type: Requirement

Synopsis	Shall ensure that the PHY's cable diagnostic does not indicate a short or open for an error-free channel.
Prerequisites	 DUT must be able to trigger the PHY's cable diagnostic feature. The link partner shall terminate the channel properly. The link partner should not be transmitting any signal (typically "SEND_Z" or as SLAVE).
Test Setup	DUT is connected to a properly terminated link partner.
Test procedure	 DUT shall soft reset and reconfigure its PHY DUT shall start cable diagnostic of its PHY. DUT shall wait until the PHY finished cable diagnostics. DUT shall read out the indicated result.
Pass criteria	 Each test iteration shall be classified as passed, if all of the following condition(s) are fulfilled. Cable diagnostic reported no errors (i.e., no short / open of the bus lines).
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	-

Table 22: Main test structure of 100BASET1_IOP_31

Instance Test Case #	-
5.2.1.1	100BASET1_IOP_31_SR

 Table 23: Main test structures of 100BASET1_IOP_31

5.2.2 Cable diagnostics for near and far end open

ID: 100BASET1_IOP_32

Type: Requirement

Synopsis	Shall ensure that the PHY's cable diagnostic reliably detects an open of one or both of the bus lines. The test shall be performed for both a near end open at the connector of the DUT, and for a far end open at the connector of the LP.		
Prerequisites	 DUT must be able to trigger the PHY's cable diagnostic feature. The link partner shall terminate the channel properly. The link partner should not be transmitting any signal (typically "SEND_Z" or as SLAVE) 		
Test Setup	DUT is connected to a properly terminated link partner. One or both of the bus wires have a near or far end open.		
Test procedure	 DUT shall soft reset and reconfigure its PHY. DUT shall start cable diagnostic of its PHY. DUT shall wait until the PHY finished cable diagnostics. DUT shall read out the indicated result. 		
Pass criteria	 Each test iteration shall be classified as passed, if all of the following condition(s) are fulfilled. Cable diagnostic reported an open of the bus line(s). 		
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations		
Notes	For a near end open, one or both bus lines shall be disconnected directly at the connector of the DUT. For a far end open, one or both bus lines shall be disconnected directly at the connector of the LP.		

Table 24: Main test structure of 100BASET1_IOP_32

Instance Test Case #	DUT / LP configuration	Test setup	Open is on ETH_N or ETH_P	Open on both ETH_N and ETH_P
5.2.2.1	DUT is SLAVE	Near-end open (on connector of DUT).	100BASET1_IOP_32 _SR_O1_NEAR_S_M	
5.2.2.2	DUT is SLAVE	Near-end open (on connector of DUT).		100BASET1_IOP_32 _SR_O2_NEAR_S_M
5.2.2.3	DUT is SLAVE	Far-end open (on connector of LP).	100BASET1_ IOP_32 _SR_O1_FAR_S_M	
5.2.2.4	DUT is SLAVE	Far-end open (on connector of LP).		100BASET1_IOP_32 _SR_O2_FAR_S_M
5.2.2.5	DUT is MASTER	Near-end open (on connector of DUT).	100BASET1_ IOP_32 _SR_01_NEAR_M_S	
5.2.2.6	DUT is MASTER	Near-end open (on connector of DUT).		100BASET1_IOP_32 _SR_O2_NEAR_M_S
5.2.2.7	DUT is MASTER	Far-end open (on connector of LP).	100BASET1_IOP_32 _SR_O1_FAR_M_S	
5.2.2.8	DUT is MASTER	Far-end open (on connector of LP).		100BASET1_ IOP_32 _SR_O2_FAR_M_S

Table 25: Test case instances of 100BASET1_IOP_32

5.2.3 Cable diagnostics for near and far end short

ID: 100BASET1_IOP_33

Type: Requirement

Synopsis	Shall ensure that the PHY's cable diagnostic reliably detects a short of the bus lines. The test shall be performed for both a near end short at the connector of the DUT, and for a far end short at the connector of the LP.		
Prerequisites	 DUT must be able to trigger the PHY's cable diagnostic feature. The link partner shall terminate the channel properly. The link partner should not be transmitting any signal (typically "SEND_Z" or as SLAVE) 		
Test Setup	 DUT is connected to a properly terminated link partner. The bus wires are connected via a <= 1 Ohm resistor to: SHORT between both bus wires, far and near end. SHORT of both conductors to ground (GND), far and near end. SHORT of both conductors to supply line (VBAT), far and near end. 		
Test procedure	 DUT shall soft reset and reconfigure its PHY. DUT shall start cable diagnostic of its PHY. DUT shall wait until the PHY finished cable diagnostics. DUT shall read out the indicated result. 		
Pass criteria	 Each test iteration shall be classified as passed, if all of the following condition(s) are fulfilled. Cable diagnostic reported a short between the bus wires and to ground or supply line. 		
Test iterations	See suggested test iterations in Appendix – 7.1 Suggested Iterations		
Notes	For a near end short, both bus lines and to ground or battery (see respective test instances Table) shall be connected via a <= 1 Ohm resistor directly at the connector of the DUT. For a far end short, both bus lines shall be connected via a <= 1 Ohm resistor directly at the connector of the LP.		

Table 26: Main test structure of 100BASET1_IOP_33

Instance Test Case #	DUT / LP configuration	Test setup	
5.2.3.1	DUT is SLAVE	Near-end short (on connector of DUT).	100BASET1_ IOP_33 _SR_NEAR_S_M
5.2.3.2	DUT is SLAVE	Far-end short (on connector of LP).	100BASET1_ IOP_33 _SR_FAR_S_M
5.2.3.3	DUT is SLAVE	Near-end short (on connector of DUT).	100BASET1_ IOP_33 _SR_NEAR_GND_S_M
5.2.3.4	DUT is SLAVE	Far-end short (on connector of LP).	100BASET1_ IOP_33 _SR_FAR_GND_S_M
5.2.3.5	DUT is SLAVE	Near-end short (on connector of DUT).	100BASET1_ IOP_33 _SR_NEAR_VBAT_S_M
5.2.3.6	DUT is SLAVE	Far-end short (on connector of LP).	100BASET1_ IOP_33 _SR_FAR_VBAT_S_M
5.2.3.7	DUT is MASTER	Near-end short (on connector of DUT).	100BASET1_ IOP_33 _SR_NEAR_M_S
5.2.3.8	DUT is MASTER	Far-end short (on connector of LP).	100BASET1_ IOP_33 _SR_FAR_M_S
5.2.3.9	DUT is MASTER	Near-end short (on connector of DUT).	100BASET1_ IOP_33 _SR_NEAR_GND_M_S
5.2.3.10	DUT is MASTER	Far-end short (on connector of LP).	100BASET1_ IOP_33 _SR_FAR_GND_M_S
5.2.3.11	DUT is MASTER	Near-end short (on connector of DUT).	100BASET1_ IOP_33 _SR_NEAR_VBAT_M_S
5.2.3.12	DUT is MASTER	Far-end short (on connector of LP).	100BASET1_ IOP_33 _SR_FAR_VBAT_M_S

Table 27: Test case instances of 100BASET1_IOP_33

6 Wake-up/Sleep

ID: WAKE_IOP_1

Type: Requirement

The test cases defined in this section except WAKE_IOP_8 are mandatory for all 100BASE-T1 devices supporting the wake-up/sleep functionality defined in [14]. WAKE_IOP_8 is mandatory if the PHY supporting wakeup and sleep signaling over dedicated I/O pins.

6.1 Group 5, Wake-up reception and signalizing *ID:* WAKE_IOP_2

Type: Information

The test cases defined in this section shall ensure that a wake-up (WUP/WUR) can be received and signalized to the upper layer as described in [14].

6.1.1 Reception of a wake-up pulse (WUP)

ID: WAKE_IOP_3

Synopsis	 Shall ensure that a DUT is able to receive a WUP over a passive link, signalize the wake-up event and upon this to establish a link within an expected time. Parameters to be measured: t_wkp_unpwrd: Time between wake-up request on the LP and DUT wake-up
	signalization.
	 t_wkp_link-up: Time between DUT wake-up signalization and link-up. Link stability after a wake-up condition.
Prerequisites	 DUT with the capability to reset and configure its PHYs. DUT with the capability to set its PHYs into sleep mode. Link partner, or device that is connected to the DUT, shall be able to send a wake-up pulse (WUP). The test system shall be able of providing time measurement capabilities synchronized with the test steps events.
Test Setup	 DUT DUT_P1 Passive link [P1_P1 LP1] DUT shall be connected to a link partner (LP1) with a passive link with opposite MASTER/SLAVE configuration. DUT shall be in sleep state. LP1 including LP1_P1 shall be powered and connected to the DUT with a passive link.
Test	1. Reset timer t ₀

procedure	 Trigger a wake-up request on LP1 Start timer t₀ Wait until the DUT signalizes a wake-up condition Readout timer value (t_wkp_unpwrd = t₀) Configuration of the DUT must be finished within 20ms after wake-up. Wait until DUT signalizes a link-up condition Readout timer value (t_wkp_link-up = t₀ - t_wkp_unpwrd - 20ms (configuration time)) Monitor the link status for additional 750ms
Pass criteria	 For all the executed iterations the following pass criterion shall be fulfilled: t_wkp_unpwrd < TWU_Link_Passive + T_Powersupply_Stable + T_PHY_Initialization t_wkp_unpwrd < 17 ms t_wkp_link-up ≤ 100 ms No link drop is observed after link-up condition has been reached.
Test iterations	See suggested test iterations in Appendix- 7.1 Suggested Iterations
Notes	The test shall be executed for each DUT 100BASE-T1 port

Table 28: Main test structure of WAKE_IOP_3

Instance Test Case #	DUT / LP configuration	LP as SLAVE	LP as MASTER	LP is MASTER, LP connected with swapped polarity of ETH_N and ETH_P
6.1.1.1	DUT as SLAVE		WAKE_IOP_ 3_S_M	
6.1.1.2	DUT as MASTER	WAKE_IOP_ 3_M_S		
6.1.1.3	DUT as SLAVE			WAKE_IOP_ 3_S_M_P

Table 29: Test case instances of WAKE_IOP_3

6.1.2 Reception of a wake-up request (WUR) ID: WAKE_IOP_4

Type: Requirement

Synopsis	Shall ensure that DUT is able to receive a WUR over an active link and to signalize it.				
	Parameter to be measured:				
	 TWU_Link_active: Wake-up transmission time over an active link. 				
	 Link stability during and after WUR event. 				
Prerequisites	1. DUT with the capability to reset and configure its PHYs.				
	2. Link partner, or device that is connected to the DUT, shall be able to send a				
	wake-up request (WUR).				
	3. The test system shall be able of providing time measurement capabilities				
Toot Setur	synchronized with the test steps events.				
Test Setup					
	DUT DUT DA Active link LD4 D4 LD4				
	 DUT shall be connected to an active link partner (LP1) with opposite MASTER/SLAVE configuration. 				
	 A stable link-up condition shall be present at the moment of starting the test 				
	execution.				
Test	1. Reset timer t_0				
procedure	 Trigger a wake-up request on LP1 				
p	3. Start timer t_0				
	4. Wait until the DUT signalizes a wake-up condition				
	5. Readout timer value ($TWU_Link_active = t_0$)				
	6. Monitor the link status for additional 750ms				
Pass criteria	For all the executed iterations the following pass criterion shall be fulfilled:				
	• <i>TWU_Link_active</i> < 2 ms				
	 No link drop is observed during the test execution. 				
Test					
iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations				
Notes	The test shall be executed for each DUT 100BASE-T1 port				
	· ·				

Table 30: Main test structure of WAKE_IOP_4

Instance Test Case #	DUT / LP configuration	LP as SLAVE	LP as MASTER
6.1.2.1	DUT as SLAVE		WAKE_IOP_4_S_M
6.1.2.2	DUT as MASTER	WAKE_IOP_4_M_S	

Table 31: Test case instances of WAKE_IOP_4

6.1.3 Reception of a wake-up pulse (WUP) on an already active DUT *ID:* WAKE_IOP_5

Synopsis	Shall ensure that a DUT is able to receive a WUP over a passive link, signalize the			
	wake-up event and upon this to establish a link while another DUT's port link is			
	already established.			
	Parameters to be measured:			
	• <i>TWU_Link_passive</i> : Wake-up transmission time over a passive link.			
	 <i>t_wkp_link-up</i>: Time between DUT wake-up signalization and link-up. 			
	Link stability after a wake-up condition.			
Prerequisites	 DUT shall have more than one port. DUT with the capability to reset and configure its DUYs. 			
	 DUT with the capability to reset and configure its PHYs. DUT with the capability to set its PHYs into sleep mode. 			
	4. Link partner, or device that is connected to the DUT, shall be able to send a			
	wake-up pulse (WUP).			
	 Link partner shall have local wake-up input available. The test system shall be able of providing time measurement capabilities 			
	synchronized with the test steps events.			
Test Setup				
	DUT DUT_P1 Passive link LP1_P1 LP1			
	DUT shall be connected to a link northern (LD1) with a passive link with			
	 DUT shall be connected to a link partner (LP1) with a passive link with opposite MASTER/SLAVE configuration. 			
	 LP1 including LP1_P1 shall be powered and connected to the DUT with a 			
	passive link.			
	 DUT including DUT_P1 shall be powered and connected to the LP1 with a passive link. 			
Test	1. Reset timer t_0			
procedure	 Trigger a wake-up request on LP1 			
	3. Start timer t_0			
	4. Wait until the DUT signalizes a wake-up condition			
	 Readout timer value (<i>TWU_Link_passive</i> = t₀) Configuration of the DUT must be finished within 20ms after wake-up. 			
	 Wait until DUT signalizes a link-up condition 			
	8. Readout timer value $(t_wkp_link_up = t_0 - TWU_link_passive - 20ms$			
	(configuration time))			
	 Configuration of the DUT must be finished within 20ms after wake-up. Monitor the link status for additional 750ms 			
Pass criteria	For all the executed iterations the following pass criterion shall be fulfilled:			
	• TWU_Link_passive < 2 ms			
	• $t_w kp_link_up \le 100 \text{ ms}$			

	 No link drop is observed after link-up condition has been reached.
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	Test can be skipped for DUTs with one port.
	The test shall be executed for each DUT 100BASE-T1 port

Table 32: Main test structure of WAKE_IOP_5

Instance Test Case #	DUT / LP configuration	LP as SLAVE	LP as MASTER
6.1.3.1	DUT as SLAVE		WAKE_IOP_ 5_S_M
6.1.3.2	DUT as MASTER	WAKE_IOP_ 5_M_S	

Table 33: Test case instances of WAKE_IOP_5

6.2 Group 6, Wake-up transmission *ID:* WAKE_IOP_6

Type: Information

The test cases defined in this section shall ensure that a wake-up (WUP/WUR) can be transmitted and signaled to the upper layer as described in [14].

6.2.1 Transmission of a wake-up pulse (WUP) ID: WAKE_IOP_7

Synopsis	Shall ensure that the DUT is able to send a WUP over a passive link within an expected time and to properly signalize the action.
	Parameters to be measured:
	 TWU_forward_passive: Time between local wake-up event on the DUT and LP1 wake-up signalization. t_wkp_link-up : Time between DUT wake-up signalization and link-up. Link stability after a wake-up condition.
Prerequisites	1. DUT with the capability to reset and configure its PHYs.
	 DUT with the capability to set its PHYs into sleep mode. Link partner, or device that is connected to the DUT, shall be able to receive a
	wake-up pulse (WUP).
	 DUT implementation shall have local wake-up input available. The test system shall be able of providing time measurement capabilities
	synchronized with the test steps events.
Test Setup	 DUT DUT_P1 Passive link LP1_P1 LP1 DUT shall be connected to a link partner (LP1) with a passive link with opposite MASTER/SLAVE configuration. LP1 including LP1_P1 shall be powered and connected to the DUT with a passive link. DUT including DUT_P1 shall be powered and connected to the LP1 with a passive link.
Test procedure	 Reset timer t₀ Trigger a wake-up request on DUT
F	3. Start timer t_0
	 Wait until LP1 signalizes a wake-up condition Readout timer value (TWU link passive = t₀)
	 Readout timer value (TWU_link_passive = t₀) Configuration of the DUT must be finished within 20ms after wake-up.
	 Wait until DUT signalizes a link-up condition

	 8. Readout timer value (t_wkp_link-up = t₀-TWU_link_passive- 20ms (configuration time)) 9. Monitor the link status for additional 750ms
Pass criteria	 For all the executed iterations the following pass criterion shall be fulfilled: TWU_link_passive < 2 ms t_wkp_link-up ≤ 100 ms No link drop is observed after link-up condition has been reached.
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	The test shall be executed for each DUT 100BASE-T1 port

Table 34: Main test structure of WAKE_IOP_7

Instance Test Case #	DUT / LP configuration	LP as SLAVE	LP as MASTER	LP is MASTER, LP connected with swapped polarity of ETH_N and ETH_P
6.2.1.1	DUT as SLAVE		WAKE_IOP_ 7_S_M	
6.2.1.2	DUT as MASTER	WAKE_IOP_ 7_M_S		
6.2.1.3	DUT as SLAVE			WAKE_IOP_ 7_S_M_P

Table 35: Test case instances of WAKE_IOP_7

6.2.2 Transmission of a wake-up pulse after local wake-up (WUP) ID: WAKE_IOP_8

Synopsis	Shall ensure that the DUT is able to send a WUP over a passive link within an				
- ,	expected time and to properly signalize the action.				
	Parameters to be measured:				
	• <i>t_wkp_unpwrd</i> : Time between local wake-up event on the DUT and LP1				
	wake-up signalization.				
	 t_wkp_link-up : Time between DUT wake-up signalization and link-up. 				
	 Link stability after a wake-up condition. 				
Prerequisites	1. DUT with the capability to reset and configure its PHYs.				
	2. DUT with the capability to set its PHYs into sleep mode.				
	3. Link partner, or device that is connected to the DUT, shall be able to receive a				
	wake-up pulse (WUP).				
	 DUT implementation shall have local wake-up input available. The test system shall be able of providing time measurement capabilities 				
	synchronized with the test steps events.				
	6. The DUT provides a local wake-up pin.				
Test Setup					
	Local_Wkp DUT DUT_P1 Passive link LP1_P1 LP1				
	• DUT shall be connected to a link partner (LP1) with a passive link with				
	opposite MASTER/SLAVE configuration.				
	DUT shall be in sleep state.				
	 LP1 including LP1_P1 shall be powered and connected to the DUT with a 				
	passive link.				
Test	1. Reset timer t_0				
procedure	 Apply a local wake pulse to DUT for at least 50us Start timer t₀ 				
	 4. Wait until LP1 signalizes a wake-up condition 				
	5. Readout timer value $(t_wkp_unpwrd = t_0)$				
	 Configuration of the DUT must be finished within 20ms after wake-up. 				
	7. Wait until DUT signalizes a link-up condition				
	8. Readout timer value $(t_wkp_link-up = t_0 - t_wkp_unpwrd - 20ms$				
	(configuration time))				
	9. Monitor the link status for additional 750ms				
Pass criteria	For all the executed iterations the following pass criterion shall be fulfilled:				
	 t_wkp_unpwrd < TWU_WakeIO + TWU_Link_passive + 				
	(T_Powersupply_Stable + T_PHY_Initialization)				
	$t_wkp_unpwrd < 1ms + 2ms + (15ms)$				
	t_wkp_unpwrd < 18 ms				
	• $t_w k p_link - up \le 100 \text{ ms}$				
	 No link drop is observed after link-up condition has been reached. 				

Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	The test shall be executed for each DUT 100BASE-T1 port

Table 36: Main test structure of WAKE_IOP_8

Instance Test Case #	DUT / LP configuration	LP as SLAVE	LP as MASTER
6.2.2.1	DUT as SLAVE		WAKE_IOP_ 8_S_M
6.2.2.2	DUT as MASTER	WAKE_IOP_ 8_M_S	

Table 37: Test case instances of WAKE_IOP_8

6.2.3 Transmission of a wake-up request (WUR)

ID: WAKE_IOP_9

Type: Requirement

Synopsis	Shall ensure that the DUT is able to send a WUR over an active link.				
	Parameters to be measured:				
	• TWILL Link, active: Wake up transmission time over an active link				
	 <i>TWU_Link_active</i>: Wake-up transmission time over an active link. Link stability after a wake-up condition. 				
Prerequisites	1. DUT with the capability to reset and configure its PHYs.				
	 Link partner, or device that is connected to the DUT, shall be able to receive a wake-up request (WUR). 				
	 The test system shall be able of providing time measurement capabilities synchronized with the test steps events. 				
Test Setup					
Tort	 DUT DUT_P1 Active link LP1_P1 LP1 DUT shall be connected to an active link partner (LP1) with opposite MASTER/SLAVE configuration. A link-up condition shall be present at the moment of starting the test execution. 				
Test procedure	 Reset timer t₀ Trigger a WUR on the DUT 				
p. occurre	3. Start timer t_0				
	 Wait until the LP1 signalizes a wake-up condition Readout timer value (<i>TWU_Link_active</i> = t₀) 				
Pass criteria	For all the executed iterations the following pass criterion shall be fulfilled:				
	• TWU_Link_active < 2 ms				
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations				
Notes	The test shall be executed for each DUT 100BASE-T1 port				

 Table 38: Main test structure of WAKE_IOP_9

Instance Test Case #	DUT / LP configuration	LP as SLAVE	LP as MASTER
6.2.3.1	DUT as SLAVE		WAKE_ IOP_9_S_M
6.2.3.2	DUT as MASTER	WAKE_ IOP_9_M_S	

Table 39: Test case instances of WAKE_IOP_9

6.3 Group 7, Wake-up forwarding

ID: WAKE_IOP_10

Type: Information

The test cases defined in this section shall ensure that a wake-up request can be forwarded as described in [14].

This section applies for multi-port DUTs.

6.3.1 Forwarding wake-up request from active to passive link ID: WAKE_IOP_11

Synopsis	Shall ensure that a wake-up request received by a DUT over an active link can be		
	forwarded within the expected time to a LP via a passive link.		
	Parameters to be measured:		
	 t_wkp_fwd: Time between triggering the WUR on LP2 and LP1 wake-up signalization. 		
Prerequisites	 DUT shall have more than one port. DUT with the capability to reset and configure its PHYs. DUT with the capability to set its PHYs into sleep mode. Link partner, or device that is connected to the DUT, shall be able to send and receive a wake-up pulse (WUP). The test system shall be able of providing time measurement capabilities synchronized with the test steps events. 		
Test Setup	 DUT ports shall be connected to their LPs with opposite MASTER/SLAVE configuration. DUT port <i>DUT_P1</i> shall be connected to LP1. LP1 including LP1_P1 shall be powered and the link between DUT_P1 and LP1_P1 shall be passive at the moment of starting the test execution. DUT port <i>DUT_P2</i> shall be connected to LP2. LP2 shall be in normal mode and the link between DUT_P2 and LP2_P1 shall be active at the moment of starting the test execution. 		
Test	1. Reset timer t_0		

procedure Pass criteria	 Trigger a WUR on LP2 Start timer t₀ Wait until the LP1 signalizes a wake-up condition Readout timer value (t_wkp_fwd = t₀) Each test iteration shall be classified as pass, if all of the following condition(s) are
	 fulfilled : t_wkp_fwd < TWU_Link_active + TWU_Forwarding + TWU_Link_passive t_wkp_fwd < 2ms + 1ms + 2ms t_wkp_fwd < 5ms
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	The test shall be executed for each DUT 100BASE-T1 port

Table 40: Main test structure of WAKE_IOP_11

Instance Test Case #	DUT / LP configuration	LP1 as SLAVE, LP2 as SLAVE	LP1 as MASTER, LP2 as MASTER	LP1 as MASTER, LP2 as SLAVE	LP1 as SLAVE, LP2 as MASTER
6.3.1.1	DUT_P1 as SLAVE, DUT_P2 as MASTER			WAKE_ IOP_11_SM_MS	
6.3.1.2	DUT_P1 as MASTER, DUT_P2 as SLAVE				WAKE_ IOP_11_MS_SM
6.3.1.3	DUT_P1 as MASTER, DUT_P2 as MASTER	WAKE_ IOP_11_MM_S S			
6.3.1.4	DUT_P1 as SLAVE, DUT_P2 as SLAVE		WAKE_ IOP_11_SS_MM		

Table 41: Test case instances of WAKE_IOP_11

6.3.2 Forwarding a wake-up request from active to active link *ID:* WAKE_IOP_12

forwarded within the expected time to a LP via an active link. Parameters to be measured: • t_wkp_fwd: Time between triggering the WUR on LP2 and LP1 wake-up signalization. Prerequisites 1. DUT shall have more than one port. 2. DUT with the capability to reset and configure its PHYs. 3. DUT with the capability to reset and configure its PHYs. 4. Link partner, or device that is connected to the DUT, shall be able to receive a wake-up request (WUR). 5. The test system shall be able of providing time measurement capabilities synchronized with the test steps events. Test Setup • DUT ports shall be connected to their LPs with opposite MASTER/SLAVE configuration. • DUT port shall be connected to LP1. • LP1 shall be powered and the link between DUT_P1 and LP1_P1 shall be active at the moment of starting the test execution. • DUT port DUT_P2 test shall be connected to LP2. • LP2 shall be in normal mode and the link between DUT_P2 and LP2_P1 shall be active at the moment of starting the test execution. • DUT port DUT_P2 test shall be connected to LP2. • LP2 shall be in normal mode and the link between DUT_P2 and LP2_P1 shall be active at the moment of starting the test execution. • DUT port DUT_P2 test shall be connected to LP2. • LP2 shall be in normal mode and the link between DUT_P2 and LP2_P1 shall be active at the moment of starting the test execution. • DUT port DUT_P2	Superaie	Shall ansure that a wake up request received by a DUT over an active link can be				
Parameters to be measured: • t_wkp_fwd: Time between triggering the WUR on LP2 and LP1 wake-up signalization. Prerequisite 1. DUT shall have more than one port. 2. DUT with the capability to reset and configure its PHYs. 3. DUT with the capability to reset and configure its PHYs. 3. DUT with the capability to reset and configure its PHYs. 3. DUT with the capability to reset and configure its PHYs. 3. DUT with the capability to reset and configure its PHYs. 5. The test system shall be able of providing time measurement capabilities synchronized with the test steps events. Test Setup • DUT ports shall be connected to their LPs with opposite MASTER/SLAVE configuration. • DUT port bUT_P1 test shall be connected to LP1. • LP1 shall be powered and the link between DUT_P1 and LP1_P1 shall be active at the moment of starting the test execution. • DUT port DUT_P2 test shall be connected to LP2. • LP2 shall be in normal mode and the link between DUT_P2 and LP2_P1 shall be active at the moment of starting the test execution. • DUT port DUT_P2 test shall be connected to LP2. • LP2 shall be in normal mode and the link between DUT_P2 and LP2_P1 shall be active at the moment of starting the test execution. • DUT port DUT_P2 test shall be connected to LP2. • LP2 shall be in normal mode and the link between DUT_P2 and LP2_P1 shall be active at the moment of starting the test execution.	Synopsis					
e t_wkp_fwd: Time between triggering the WUR on LP2 and LP1 wake-up signalization. Prerequisites 1. DUT shall have more than one port. 2. DUT with the capability to reset and configure its PHYs. 3. DUT with the capability to set its PHYs into sleep mode. 4. Link partner, or device that is connected to the DUT, shall be able to receive a wake-up request (WUR). 5. The test system shall be able of providing time measurement capabilities synchronized with the test steps events. Test Setup DUT ports shall be connected to their LPs with opposite MASTER/SLAVE configuration. DUT ports bhall be connected to their LPs with opposite MASTER/SLAVE configuration. DUT port DUT_P1 test shall be connected to LP1. LP1 shall be powered and the link between DUT_P1 and LP1_P1 shall be active at the moment of starting the test execution. DUT port DUT_P2 test shall be connected to LP2. LP2 shall be in normal mode and the link between DUT_P2 and LP2_P1 shall be active at the moment of starting the test execution. DUT port DUT_P2 test shall be connected to LP2. LP2 shall be in normal mode and the link between DUT_P2 and LP2_P1 shall be active at the moment of starting the test execution. DUT port SubJ on LP2 Start timer to Readout timer value (t_wkp_fwd = t_0) Pass criteria Each test iteration shall be classified as pass, if all of the following condition(s) are fulfilled : t_wkp_fwd < TWU_Link_active + TWU_Forwarding + TWU_Link_active <th></th> <th colspan="3">forwarded within the expected time to a LP via an active link.</th>		forwarded within the expected time to a LP via an active link.				
e t_wkp_fwd: Time between triggering the WUR on LP2 and LP1 wake-up signalization. Prerequisites 1. DUT shall have more than one port. 2. DUT with the capability to reset and configure its PHYs. 3. DUT with the capability to set its PHYs into sleep mode. 4. Link partner, or device that is connected to the DUT, shall be able to receive a wake-up request (WUR). 5. The test system shall be able of providing time measurement capabilities synchronized with the test steps events. Test Setup DUT ports shall be connected to their LPs with opposite MASTER/SLAVE configuration. DUT ports bhall be connected to their LPs with opposite MASTER/SLAVE configuration. DUT port DUT_P1 test shall be connected to LP1. LP1 shall be powered and the link between DUT_P1 and LP1_P1 shall be active at the moment of starting the test execution. DUT port DUT_P2 test shall be connected to LP2. LP2 shall be in normal mode and the link between DUT_P2 and LP2_P1 shall be active at the moment of starting the test execution. DUT port DUT_P2 test shall be connected to LP2. LP2 shall be in normal mode and the link between DUT_P2 and LP2_P1 shall be active at the moment of starting the test execution. DUT port SubJ on LP2 Start timer to Readout timer value (t_wkp_fwd = t_0) Pass criteria Each test iteration shall be classified as pass, if all of the following condition(s) are fulfilled : t_wkp_fwd < TWU_Link_active + TWU_Forwarding + TWU_Link_active <th></th> <th colspan="4"></th>						
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 4. Wait until the LP1 signalizes a wake-up condition 5. Readout timer value (t_wkp_fwd = t_0) Pass criteria Each test iteration shall be classified as pass, if all of the following condition(s) are fulfilled : t_wkp_fwd < TWU_Link_active + TWU_Forwarding + TWU_Link_active 	procedure					
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 t_wkp_fwd < TWU_Link_active + TWU_Forwarding + TWU_Link_active 						
		 t wkp fwd < TWU Link active + TWU Forwarding + TWU Link active 				
		$t_wkp_fwd < 2ms + 1ms + 2ms$				
$t_w kp_f wd < 5 ms$						

Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	The test shall be executed for each DUT 100BASE-T1 port
	Table 42: Main test structure of MAKE JOB 12

 Table 42: Main test structure of WAKE_IOP_12

Instance Test Case #	DUT / LP configuration	LP1 as SLAVE, LP2 as SLAVE	LP1 as MASTER, LP2 as MASTER	LP1 as MASTER, LP2 as SLAVE	LP1 as SLAVE, LP2 as MASTER
6.3.2.1	DUT_P1 as SLAVE, DUT_P2 as MASTER			WAKE_ IOP_12_SM_MS	
6.3.2.2	DUT_P1 as MASTER, DUT_P2 as SLAVE				WAKE_ IOP_12_MS_SM
6.3.2.3	DUT_P1 as MASTER, DUT_P2 as MASTER	WAKE_ IOP_12_MM_S S			
6.3.2.4	DUT_P1 as SLAVE, DUT_P2 as SLAVE		WAKE_ IOP_12_SS_MM		

Table 43: Test case instances of WAKE_IOP_12

6.3.3 Forwarding a wake-up request from passive to active link *ID:* WAKE_IOP_13

Cum an ata	Chall around that a wake up request reactional buy DUT around reaction that we have				
Synopsis	Shall ensure that a wake-up request received by a DUT over a passive link can be				
	forwarded within the expected time to a LP via an active link.				
	Parameters to be measured:				
	• t_wkp_fwd: Time between triggering the WUR on LP1 and LP2 wake-up				
	signalization.				
Prerequisites	1. DUT shall have more than one port.				
er equilortes	 DUT with the capability to reset and configure its PHYs. 				
	3. DUT with the capability to set its PHYs into sleep mode.				
	4. Link partner, or device that is connected to the DUT, shall be able to receive a				
	wake-up request (WUR).				
	5. The test system shall be able of providing time measurement capabilities				
	synchronized with the test steps events.				
Test Setup					
	DUT_P1 DUT_P2 Active ink				
	LP1_P1 LP2_P1				
	LP1 LP2				
	 DUT ports shall be connected to their LPs with opposite MASTER/SLAVE 				
	configuration.				
	 DUT port <i>DUT_P1</i> test shall be connected to LP1. LP1 including LP1_P1 shall be powered and the link between DUT_P1 and 				
	LP1_P1 shall be passive at the moment of starting the test execution.				
	 DUT port <i>DUT_P2</i> test shall be connected to LP2. 				
	 LP2 shall be in normal mode and the link between DUT_P2 and LP2_P1 shall 				
	be active at the moment of starting the test execution.				
Test	1. Reset timer t_0				
procedure	 Trigger a wake-up request on LP1 				
procedure	3. Start timer t_0				
	4. Wait until the LP2 signalizes a wake-up condition				
	5. Readout timer value $(t_wkp_fwd = t_0)$				
Pass criteria	Each test iteration shall be classified as pass, if all of the following condition(s) are				
	fulfilled :				
	 t_wkp_fwd < TWU_Link_passive + TWU_Forwarding + TWU_Link_active 				
	<i>t_wkp_fwd</i> < 2ms + 1ms + 2ms				
	t_wkp_fwd < 5ms				

Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	The test shall be executed for each DUT 100BASE-T1 port
8	Table 44. Moin test structure of MAKE IOD 12

 Table 44: Main test structure of WAKE_IOP_13

Instance Test Case #	DUT / LP configuration	LP1 as SLAVE, LP2 as SLAVE	LP1 as MASTER, LP2 as MASTER	LP1 as MASTER, LP2 as SLAVE	LP1 as SLAVE, LP2 as MASTER
6.3.3.1	DUT_P1 as SLAVE, DUT_P2 as MASTER			WAKE_ IOP_13_SM_MS	
6.3.3.2	DUT_P1 as MASTER, DUT_P2 as SLAVE				WAKE_ IOP_13_MS_SM
6.3.3.3	DUT_P1 as MASTER, DUT_P2 as MASTER	WAKE_ IOP_13_MM _SS			
6.3.3.4	DUT_P1 as SLAVE, DUT_P2 as SLAVE		WAKE_ IOP_13_SS_MM		

Table 45: Test case instances of WAKE_IOP_13

6.3.4 Forwarding a wake-up request from passive to passive link *ID:* WAKE_IOP_14

Cumonsis	Chall answe that a wake we wanted to ask and have DUT as a sector that we have				
Synopsis	Shall ensure that a wake-up request received by a DUT over a passive link can be				
	forwarded within the expected time to a LP via a passive link.				
	Darameters to be measured:				
	Parameters to be measured:				
	• t_wkp_fwd: Time between triggering the WUR on LP1 and LP2 wake-up				
	signalization.				
Prerequisites	1. DUT shall have more than one port.				
Frerequisites	 DUT with the capability to reset and configure its PHYs. 				
	 DUT with the capability to set its PHYs into sleep mode. 				
	 Link partner, or device that is connected to the DUT, shall be able to receive a 				
	wake-up pulse (WUP).				
	5. The test system shall be able of providing time measurement capabilities				
	synchronized with the test steps events.				
Test Setup					
rest setup	DUT				
	DUT_P2 Passive ed				
	LP1_P1 LP2_P1				
	LP1 LP2				
	 DUT ports shall be connected to their LPs with opposite MASTER/SLAVE 				
	configuration.				
	 DUT port DUT_P1 test shall be connected to LP1. 				
	 LP1 including LP1_P1 shall be powered and the link between DUT_P1 and 				
	LP1_P1 shall be passive at the moment of starting the test execution.				
	 DUT port DUT_P2 test shall be connected to LP2. 				
	 LP1 including LP1_P2 shall be powered and the link between DUT_P1 and 				
	LP1_P1 shall be passive at the moment of starting the test execution.				
Test	1. Reset timer <i>t</i> ₀				
procedure	2. Trigger a wake-up request on LP1				
	3. Start timer t_0				
	4. Wait until the LP2 signalizes a wake-up condition				
	5. Readout timer value $(t_wkp_fwd = t_0)$				
Pass criteria	Each test iteration shall be classified as pass, if all of the following condition(s) are				
	fulfilled :				
	 t_wkp_fwd < TWU_Link_passive + TWU_Forwarding + TWU_Link_passive 				
	$t_wkp_fwd < 2ms + 1ms + 2ms$				
	<i>t_wkp_fwd</i> < 5 ms				

Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	The test shall be executed for each DUT 100BASE-T1 port
	Table 46: Main test structure of MAKE IOD 14

 Table 46: Main test structure of WAKE_IOP_14

Instance Test Case #	DUT / LP configuration	LP1 as SLAVE, LP2 as SLAVE	LP1 as MASTER, LP2 as MASTER	LP1 as MASTER, LP2 as SLAVE	LP1 as SLAVE, LP2 as MASTER
6.3.4.1	DUT_P1 as SLAVE, DUT_P2 as MASTER			WAKE_ IOP_14_SM_MS	
6.3.4.2	DUT_P1 as MASTER, DUT_P2 as SLAVE				WAKE_ IOP_14_MS_SM
6.3.4.3	DUT_P1 as MASTER, DUT_P2 as MASTER	WAKE_ IOP_14_MM _SS			
6.3.4.4	DUT_P1 as SLAVE, DUT_P2 as SLAVE		WAKE_ IOP_14_SS_MM		

Table 47: Test case instances of WAKE_IOP_14

6.3.5 Forwarding a wake-up request from passive to passive link, DUT in sleep *ID:* WAKE_IOP_15

Synopsis	Shall ensure that a wake-up request received by a DUT over a passive link can be			
Synopsis				
	forwarded within the expected time to a LP via a passive link.			
	Parameters to be measured:			
	• <i>t_wkp_fwd</i> : Time between triggering the WUR on LP1 and LP2 wake-up			
	signalization.			
Prerequisites	6. DUT shall have more than one port.			
	7. DUT with the capability to reset and configure its PHYs.			
	 BUT with the capability to set its PHYs into sleep mode. Link partner, or device that is connected to the DUT, shall be able to receive a 			
	wake-up pulse (WUP).			
	10. The test system shall be able of providing time measurement capabilities			
	synchronized with the test steps events.			
Test Setup	YUI DUT_P1 DUT_P2 Passive link			
	ssed			
	LP1_P1			
	LP1 LP2			
	 DUT ports shall be connected to their LPs with opposite MASTER/SLAVE configuration. DUT port <i>DUT_P1</i> test shall be connected to LP1. LP1 including LP1_P1 shall be powered and the link between DUT_P1 and 			
	 DUT port <i>DUT_P2</i> test shall be connected to LP2. 			
	 LP1 including LP1_P2 shall be powered and the link between DUT_P1 and LP1_P1 shall be passive at the moment of starting the test execution. 			
Test	6. Reset timer t_0			
procedure	7. Trigger a wake-up request on LP1			
	8. Start timer t_0			
	 Wait until the LP2 signalizes a wake-up condition Readout timer value (t wkp fwd = t₀) 			
Pass criteria	Each test iteration shall be classified as pass, if all of the following condition(s) are			
	fulfilled :			
	 t_wkp_fwd < TWU_Link_Passive + (T_Powersupply_Stable + T_PHY_Initialization) + TWU_Forwarding + TWU_Link_Passive 			
	$t_wkp_fwd < 2ms + (15ms) + 1ms + 2ms$			
	$t_w k p_f w d < 20 \text{ ms}$			

Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations
Notes	The test shall be executed for each DUT 100BASE-T1 port

Table 48: Main test structure of WAKE_IOP_15

Instance Test Case #	DUT / LP configuration	LP1 as SLAVE, LP2 as SLAVE	LP1 as MASTER, LP2 as MASTER	LP1 as MASTER, LP2 as SLAVE	LP1 as SLAVE, LP2 as MASTER
6.3.5.1	DUT_P1 as SLAVE, DUT_P2 as MASTER			WAKE_ IOP_15_SM_MS	
6.3.5.2	DUT_P1 as MASTER, DUT_P2 as SLAVE				WAKE_ IOP_15_MS_SM
6.3.5.3	DUT_P1 as MASTER, DUT_P2 as MASTER	WAKE_ IOP_15_MM_S S			
6.3.5.4	DUT_P1 as SLAVE, DUT_P2 as SLAVE		WAKE_ IOP_15_SS_MM		

Table 49: Test case instances of WAKE_IOP_15

6.4 Group 8, Sleep

ID: WAKE_IOP_16

Type: Requirement

The test cases defined in this section shall ensure that the PHY is able to make the transition to sleep as requested.

6.4.1 Sleep request after link-up ID: WAKE_IOP_17

Synopsis	Shall ensure that the DUT is able to enter the sleep mode and remain in this state after link-up was established when the sleep request is issued on the DUT side.		
Prerequisites	 DUT with the capability to reset and configure its PHYs. DUT with the capability to set its PHYs into sleep mode. The test system shall be able of providing time measurement capabilities synchronized with the test steps events. 		
Test Setup	 DUT DUT_P1 Active link LP1_P1 LP1 DUT shall be connected to an active link partner (LP1) with opposite MASTER/SLAVE configuration. A stable link-up condition shall be present at the moment of starting the test execution. 		
Test procedure	 Trigger a sleep request on the DUT Start timer t₀ Wait until the DUT signalizes a sleep condition Readout timer value (t_sleep = t₀) DUT and LP shall monitor whether the sleep condition remains for at least 750ms. 		
Pass criteria	 Each test iteration shall be classified as pass, if all of the following condition(s) are fulfilled : t_sleep < sleep_req_timer t_sleep < 16ms Both the DUT and the LP must not leave the sleep condition after the SLEEP state has been entered. 		
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations		
Notes	The test shall be executed for each DUT 100BASE-T1 port		

Table 50: Main test structure of WAKE_IOP_17

Instance Test Case #	DUT / LP configuration	LP as SLAVE	LP as MASTER
6.4.1.1	DUT as SLAVE		WAKE_IOP_17_S_M
6.4.1.2	DUT as MASTER	WAKE_ IOP_17_M_S	

Table 51: Test case instances of WAKE_IOP_17

6.4.2 Remote sleep request after link-up

ID: WAKE_IOP_18

Type: Requirement

Synopsis	Shall ensure that the DUT is able to enter the sleep mode and remain in this state after link-up was established when the sleep request is issued on the LP side.		
Prerequisites	 DUT with the capability to reset and configure its PHYs. DUT with the capability to set its PHYs into sleep mode. The test system shall be able of providing time measurement capabilities synchronized with the test steps events. 		
Test Setup	DUT_P1 Active link LP1_P1 LP1		
	 DUT shall be connected to an active link partner (LP1) with opposite MASTER/SLAVE configuration. A stable link-up condition shall be present at the moment of starting the test execution. 		
Test procedure	 Trigger a sleep request on the LP1 Start timer t₀ Wait until the DUT signalizes a sleep condition Readout timer value (t_sleep = t₀) DUT and LP shall monitor whether the sleep condition remains for at least 750ms. 		
Pass criteria	 Each test iteration shall be classified as pass, if all of the following condition(s) are fulfilled : t_sleep < sleep_req_timer + sleep_ack_timer t_sleep < 16ms + 8ms 		
	 <i>t_sleep</i> < 24ms Both the DUT and the LP must not leave the sleep condition after the SLEEP state has been entered. 		
Test iterations	See suggested test iterations in Appendix - 7.1 Suggested Iterations		
Notes	The test shall be executed for each DUT 100BASE-T1 port		

Table 52: Main test structure of WAKE_IOP_18

Instance Test Case #	DUT / LP configuration	LP as SLAVE	LP as MASTER
6.4.2.1	DUT as SLAVE		WAKE_IOP_18_S_M
6.4.2.2	DUT as MASTER	WAKE_IOP_18_M_S	

Table 53: Test case instances of WAKE_IOP_18

7 Appendix

7.1 Suggested Iterations

7.1.1 Nomenclature

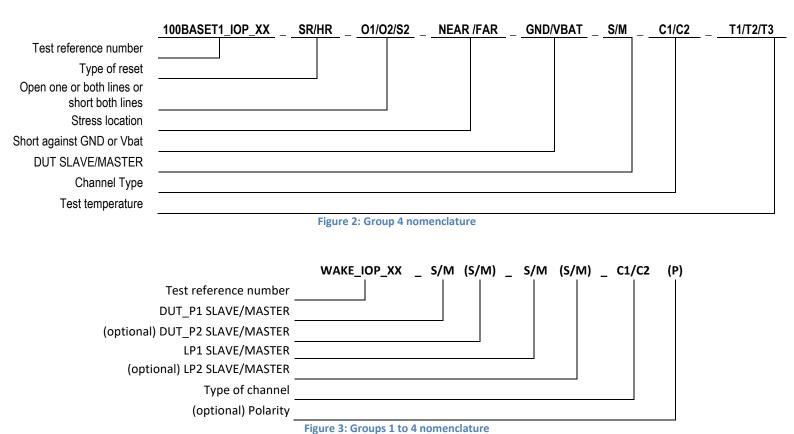
The following parameters are to describe the test environment and if apply the kind of stress and its location.

Reference name	Description
100BASET1_IOP_XX	Test reference
SR	Soft Reset
HR	Hard Reset
01	Open is on ETH_N or ETH_P
02	Open on both ETH_N and ETH_P
NEAR	Open/Short near to DUT
FAR	Open/Short near to LP
М	MASTER
S	SLAVE
Р	Swapped Polarity
	Channel Type 3 or
C1	combinations of Type 3 and
	Type 2 channels
C2	Channel Type 1
T1	Room Temperature
T2	-40°C
Т3	105°C /125°C

Table 54: Nomenclature of test enviroment variables

	100BASET1_IOP_XX	_ SR/HR	S/M	M/S	_ P .	_ C1/C2 _	
Test reference number							
Type of reset							
DUT SLAVE/MASTER							
LP SLAVE/MASTER							
Swapped Polarity							
Channel Type							
Test temperature							

Figure 1: Groups 1 to 3 nomenclature



Group	Test Case	Minimal amount of iterations per LP*
	IOP_16_SR_M_S_C1_T1	500.000
	IOP_16_SR_M_S_C2_T1	500.000
	IOP_16_SR_S_M_C1_T1	500.000
	IOP_16_SR_S_M_P_C1_T1	8.000
Group 1:	IOP_16_SR_S_M_C2_T1	500.000
	IOP_16_SR_S_M_P_C2_T1	18.000
Link Status	IOP_17_SR_M_M_C2_T1	50.000
Link Status	IOP_17_SR_S_S_C2_T1	50.000
	IOP_18_SR_M_S_P_C2_T1	6.250
	IOP_18_SR_S_M_P_C2_T1	6.250
	IOP_19_SR_M_S_C2_T1	125.000
	IOP_19_SR_S_M_C2_T1	125.000

7.1.2 Group 1 test cases iterations

Table 55: Group 1 test cases suggested iterations

*When considering multiple link partners tests.

7.1.3 Group 2 test cases iterations

		D. Charling all
		Minimal
Group	Test Case	amount of
		iterations per LP*
	IOP_21_HR_M_S_C1_T1	200
	IOP_21_HR_M_S_C1_T2	25
	IOP_21_HR_M_S_C1_T3	25
	IOP_21_HR_M_S_C2_T1	1.800
	IOP_21_HR_M_S_C2_T2	225
	IOP_21_HR_M_S_C2_T3	225
	IOP_21_HR_S_M_C1_T1	200
	IOP_21_HR_S_M_C1_T2	25
	IOP_21_HR_S_M_C1_T3	25
	IOP_21_HR_S_M_C2_T1	1.800
	IOP_21_HR_S_M_C2_T2	225
	IOP_21_HR_S_M_C2_T3	225
	IOP_21_HR_S_M_P_C1_T1	200
	IOP_21_HR_S_M_P_C1_T2	25
	IOP 21 HR S M P C1 T3	25
	IOP 21 HR S M P C2 T1	1.800
	IOP_21_HR_S_M_P_C2_T2	225
	IOP 21 HR S M P C2 T3	225
	IOP 21 SR M S C1 T1	250.000
	IOP 21 SR M S C1 T2	25.000
Group 2:	IOP_21_SR_M_S_C1_T2	25.000
	IOP_21_SR_M_S_C2_T1	500.000
Link-Up		
		25.000
	IOP_21_SR_M_S_C2_T3	25.000
	IOP_21_SR_S_M_C1_T1	250.000
	IOP_21_SR_S_M_C1_T2	24.750
	IOP_21_SR_S_M_C1_T3	24.750
	IOP_21_SR_S_M_C2_T1	500.000
	IOP_21_SR_S_M_C2_T2	25.000
	IOP_21_SR_S_M_C2_T3	25.000
	IOP_21_SR_S_M_P_C1_T1	8.000
	IOP_21_SR_S_M_P_C1_T2	250
	IOP_21_SR_S_M_P_C1_T3	250
	IOP_21_SR_S_M_P_C2_T1	72.000
	IOP_21_SR_S_M_P_C2_T2	2.250
	IOP_21_SR_S_M_P_C2_T3	2.250
	IOP_22_HR_M_S_C1_T1	800
	IOP_22_HR_M_S_C1_T2	25
	IOP_22_HR_M_S_C1_T3	25
	IOP_22_HR_M_S_C2_T1	7.200
	IOP_22_HR_M_S_C2_T2	225
	IOP_22_HR_M_S_C2_T3	225
		225

Group	Test Case	Minimal amount of iterations per LP*
	IOP_22_HR_S_M_C1_T1	800
	IOP_22_HR_S_M_C1_T2	25
	IOP_22_HR_S_M_C1_T3	25
	IOP_22_HR_S_M_C2_T1	7.200
	IOP_22_HR_S_M_C2_T2	225
	IOP_22_HR_S_M_C2_T3	225
	IOP_22_HR_S_M_P_C1_T1	800
	IOP_22_HR_S_M_P_C1_T2	25
	IOP_22_HR_S_M_P_C1_T3	25
	IOP_22_HR_S_M_P_C2_T1	7.200
	IOP_22_HR_S_M_P_C2_T2	225
	IOP_22_HR_S_M_P_C2_T3	225
	IOP_22_SR_M_S_C1_T1	20.000
	IOP_22_SR_M_S_C1_T2	625
	IOP_22_SR_M_S_C1_T3	625
	IOP_22_SR_M_S_C2_T1	180.000
	IOP_22_SR_M_S_C2_T2	5.625
	IOP_22_SR_M_S_C2_T3	5.625
	IOP_22_SR_S_M_C1_T1	20.000
	IOP_22_SR_S_M_C1_T2	625
	IOP_22_SR_S_M_C1_T3	625
	IOP_22_SR_S_M_C2_T1	180.000
	IOP_22_SR_S_M_C2_T2	5.625
	IOP_22_SR_S_M_C2_T3	5.625
	IOP_22_SR_S_M_P_C1_T1	4.000
	IOP_22_SR_S_M_P_C1_T2	125
	IOP_22_SR_S_M_P_C1_T3	125
	IOP_22_SR_S_M_P_C2_T1	36.000
	IOP_22_SR_S_M_P_C2_T2	1.125
	IOP_22_SR_S_M_P_C2_T3	1.125

Table 56: Group 2 test cases suggested iterations

*When considering multiple link partners tests.

7.1.4 Group 3 test cases iterations

Group	Test Case	Suggested amount of iterations	Minimal amount of iterations per LP*
Group 3:	IOP_24a_SR_M_S_C1_T1	1	n.a.
	IOP_24a_SR_S_M_C1_T1	1	n.a.
Signal	IOP_24b_SR_M_S_C1_T1	1	n.a.
Quality	IOP_24b_SR_S_M_C1_T1	1	n.a.

Table 57: Group 3 test cases suggested iterations

*When considering multiple link partners tests.

7.1.5 Group 4 test cases iterations

Group	Test Case	Suggested amount of iterations	Minimal amount of iterations per LP*
	IOP_31_SR_C1_T1**	50	50
	IOP_31_SR_C2_T1**	450	450
	IOP_32_SR_O1_FAR_M_C2_T1	500	n.a.
	IOP_32_SR_O1_FAR_S_C2_T1	500	n.a.
	IOP_32_SR_O1_NEAR_M_C2_T1	500	n.a.
	IOP_32_SR_O1_NEAR_S_C2_T1	500	n.a.
	IOP_32_SR_O2_FAR_M_C2_T1	500	n.a.
	IOP_32_SR_O2_FAR_S_C2_T1	500	n.a.
	IOP_32_SR_O2_NEAR_M_C2_T1	500	n.a.
Group 4:	IOP_32_SR_O2_NEAR_S_C2_T1	500	n.a.
	IOP_33_SR_S2_FAR_M_C2_T1	500	n.a.
Cable	IOP_33_SR_S2_FAR_S_C2_T1	500	n.a.
Diagnostics	IOP_33_SR_S2_NEAR_M_C2_T1	500	n.a.
	IOP_33_SR_S2_NEAR_S_C2_T1	500	n.a.
	IOP_33_SR_S2_FAR_GND_M_C2_T1	500	n.a.
	IOP_33_SR_S2_FAR_GND_S_C2_T1	500	n.a.
	IOP_33_SR_S2_NEAR_GND_M_C2_T1	500	n.a.
	IOP_33_SR_S2_NEAR_GND_S_C2_T1	500	n.a.
	IOP_33_SR_S2_FAR_VBAT_M_C2_T1	500	n.a.
	IOP_33_SR_S2_FAR_VBAT_S_C2_T1	500	n.a.
	IOP_33_SR_S2_NEAR_VBAT_M_C2_T1	500	n.a.
	IOP_33_SR_S2_NEAR_VBAT_S_C2_T1	500	n.a.

Table 58: Group 4 test cases suggested iterations

*When considering multiple link partners tests.

**Only Diagnostic test case (IOP 31)

7.1.6 Group 5 test cases iterations

Group	Test Case	Suggested amount of iterations
	WAKE_IOP_3_S_M_C1	2500
	WAKE_IOP_3_M_S_C1	2500
	WAKE_IOP_3_S_M_C2	2500
	WAKE_IOP_3_M_S_C2	2500
	WAKE_IOP_3_S_M_C1_P	5000
Group 5:	WAKE_IOP_4_S_M_C1	5000
	WAKE_IOP_4_M_S_C1	5000
Wake-up	WAKE_IOP_5_S_M_C1	2500
reception and	WAKE_IOP_5_M_S_C1	2500
signalizing	WAKE_IOP_5_S_M_C2	2500
	WAKE_IOP_5_M_S_C2	2500
	WAKE_IOP_7_M_S_C1	2500
	WAKE_IOP_7_S_M_C1	2500
	WAKE_IOP_7_M_S_C2	2500
	WAKE_IOP_7_S_M_C2	2500
	WAKE_IOP_7_M_S_C1_P	5000

Table 59: Group 1 test cases suggested iterations

7.1.7 Group 6 test cases iterations

Group	Test Case	Suggested amount of iterations
Group 6:	WAKE_IOP_8_S_M_C1	2500
	WAKE_IOP_8_M_S_C1	2500
	WAKE_IOP_8_S_M_C2	2500
Wake-up transmission	WAKE_IOP_8_M_S_C2	2500
	WAKE_IOP_9_S_M_C1	5000
	WAKE_IOP_9_M_S_C1	5000

Table 60: Group 2 test cases suggested iterations

7.1.8 Group 7 test cases iterations

Group	Test Case	Suggested amount of iterations
	WAKE_IOP_11_MM_SS_C1	5000
	WAKE_IOP_11_SS_MM_C1	5000
	WAKE_IOP_11_MS_SM_C1	5000
	WAKE_IOP_11_SM_MS_C1	5000
	WAKE_IOP_12_MM_SS_C1	5000
	WAKE_IOP_12_SS_MM_C1	5000
	WAKE_IOP_12_MS_SM_C1	5000
Group 7:	WAKE_IOP_12_SM_MS_C1	5000
	WAKE_IOP_13_MM_SS_C1	5000
	WAKE_IOP_13_SS_MM_C1	5000
Wake-up forwarding	WAKE_IOP_13_MS_SM_C1	5000
	WAKE_IOP_13_SM_MS_C1	5000
	WAKE_IOP_14_MM_SS_C1	5000
	WAKE_IOP_14_SS_MM_C1	5000
	WAKE_IOP_14_MS_SM_C1	5000
	WAKE_IOP_14_SM_MS_C1	5000
	WAKE_IOP_15_MM_SS_C1	5000
	WAKE_IOP_15_SS_MM_C1	5000
	WAKE_IOP_15_MS_SM_C1	5000
	WAKE_IOP_15_SM_MS_C1	5000

Table 61: Group 3 test cases suggested iterations

7.1.9 Group 8 test cases iterations

Group	Test Case	Suggested amount of iterations
Group 8:	WAKE_IOP_17_S_M_C1	5000
	WAKE_IOP_17_M_S_C1	5000
Sleep	WAKE_IOP_18_S_M_C1	5000
	WAKE_IOP_18_M_S_C1	5000

Table 62: Group 4 test cases suggested iterations

7.2 Artificial degradation of channel quality

7.2.1 Description

Figure 4 shows an example approach to artificially reduce the quality of the communication channel with a differential directional coupler whose parameters are defined in Table 63.

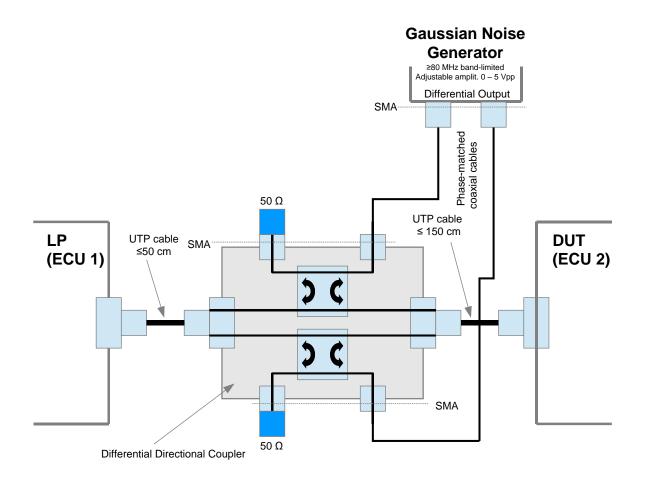


Figure 4: Example for artificial degradation of channel quality

Differential Directional Coupler			
Parameter	Value	Frequency	
Insertion Loss	≤ 1 dB	1 – 66 MHz	
Return Loss	18 dB 18 – 10 x log 10(f/20)	1 MHz ≤ f ≤ 20 MHz 20 MHz ≤ f ≤ 66 MHz	
Coupling Flatness	± 1 dB	1 – 66 MHz	
Coupling Attenuation Forward	20 dB ± 1 dB		
Coupling Attenuation Backward	21 dB ± 1 dB		

Table 63: Example for Differential Directional Coupler Parameters

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