10BASE-T1S PLCA Conformance Test Suite Specification

PLCA Conformance Test Suite Specification

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VERSION AND RESTRICTION HISTORY OF THIS DOCUMENT

VERSION	DESCRIPTION	RESTRICTION LEVEL	DATE
0.1	Initial version	OPEN Members Only	
0.2	Implemented Feedback from April 4, 2023		April 20, 2023
0.3	Implemented Feedback from CanovaTech discussed on May 11, 2023		May 11, 2023
0.4	Following the consensus achieved in the ballot held at the TC14 main regular call on June 20, 2023, the PLCA Recovery section has been defined as informative and the respective pass criteria were updated accordingly		June 22, 2023
0.5	Last editorial feedback from Canovatech and Onsemi of typos and copy/paste errors were corrected		August 28, 2023
1.0	Public	Public	November 8, 2023
1.1	Update considering early testing experience	OPEN Members Only	February 5, 2025
1.2	Update includes minor corrections to the equations in Groups T2 & T3 as per the latest feedback from Microchip.		March 10, 2025
1.2a	Update includes editorial changes as per the latest feedback from OnSemi.		March 11, 2025
1.3	Transferred into new OPEN Template and creation of final version	Public	June 16, 2025

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1 INTRODUCTION

This suite of tests has been developed to help implementers evaluate the functionality of the PLCA reconciliation sublayer of their 10BASE-T1S device.

These tests are designed to determine if a product conforms to specifications defined in IEEE802.3cg Clause 148. Successful completion of all tests contained in this suite does not guarantee that the tested device will operate with other devices. However, combined with satisfactory operation when tested in accordance with the OPEN Alliance 10BASE-T1S Interoperability Test Suite, these tests provide a reasonable level of confidence that the Device Under Test (DUT) will function properly in many 10BASE-T1S automotive environments.

2 NORMATIVE REFERENCES

The following documents are referred to in the text in such a way that some or all their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

[1] IEEE P802.3cg: Physical Layer Specifications and Management Parameters for 10 Mb/s Operation and Associated Power Delivery over a Single Balanced Pair of Conductors

[2] OPEN ALLIANCE: 10BASE-T1S Physical Media Attachment Test Suite – Revision 1.2 (draft)

[3] OPEN ALLIANCE: 10BASE-T1S Physical Coding Sublayer Test Suite – Revision 0.3 (draft)

[4] OPEN ALLIANCE: Channel and Components Requirements for 10BASE-T1S Link Segment – Revision 0.2 (draft)

[5] OPEN ALLIANCE: IEEE 10BASE-T1S System Implementation Specification – Revision 1.0

[6] OPEN ALLIANCE: 10BASE-T1S PLCA Management Registers – Revision 1.2

[7] ISO/IEC 9646 — Information technology — Open Systems Interconnection — Conformance testing methodology and framework

[8] OPEN ALLIANCE: 10BASE-T1x MAC-PHY Serial Interface – Revision 1.1

3 TERMS AND DEFINITIONS

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- ISO Online browsing platform: available at https://www.iso.org/obp
- IEC Electropedia: available at http://www.electropedia.org/

3.1 Node term definition

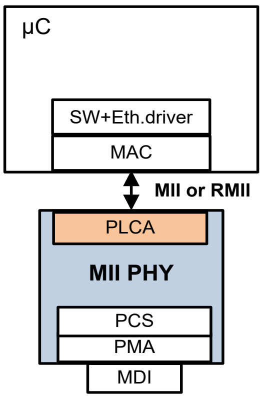
End Node	A node that is at either end of a mixing segment. There are no other nodes between the End Node and the 100Ω edge termination. The End Node may contain the 100Ω edge termination.
Drop Node	Any node that is located between the two end nodes
Coordinator	This is the node configured as aPLCALocalNodeID=0 that is responsible for the periodic transmission of the BEACON and configuring the number of transmit opportunities between each BEACON.
Follower	Followers are any nodes configured as aPLCALocalNodeID=1..254. They synchronize their transmit opportunity counter with the reception of the periodic BEACON transmitted by the coordinator
Head Node	This is the highest-level application node on the mixing segment. It typically implements a switch or gateway access to the core network beyond the bus segment.

Note: It is expected that each network segment includes one Coordinator Node, one Head Node, and two End Nodes. The Coordinator and Head Node functions may be implemented in any physical node (including End Nodes) and may be combined into a single physical node or separate physical nodes.

3.2 PLCA location within different 10BASE-T1S PHYs implementations

Following table describes an overview of the different possible 10BASE-T1S PHYs implementations that are covered by this test specification.

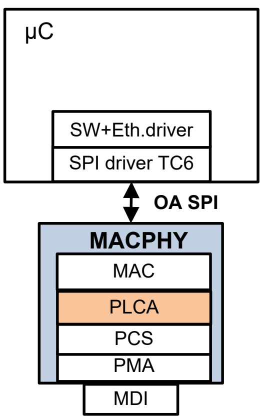
PHY with MII



PLCA integrated in PHY: transparent for every uC

Compatible with every MAC controller supporting Half-duplex

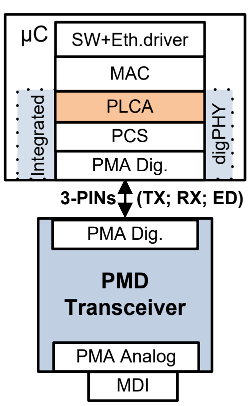
PHY with SPI (MACPHY)



Low-cost ECU without MAC and smaller interface

Requires Ethernet frame processing over SPI interface as defined in [8].

DigPHY/PMD Transceiver



The 10BASE-T1S PMD Transceiver is a simple and cost effective solution with 3-pin clock-less interface between the host controller and the PMD transceiver chip suited for embedded systems where the digital portion of the PHY is fully integrated into an MCU, an Ethernet switch core, or any other suitable host where only the analog portion is left into a separate chip (i.e., the PMD transceiver).

4 ABBREVIATION/SYMBOLS

Abbreviation	Glossary term	Glossary definition
dPLCA	Dynamic Physical Layer Collision Avoidance	It is an optional PLCA Node ID allocation method. This should allow all node IDs (including node 0) to be assigned dynamically and to change during operation. The coordinator node shall also be able to vary the node count depending on how many active nodes are detected. dPLCA is fully backward compatible to the normal PLCA defined in 802.3cg, so that dPLCA enabled nodes can join a network with normal PLCA nodes without disturbing the operation.
DUT	Device under test	Combination of uC, PHY/Switch component, PHY/Switch configuration and filter that is being tested.
IUT	Implementation under test	The PHYs entirely in a network environment are considered as the IUT
MAC	Media Access Control	Abbreviation for the sub layer of the data link layer (layer 2) of the OSI model or for the physical device that implements the Media Access Control functions.
MDI	Media dependent interface	
MII	Medium Independent Interface	
P2P	Point-to-point	
PCS	Physical Coding Sublayer	
PHY	Interface semiconductor circuit for implementation of the functions of the Ethernet physical layer	Abbreviation for the physical layer (layer 1) of the OSI model or for the device that implements layer 1 of the OSI model.
PLCA	Physical Layer Collision Avoidance	A method for generating transmit opportunities for 10BASE-T1S operating on mixing segments. (See[1], Clause 148.)
PMA	Physical Medium Attachment	
SPI	Serial Peripheral Interface	
TO	Transmit opportunity	Each node on the network get assigned at least one transmit opportunity in each transmission cycle.
n.a.	Not applicable	-

Table 1: List of Abbreviations.

5 GLOSSARY TERMS

Glossary term	Glossary definition
MAY	This word or the adjective "OPTIONAL", means that an item is truly optional. One vendor may choose to include the item because a particular marketplace requires it or because the vendor feels that it enhances the product while another vendor may omit the same item. An implementation which does not include a particular option MUST be prepared to interoperate with another implementation which does include the option, though perhaps with reduced functionality. In the same way an implementation which does include a particular option MUST be prepared to interoperate with another implementation which does not include the option (except, of course, for the feature the option provides.)
MUST	This word, or the terms "REQUIRED" or "SHALL", means that the definition is an absolute requirement of the specification.
MUST NOT	This phrase or the phrase "SHALL NOT", means that the definition is an absolute prohibition of the specification.
SHOULD	This word, or the adjective "RECOMMENDED", means that there may exist valid reasons in particular circumstances to ignore a particular item, but the full implications must be understood and carefully weighed before choosing a different course.
SHOULD NOT	This phrase, or the phrase "NOT RECOMMENDED" means that there may exist valid reasons in particular circumstances when the particular behavior is acceptable or even useful, but the full implications should be understood, and the case carefully weighed before implementing any behavior described with this label.
External PHY filter or external filter.	An additional circuit that is connected directly to the PHY and filters the in- and outgoing physical layer signaling. The PHY vendor typically provides a reference filter design.
PHY configuration	Variable settings that affect the PHY's behavior (e.g., sensitivity of internal equalizers, or shaping of outgoing physical layer signaling). The PHY configuration could be set by an upper layer (e.g., by software) or could be hardcoded, e.g., via dedicated PHY configuration pins.
Test case	Description of one or more test steps and a set of conditions that define whether the observed behavior when executing the test steps matches the expected results.
Test iteration	The execution of all test steps of a given test case.
Test instance	A test instance defines different test parameters for a given test case, such as the DUT's PHY Coordinator/Follower configuration, or used cable to connect the link partner. The test case itself is not altered.
Channel	Synonym for physical layer communication channel (cf. [4]).

Table 2: List of Definitions.

6 ORGANIZATION OF TESTS

In this chapter the main structure of the test cases as well as the elementary test case structure will be introduced.

6.1 Elementary test structure

The main structure description of a test case is shown in Table 3. A brief description of the meaning of each field is provided.

Purpose	A short description of the purpose of the test case is given here.
Reference	
Prerequisites	A list of requirements and capabilities needed for proper test conduction
DUT set-up	The respective test environment setup is specified (e. g. if different test case sequences will require different test system configuration)
Test description	The first note here describes the total sum of test case executions due to setup variations to give the test implementer a first impression of the specific test case. As the second part of the test case execution, the test steps are described dealing with the setup being applied and what is observed and measured at each execution etc. All actions of the test environment shall be described explicitly in this item.
Pass criteria	In this response cell, a description is given about what is expected as the result. Pass criteria are also specified in this point.
Test iterations	Amount of test repetitions.
Notes	When necessary, a note will be added complementing the information of the test case.

Table 3 - Main test structure

6.2 Test case instance structure

Together with the test definition and all its parameters, the test case instances that are part of each test case will also be defined. A test case instance can be defined as a repetition of the same test case modifying certain configurations of the DUT and the test environment without losing focus on the test purpose.

Instance Test Case #	Description	Parameter	Condition
AX.XX	Description of the test cases belonging to this subgroup	α	conditions under which the variables are applied either in different configurations or stress conditions.
AX.XX		β	

Table 4 - Test case instance definition

6.3 DUT requirements

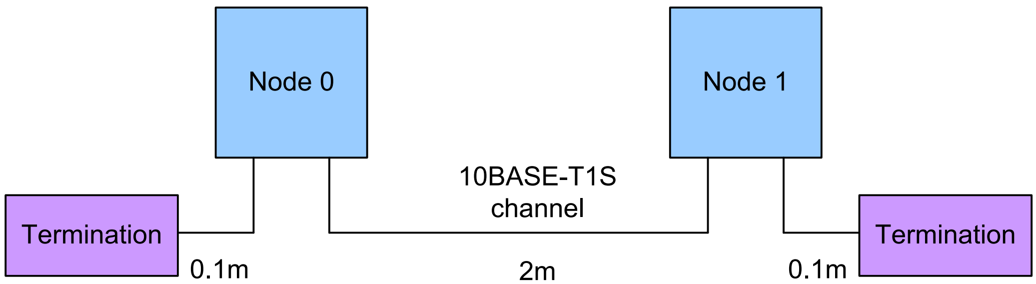
For the purposes of this test suite, it is assumed that the DUT can manipulate PLCA-related signals and ID numbers via registers. In addition, at least one or more nodes are required for PLCA testing. This node must be able to set the ID to any number from 0, 255, 1-254.

7 PLCA CONFORMANCE TEST DEFINITIONS

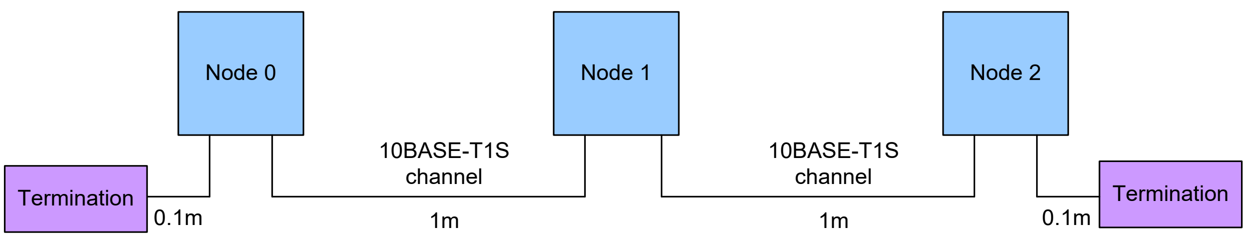
7.1 Channels definition

This definition shall be used for defining a test wiring harness that simulates various communication channels according to the channel definitions of IEEE Std. 802.3cg, [4] and [5].

7.1.1 Channel type 1 (2 node mixing segment) [H1]



7.1.2 Channel type 2 (3 node mixing segment) [H2]



7.2 PLCA configuration

PLCA parameters not mentioned here shall be set to “default” according to [6] and [1]. dPLCA is outside the scope of this document.

7.2.1 PLCA configuration in 2 nodes in the mixing segment [H1]

The nodes are numbered from 0 to 1. Node 0 is configured to be the coordinator. The maximum slot number (TO) is 1, so that the beacon follows immediately after the message send from node 1.

The amount of data per message and the data itself that is to be sent in each message is defined in the section 7.3.

PLCA slot	0	1	0
Node	0	1	0
Burst	1	1	

Figure 7-1: PLCA cycle in 2 nodes mixing segment [H1]

7.2.2 PLCA configuration in 3 nodes in the mixing segment [H2]

The nodes are numbered from 0 to 2. Node 0 is configured to be the coordinator. The maximum slot number (TO) is 2, so that the beacon follows immediately after the message sent from node 2.

The amount of data per message and the data itself that is to be sent in each message is defined in the section 7.3.

PLCA slot	0	1	2
Node	0	1	2
Burst	1	1	1

Figure 7-2: PLCA cycle in 3 nodes mixing segment [H2]

7.3 Message transfer

When messages are sent, PLCA is active on all nodes.

M1: all frames have **maximum length** (1500 bytes in the data field)

- M1A: all nodes in the mixing segment transmit messages
- M1B: only the DUT as Coordinator transmits messages
- M1C: only the DUT as Follower transmit messages

M2: No data is sent, so all TO slots are empty, i.e. without transmission.

M3: Only the Coordinator node sends BEACON and data in TO#0

The addresses in a frame shall be:

- Destination address DA = Broadcast, so all nodes can check counters and report an error (within their frames)
- Source address SA = Unique in each node

Each node shall maintain and transmit the following parameters:

CycleCounter (CC) (16 bit) increases when the message sent by the Coordinator has been received; this message can be identified by the source address (SA).

SequenceNumber (SC) (8 bit), recent number of messages in a burst. The sequence number indicates the last received frame of a burst. The node sending the burst increments the sequence number by 1 after each successfully sent frame until the maximum number of burst frames for the node is reached.

MessageCounter (MC) (32 bit), increases, with each message sent by this node

StatusInformation (SI) (16 bit), to be defined:

- state of health (PLCA Status, SQI if supported, local/remote jabber indication),
- information to synchronize stress conditions applied alternating and cyclically in a decentralized manner like for example loss of power or variable terminations.
- dedicated Request commands (for example, node 0 can request other nodes to reset counters or to stop communication and enter low power mode).

aPLCALocalNodeID (PLCA ID) (8 bit), static value

(10 bytes data field up to here, remaining 1490 bytes for padding)

Data field layout: [CC, SC, MC, SI, PLCA ID, Padding]

Padding pattern in M1 (fixed length 1490 bytes):

[0xFF, 0xFE, ...0x01, 0x00]	256 bytes, decreasing
64 x [0x00]	64 bytes constant 0x00
[0x00, 0x01, ... 0xFE, 0xFF]	256 bytes, increasing
64x [0xFF]	64 bytes constant 0xFF
[0x0F, 0x0E, ...0xF1, 0xF0]	256 bytes, decreasing, XORed with 0xF0
64x [0xAA]	64 bytes constant 0xAA
[0xF0, 0xF1, ... 0x0E, 0x0F]	256 bytes, increasing, XORed with 0xF0
64x [0x5A]	64 bytes constant 0x5A

Followed by

210 x [0x3C]   210 bytes constant 0x3C

7.4 Power conditions

7.4.1 Nominal Battery Voltage

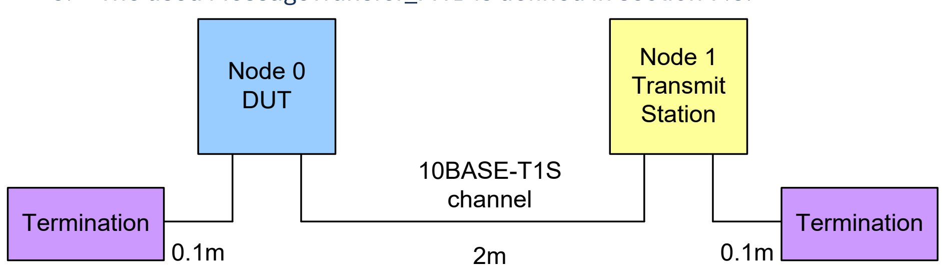
Unless differently indicated the nominal battery voltage used in this specification is 14V ± 0.1V.

8 GROUP 1 – PLCA TEST CASES

8.1 [T] PLCA Timing requirements

The test cases defined in this section shall ensure that the PLCA is able to communicate within the required timing parameters.

8.1.1 Group T1 – Coordinator node

Purpose	The purpose of this test is to verify important timing parameters for interoperability of nodes in PLCA mode. Under any circumstance, a packet sent by a node during its own TO shall be received by any other node within the corresponding TO boundaries.
Reference	[1], Table 147-6 10BASE-T1S delay constraints
Prerequisites	1. DUT with the capability to reset and configure its PHY. 2. DUT shall be able to be configured either as Coordinator node or as Follower node. 3. DUT must be able to indicate PLCA status via its status registers. 4. DUT must be able to send frames in the respective transmit opportunity.
DUT set-up	1. This test case is conducted with H1 topology (P2P link segment) 2. This test case is conducted with nodes in a mixing-segment multi drop. • aPLCANodeCount = 2 • aPLCATransmitOpportunityTimer = 32 3. DUT should be configured as Coordinator node with aPLCALocalNodeID = 0. 4. DUT shall be ready to transmit before BEACON. 5. The used MessageTransfer_M1B is defined in section 7.3.  *Figure 8-1: Topology for test group T1*
Test description	1. Once the configuration in all nodes is completed, enable the PLCA reconciliation sublayer functionality at Follower Node and subsequently at the coordinator node (Node #0) to start communication. 2. Test should wait for PLCA on all nodes to be activated before continuing with next step. 3. Initiate data transmission following the respective PLCA Cycle and Message transfer configurations. 4. Measure the time between BEACON expiration and node's transmission with an oscilloscope (oscilloscope probe is connected at MDI of the coordinator DUT), as shown as $t_{measure}$ in the figure below:

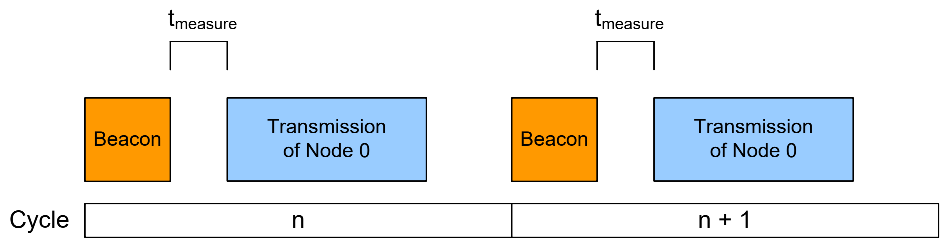
	 *Figure 8-2: Time between BEACON expiration and node's transmission – Coordinator node*
Pass criteria	The measured interval shall be between following values: • Min = ($CRS\_deasserted_{min}$) + ($t_{PLCAresp\_min}$[1]) + (TX_EN to MDI_{min}) + ($MII\_propagation\_time_{min}$[2]) = **1060 ns** • Max = ($CRS\_deasserted_{max}$) + ($t_{PLCAresp\_max}$) + (TX_EN to MDI_{max}) + ($MII\_propagation\_time_{max}$) = **2360 ns**
Test iterations	Amount of test repetitions: n.a.
Notes	In this scenario the BEACON and subsequent data are sent by the coordinator, therefore neither skew (same CRS fall time) nor the prop delay of the Tx_line (same node) are applicable in the calculation.

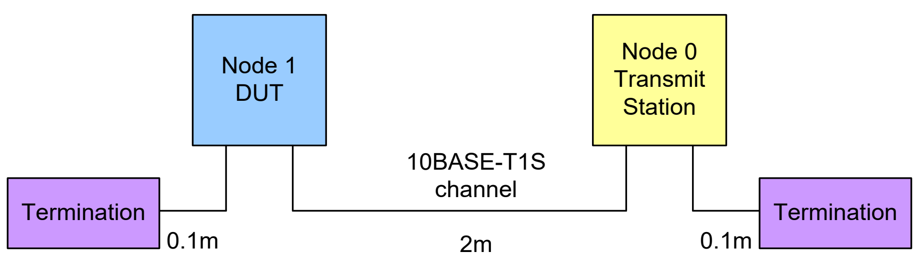
Table 5: Main test structure of Group T1

Instance Test Case #	Description	Parameter	Condition
T1.1	Normal communication undisturbed	n.a.	n.a.

Table 6 - Test case instances definition for Group T1 - Tests case T1.1

[1] This is the PLCA RS response time. This is the time that it takes for the PLCA state machines to perform an action and transition to new states following the de-assertion of carrier sense. This time is not zero, it is assumed to be minimum = 300 ns and maximum 800ns (the wake/sleep specification added a couple states to the PLCA Control state diagram which requires extra time) and must be accounted for.
[2] From the IEEE formalism point of view, there is a propagation time for the MII of 2 clock cycles (max. 800ns), however this is only applicable for external PLCA implementations, implementing PLCA external to the PHY makes no sense, it is assumed 0 ns for an internal PLCA/PHY implementation.

8.1.2 Group T2 – Follower node BEACON

Purpose	The purpose of this test is to verify important timing parameters for interoperability of nodes in PLCA mode. Under any circumstance, a packet sent by a node during its own TO shall be received by any other node within the corresponding TO boundaries.
Reference	[1], Table 147-6 10BASE-T1S delay constraints
Prerequisites	1. DUT with the capability to reset and configure its PHY. 2. DUT shall be able to be configured either as Coordinator node or as Follower node. 3. DUT must be able to indicate PLCA status via its status registers. 4. DUT must be able to send frames in the respective transmit opportunity.
DUT set-up	1. This test case is conducted with H1 topology (P2P link segment) 2. This test case is conducted with either nodes mixing-segment multi drop topology or with an arbitrary waveform generator capable to emulate a BEACON pattern (Node#3). • aPLCANodeCount = 2 • aPLCATransmitOpportunityTimer = 32 3. DUT should be configured as Follower node with aPLCALocalNodeID = 1. 4. DUT shall be ready to transmit before BEACON. 5. The used *MessageTransfer_M1C* is defined in section 7.3. 6. To avoid having the test being affected by the MAC inter-packet gap, allow at least 10us of line idle (no transmissions) before starting the test. 7. Expiration of TO timer needs to be considered.  *Figure 8-3: Topology for test group T2*
Test description	1. Once the configuration in all nodes is completed, enable the PLCA reconciliation sublayer functionality at Follower Node and subsequently at the coordinator node (Node #0) to start communication. 2. Test should wait for PLCA on all nodes to be activated before continuing with next step. 3. Initiate data transmission with the respective PLCA Cycle and Message transfer. 4. Measure the time between BEACON expiration and node's transmission with an oscilloscope (oscilloscope probe is connected at the MDI of the follower DUT), as shown as $t_{measure}$ in the figure below:

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<tr>
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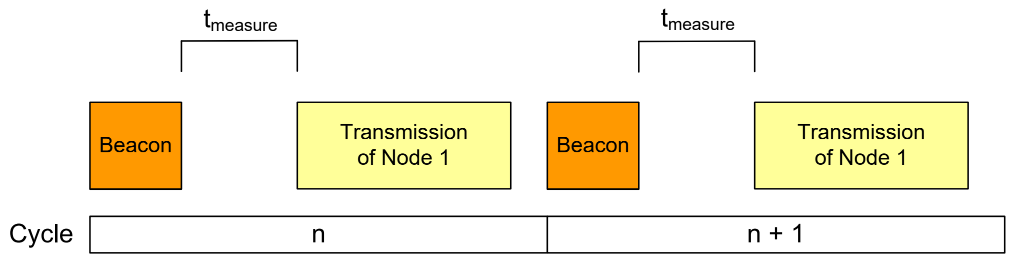
<td>


Figure 8-4: Time between BEACON expiration and node's transmission – Follower node (aPLCALocalNodeID = 1)
</td>
</tr>
<tr>
<td>Pass criteria</td>
<td>
The test case shall be considered as passed if all the following conditions are fulfilled:
The measured interval shall be between the following values:

Time = Tcf + $t_{PLCAresp}$ + Ttx + MII delay + (TO_timer x 100ns x Node_ID)

– min Tcf = 640ns
– max Tcf = 1120ns
– Tpd =If the oscilloscope probe is connected at the follower DUT, then there is no need to account for the propagation delay = 0ns
– min $t_{PLCAresp}$ = 300ns
– max $t_{PLCAresp}$ = 800ns[3]
– min Ttx = 120ns
– max Ttx = 440ns
– MII delay = 0ns, it is assumed 0 ns for an internal PLCA/PHY implementation.

• Min = min Tcf + min $t_{PLCAresp}$ + min Ttx + MII delay + (TO_timer x 100ns x Node_ID) =
= 640ns + 300ns + 120ns + 0ns + (TO_timer x100ns x Node_ID) =
= 1060 ns + (TO_timer x 100ns x Node_ID)

• Max = max Tcf + max $t_{PLCAresp}$ + max Ttx + MII delay + (TO_timer x 100ns x Node_ID) =
= 1120ns + 800ns + 440ns + 0ns + (TO_timer x 100ns x Node_ID) =
= 2360 ns + (TO_timer x 100ns x Node_ID)
</td>
</tr>
<tr>
<td>Test iterations</td>
<td>Amount of test repetitions: 10</td>
</tr>
</table>

[3] The wake/sleep specification added a couple states to the PLCA Control state diagram which requires extra time.

Notes	

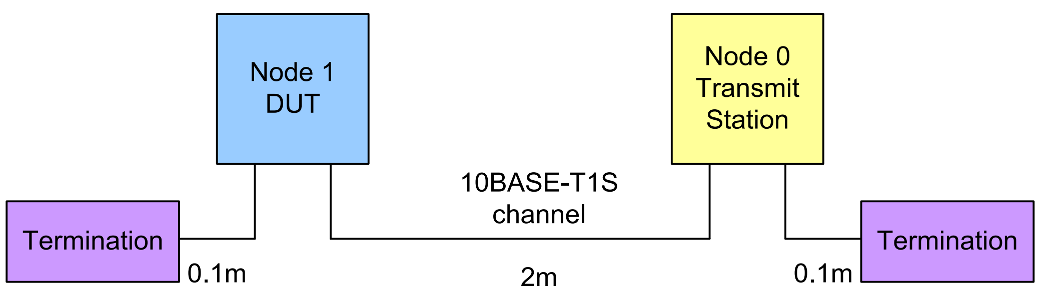
Table 7: Main test structure of Group T2

Instance Test Case #	Description	Parameter	Condition
T2.1	PLCA Timing requirements – Follower Node - BEACON	***Node_ID*** = from 1 to 16 The aPLCANodeCount should be incremented accordingly when Node_ID >1 ***TO_TIMER*** = minimum value declared by the PHY manufacturer[4], 32, 36 and 40.	repeat the test with different values of TO_TIMER and different values of the node ID/ aPLCANodeCount.

Table 8 - Test case instances definition for Group T2 - Tests case T2.1

[4] ***TO_TIMER*** = 28 will be considered if no minimum value is declared by the PHY manufacturer.

8.1.3 Group T3 – Follower node packet

Purpose	The purpose of this test is to verify important timing parameters for interoperability of nodes in PLCA mode. Under any circumstance, a packet sent by a node during its own TO shall be received by any other node within the corresponding TO boundaries.
Reference	[1], Table 147-6 10BASE-T1S delay constraints
Prerequisites	1. DUT with the capability to reset and configure its PHY. 2. DUT shall be able to be configured either as Coordinator node or as Follower node. 3. DUT must be able to indicate PLCA status via its status registers. 4. DUT must be able to send frames in the respective transmit opportunity.
DUT set-up	1. This test case is conducted with H1 topology (P2P link segment) 2. This test case is conducted with either nodes mixing-segment multi drop topology or with an arbitrary waveform generator capable to emulate a BEACON pattern (Node#1). • aPLCANodeCount = 2 • aPLCATransmitOpportunityTimer = 32 3. DUT should be configured as Follower node with aPLCALocalNodeID = 1. 4. DUT shall be ready to transmit before BEACON. 5. The used *MessageTransfer_M1A* is defined in section 7.3. 6. To avoid having the test being affected by the MAC inter-packet gap, allow at least 10us of line idle (no transmissions) before starting the test. 7. Expiration of TO timer needs to be taken into account.  *Figure 8-5: Topology for test group T3*
Test description	1. Once the configuration in all nodes is completed, enable the PLCA reconciliation sublayer functionality at Follower Node and subsequently at the coordinator node (Node #0) to start communication. 2. Test should wait for PLCA on all nodes to be activated before continuing with next step. 3. Initiate data transmission with the respective PLCA Cycle and Message transfer. 4. Measure the time between the expiration of one packet to the beginning of the next packet sent from the DUT with an oscilloscope (oscilloscope probe is connected at the MDI of the follower DUT), as shown as tmeasure in the figure below:

<table>
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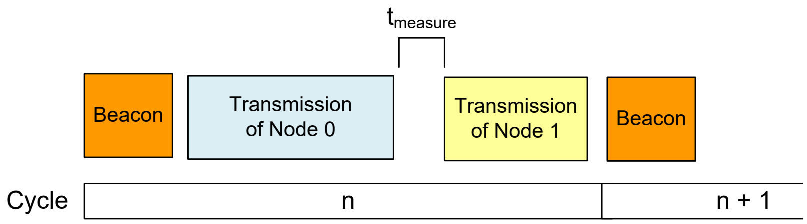
<td>


Figure 8-6: Time between node’s transmission expiration and beginning of next node’s transmission – Follower node (aPLCALocalNodeID = 1)
</td>
</tr>
<tr>
<td>Pass criteria</td>
<td>
The test case shall be considered as passed if all the following conditions are fulfilled.

The measured interval shall be between the following values:

$$\text{Time} = \text{Tcf} + t_{\text{PLCAresp}} + \text{Ttx} + \text{MII delay} + (\text{TO\_timer} \times 100\text{ns} \times (\text{Node\_ID} - 1))$$

min Tcf = 640ns
max Tcf = 1120ns
Tpd = If the oscilloscope probe is connected at the follower DUT, then there is no need to account for the propagation delay = 0ns
min $t_{PLCAresp}$ = 300ns
max $t_{PLCAresp}$ = 800ns
min Ttx = 120ns
max Ttx = 440ns
MII delay = 0ns, it is assumed 0 ns for an internal PLCA/PHY implementation.

• Min = min Tcf + min $t_{PLCAresp}$ + min Ttx + MII delay + (TO_timer x 100ns x (Node_ID - 1))
= 640ns + 300ns + 120ns + 0ns + (TO_timer x 100ns x (Node_ID -1)) =
= 1060 ns + (TO_timer x 100ns x (Node_ID – 1))

• Max = max Tcf + max $t_{PLCAresp}$ + max Ttx + MII delay + (TO_timer x 100ns x (Node_ID – 1)) =
= 1120ns + 800ns + 440ns + 0ns + (TO_timer x 100ns x (Node_ID - 1)) =
= 2360 ns + (TO_timer x 100ns x (Node_ID -1))
</td>
</tr>
<tr>
<td>Test iterations</td>
<td>Amount of test repetitions: 10</td>
</tr>
<tr>
<td>Notes</td>
<td></td>
</tr>
</table>

Table 9: Main test structure of Group T3

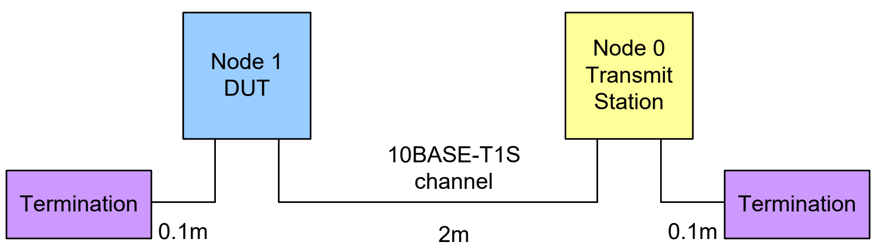
Instance Test Case #	Description	Parameter	Condition
TR3.1	PLCA Timing requirements – Follower Node - PACKET	***TO_TIMER*** = minimum value declared by the PHY manufacturer[5], 32, 36 and 40. ***Node_IDs*** = from 1 to 16 The aPLCANodeCount should be incremented accordingly when Node_ID >1	repeat the test with different values of the TO_TIMER and different values of the node ID/ aPLCANodeCount.

Table 10 - Test case instances definition for Group T3 - Tests case T3.1

[5] ***TO_TIMER*** = 28 will be considered if no minimum value is declared by the PHY manufacturer.

8.2 [D] PLCA Decoding of BEACON and message reception

8.2.1 Group D1 – Decoding of BEACON

Purpose	The purpose of this test case is to test the ability of the DUT to correctly decode the BEACON sent by the coordinator node.
Reference	[1], chapter 22.2.2.8 RXD (receive data) [1], Figure 148–3—PLCA Control state diagram, Transition from state RESYNC to EARLY_RECEIVE and back
Prerequisites	1. DUT with the capability to reset and configure its PHY. 2. DUT shall be able to be configured either as coordinator node or as follower node. 3. DUT must be able to indicate PLCA status via its status registers. 4. DUT must be able to send frames in the respective transmit opportunity.
DUT set-up	1. This test case is conducted with H1 topology (P2P link segment) 2. This test case is conducted with an arbitrary waveform generator capable of emulating a BEACON pattern (Node#0). • aPLCANodeCount = 2 • aPLCATransmitOpportunityTimer = 32 3. DUT should be configured as Follower node with aPLCALocalNodeID = 1. 4. DUT shall be ready to transmit before BEACON. 5. The used *MessageTransfer_M1C* is defined in section 7.3. 6. To avoid having the test being affected by the MAC inter-packet gap, allow at least 10us of line idle (no transmissions) before starting the test.  Figure 8-7: Topology for test group D1
Test description	1. Once the configuration in all nodes is completed, enable the PLCA reconciliation sublayer functionality at Follower Node 2. Test should wait for PLCA on all nodes to be activated before continuing with next step. 3. Initiate the transmission of BEACON following the criteria of the different test case instances. 4. Observe the transmission of the DUT with an oscilloscope.
Pass criteria	The test case shall be considered as passed if all the following condition(s) are fulfilled. • D1.1, D1.2: DUT transmits in its transmit opportunity, as BEACON command is decoded correctly. • D1.3, D1.4: DUT does not transmit, as corrupted BEACON commands shall not be decoded as such.

Test iterations	Amount of test repetitions: n.a.
Notes	

Table 11: Main test structure of Group D1

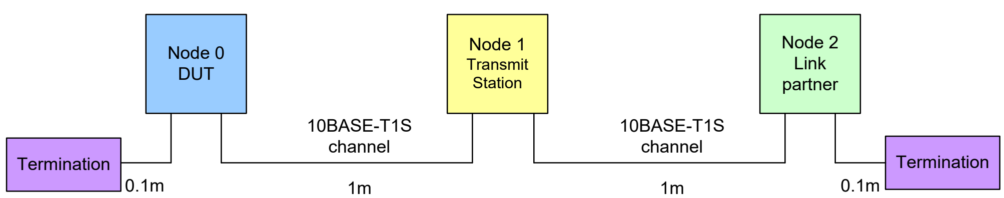
Instance Test Case #	Description	Parameter	Condition
D1.1	Nominal length BEACON (5 full N symbols)	n.a.	25 DME encoded bit times.
D1.2	Short length BEACON (4 full N symbols)	n.a.	20 DME encoded bit times.
D1.3	Short length BEACON (1 full N symbols)	n.a.	5 DME encoded bit times.
D1.4	Nominal length BEACON (5 full N symbols), but every second N symbol is inverted	n.a.	25 DME encoded bit times, with incorrect symbols

Table 12 - Test case instances definition for Group D1 - Tests cases D1.1 to D1.4

8.3 [R] PLCA Recovery

The test cases defined in this section have an informational nature and their results should not influence the final test outcome. These test cases provide information about the functionality of the PLCA, whether the DUT detects or overlooks invalid patterns and whether or not it goes into the respective recovery states. Invalid patterns capable of asserting CRS cannot necessarily be distinguished from noise in high noise environments.

8.3.1 Group R1 – Recovery of a Coordinator node

Purpose	The purpose of this test case is to test the ability of the DUT as coordinator node to correctly recover from a distorted ethernet channel.
Reference	[1], Figure 148–3—PLCA Control state diagram, RESYNC/RECOVER states.
Prerequisites	1. DUT with the capability to reset and configure its PHY. 2. DUT shall be able to be configured either as Coordinator node or as Follower node. 3. DUT must be able to indicate PLCA status via its status registers. 4. DUT must be able to send frames in the respective transmit opportunity.
DUT set-up	1. This test case is conducted with H2 topology (3 node mixing segment) 2. This test case is conducted with an arbitrary waveform generator capable of emulating a sent package (Node#1). • aPLCANodeCount = 3 • aPLCATransmitOpportunityTimer = 32 3. DUT should be configured as Coordinator node with aPLCALocalNodeID = 0. 4. DUT shall be ready to transmit before BEACON. 5. The used *MessageTransfer_M2* is defined in section 7.3.  *Figure 10 1: Topology for test group R1*
Test description	1. Once the configuration in all nodes is completed, enable the PLCA reconciliation sublayer functionality at Follower Node 2. DUT imitates the PLCA Cycle as coordinator transmitting BEACON, no data is sent, so all TO slots are empty, i.e. without transmission. 3. Initiate the transmission of the disturbance invalid pattern composed by two 11111(5B) symbols, from Node #1 at the transmit opportunity of Node #1. 4. Observe the transmission of the DUT with an oscilloscope for the next PLCA cycle.
Pass criteria	Whether or not the DUT detects the invalid pattern can result in two different scenarios:

	• If the DUT sends the BEACON regularly, with a similar interval between BEACONs, with a duration of about BEACON_TIMER + number of empty TOs * TO_TIMER, it means that the invalid pattern was filtered out as it could not be distinguished from noise. • If the DUT sends the BEACON after the invalid pattern with a delay longer than the normal one[6], with a duration much longer than BEACON_TIMER + nro. of empty TOs * TO_TIMER, it means that the DUT was able to detect the invalid pattern.
Test iterations	Amount of test repetitions: n.a.
Notes	

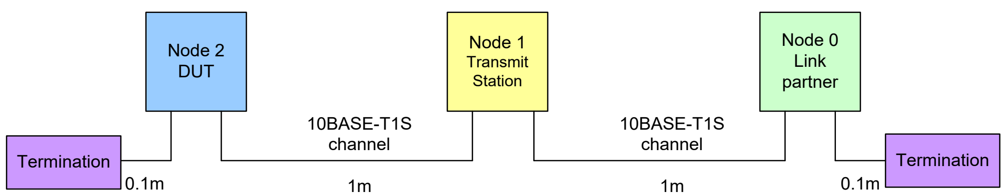
Table 13: Main test structure of Group R1

Instance Test Case #	Description	Parameter	Condition
R1.1	Recovery of a Coordinator node	n.a.	n.a.

Table 14 - Test case instances definition for Group R1 - Tests cases R1.1

[6] DUT will wait for 2 TO, then send another BEACON

8.3.2 Group R2 – Recovery of a Follower node

Purpose	The purpose of this test case is to test the ability of the DUT as follower node to correctly recover from a distorted ethernet channel.
Reference	[1], Figure 148–3—PLCA Control state diagram, RESYNC/RECOVER states.
Prerequisites	1. DUT with the capability to reset and configure its PHY. 2. DUT shall be able to be configured either as Coordinator node or as Follower node. 3. DUT must be able to indicate PLCA status via its status registers. 4. DUT must be able to send frames in the respective transmit opportunity. 5. The Link Partner configured as Coordinator node shall be able to filter out or ignore the invalid pattern, otherwise it will also enter in recovery, and this would defeat the purpose of this test, which is to analyze whether or not the DUT, configured as a Follower, enters recovery after an invalid pattern.
DUT set-up	1. This test case is conducted with H2 topology (3 node mixing segment) 2. This test case is conducted with an arbitrary waveform generator capable to emulate a sent package (Node#1). 3. DUT should be configured as Follower node with • aPLCALocalNodeID = 2. • aPLCANodeCount = 3 • aPLCATransmitOpportunityTimer = 32 4. DUT shall be ready to transmit before BEACON. 5. The used *MessageTransfer_M1C* is defined in section 7.3. 6. To avoid having the test being affected by the MAC inter-packet gap, allow at least 10us of line idle (no transmissions) before starting the test.  *Figure 8-8: Topology for test group R2*
Test description	1. Once the configuration in all nodes is completed, enable the PLCA reconciliation sublayer functionality at all nodes. 2. Initiate the transmission of the disturbance invalid pattern composed by five 11111 (5B) symbols, from Node #1 at the transmit opportunity of the Node #1. 3. Observe the transmission of the DUT with an oscilloscope. 4. Wait for the next PLCA cycle, identified by the next BEACON 5. Observe the transmission of the DUT with an oscilloscope.
Pass criteria	DUT shall never transmit in a misaligned transmit opportunity. • If the DUT sends its message in the current PLCA cycle, it means that the invalid pattern was filtered out as it could not be distinguished from noise. • If the DUT does not send its message in the disturbed PLCA cycle (test step 3) but resynchronizes and sends its message in the next undisturbed PLCA cycle

	(test step 5) starting "2 * to_timer" after the BEACON ends, it means that the DUT was able to detect the invalid pattern.
Test iterations	Amount of test repetitions: n.a.
Notes	

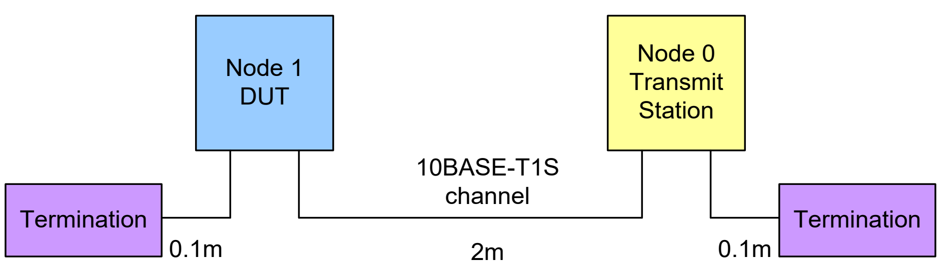
Table 15: Main test structure of Group R2

Instance Test Case #	Description	Parameter	Condition
R2.1	Recovery of a Follower node	n.a.	n.a.

Table 16 - Test case instances definition for Group R2 - Tests case R2.1

8.4 [B] PLCA Burst

8.4.1 10Group B1 – PLCA burst count > TX buffer

Purpose	The purpose of this test case is to test the ability of the DUT to correctly abort the burst sequence when the TX buffer is empty before the max burst count is reached.
Reference	[1], Figure 148–3—PLCA Control state diagram, Transition between states TRANSMIT and BURST
Prerequisites	1. DUT with the capability to reset and configure its PHY. 2. DUT shall be able to be configured either as Coordinator node or as Follower node. 3. DUT must be able to indicate PLCA status via its status registers. 4. DUT must be able to send frames in the respective transmit opportunity.
DUT set-up	1. This test case is conducted with H1 topology (P2P link segment) 2. This test case is conducted with an arbitrary waveform generator capable to emulate a COMMIT pattern (Node#0). 3. DUT should be configured as Follower node with • aPLCALocalNodeID = 1. • aPLCANodeCount = 2 • aPLCATransmitOpportunityTimer = 32 • aPLCAMaxBurstCount = 5 • aPLCABurstTimer = 128 4. DUT shall be ready to transmit before BEACON. 5. The used *MessageTransfer_M1C* is defined in section 7.3.  *Figure 8-9: Topology for test group B1*
Test description	1. Once the configuration in all nodes is completed, enable the PLCA reconciliation sublayer functionality at Follower Node 2. Initiate the transmission of 4 frames on the DUT. 3. Observe the transmission of the DUT for at least 4 PLCA cycles with an oscilloscope
Pass criteria	The test case shall be considered as passed if the DUT does send all 4 frames in the respective burst sequence, as the burst sequence shall be aborted if the TX buffer is empty before the max burst count is reached.
Test iterations	Amount of test repetitions: n.a.

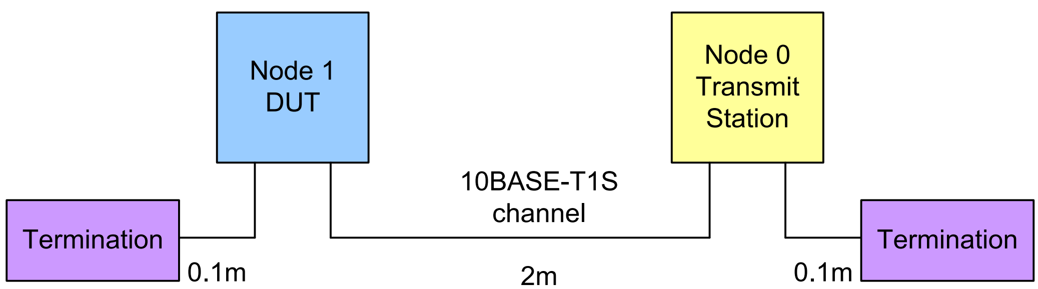
Notes	

Table 17: Main test structure of Group B1

Instance Test Case #	Description	Parameter	Condition
B1.1	Normal communication undisturbed	n.a.	n.a.

Table 18 - Test case instances definition for Group B1 - Tests cases B1.1

8.4.2 Group B2 – PLCA burst count < TX buffer

Purpose	The purpose of this test case is to test the ability of the DUT to correctly handle the burst sequence when the TX buffer still contains packets after the max burst count is reached.
Reference	[1], Figure 148–3—PLCA Control state diagram, Transition between states TRANSMIT and BURST
Prerequisites	1. DUT with the capability to reset and configure its PHY. 2. DUT shall be able to be configured either as Coordinator node or as Follower node. 3. DUT must be able to indicate PLCA status via its status registers. 4. DUT must be able to send frames in the respective transmit opportunity.
DUT set-up	1. This test case is conducted with H1 topology (P2P link segment) 2. This test case is conducted with an arbitrary waveform generator capable to emulate a COMMIT pattern (Node#0). 3. DUT should be configured as Follower node with • aPLCALocalNodeID = 1. • aPLCANodeCount = 2 • aPLCATransmitOpportunityTimer = 32 • aPLCAMaxBurstCount = 5 • aPLCABurstTimer = 128 4. DUT shall be ready to transmit before BEACON. 5. The used *MessageTransfer_M1C* is defined in section 7.3. 6. To avoid having the test being affected by the MAC inter-packet gap, allow at least 10us of line idle (no transmissions) before starting the test.  *Figure 8-10: Topology for test group B2*
Test description	1. Once the configuration in all nodes is completed, enable the PLCA reconciliation sublayer functionality at Follower Node 2. Initiate the transmission of 7 frames on the DUT. 3. Observe the transmission of the DUT for at least 4 PLCA cycles with an oscilloscope
Pass criteria	The test case shall be considered as passed if the DUT does correctly send 6 frames in a burst in the first PLCA cycle and another (1) frame in a burst in a following PLCA cycle.
Test iterations	Amount of test repetitions: n.a.

Notes	

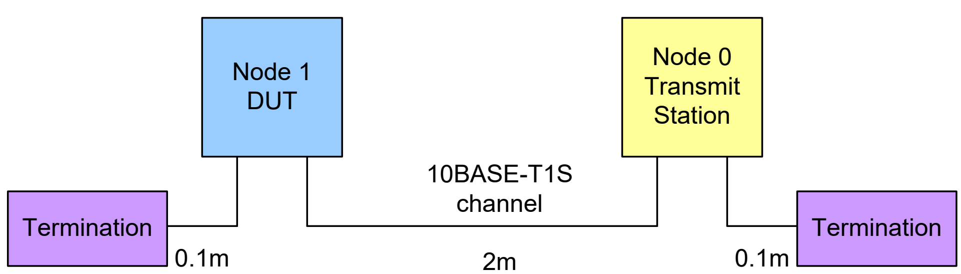
Table 19: Main test structure of Group B2

Instance Test Case #	Description	Parameter	Condition
B2.1	Normal communication undisturbed	n.a.	n.a.

Table 20 - Test case instances definition for Group B2 - Tests case B2.1

8.5 [C] PLCA Corner cases

8.5.1 Group C1 – Decoding of COMMIT near to_timer_done

Purpose	The purpose of this test case is to test the ability of the DUT to correctly decode the COMMIT sent by the coordinator node under normal conditions near the expiration of to_timer. PLCA timings are calculated such that each node shall start to transmit at the beginning of its TO, or do not transmit in that TO. This is because the propagation time for CRS assertion, deassertion and MDI transmission causes the TO counters not to be in sync between all the nodes.
Reference	[1], chapter 22.2.2.8 RXD (receive data) [1], Figure 148–3—PLCA Control state diagram, Transition between states RESYNC and RECEIVE
Prerequisites	1. DUT with the capability to reset and configure its PHY. 2. DUT shall be able to be configured either as Coordinator node or as Follower node. 3. DUT must be able to indicate PLCA status via its status registers. 4. DUT must be able to send frames in the respective transmit opportunity.
DUT set-up	1. This test case is conducted with H1 topology (P2P link segment) 2. This test case is conducted with an arbitrary waveform generator capable to emulate a COMMIT pattern (Node#0). 3. DUT should be configured as Follower node with • aPLCALocalNodeID = 1 • aPLCANodeCount = 2 • aPLCATransmitOpportunityTimer = 32 4. DUT shall be ready to receive before BEACON. 5. The used *MessageTransfer_M1C* is defined in section 7.3. 6. To avoid having the test being affected by the MAC inter-packet gap, allow at least 10us of line idle (no transmissions) before starting the test.  *Figure 8-11: Topology for test group C1*
Test description	1. Once the configuration in all nodes is completed, enable the PLCA reconciliation sublayer functionality at Follower Node 2. Initiate the transmission of BEACON followed by delayed COMMIT sequence, composed of two SYNC [J] symbols, following the criteria of the different test case instances.

	3. Observe the reception buffer of the DUT
Pass criteria	The test case shall be considered as passed if all the following condition(s) are fulfilled. • The DUT shall not violate Node #0's transmit opportunity interpreting that Node #0 has yielded its transmit opportunity. DUT sends the message, because it detects the COMMIT correctly.
Test iterations	Amount of test repetitions: n.a.
Notes	

Table 21: Main test structure of Group C1

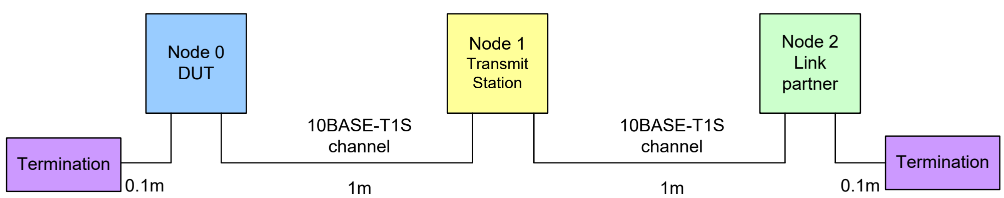
Instance Test Case #	**Description**	**Parameter**	**Condition**
C1.1	COMMIT before "to_timer_done"-condition of Transmit Opportunity of Node #0	Delayed COMMIT sequence from (to_timer-20) to (to_timer-7) bit times before "to_timer_done"	COMMIT sequence gets sent delayed cyclically in step of 1 bit time (100 ns) per PLCA Cycle. The maximum delayed time should be to_timer + CRS deassert min – CRS assert max – MII propagation time – PDELAY[7] – tPLCAresp = to_timer - 700ns. Starting from the end of BEACON transmission. According to the PLCA Control State Diagram, the to_timer is stopped once carrier sense is asserted. This causes a transition from WAIT_TO to EARLY_RECEIVE. To transition to the RECEIVE state, a JJ (COMMIT) or HH (SYNC) must be received. This does require 800 ns (minimum). The to_timer is, however, already stopped because carrier has been sensed. If there is no transition into RECEIVE before carrier sense goes away, then the transition into the RESYNC state takes place and waits for a BEACON.

Table 22 - Test case instances definition for Group C1 - Tests case C1.1

[7] P_{DELAY} is the propagation delay on the line between the testbench node to the DUT. 5ns/m; i.e. ~10ns.

8.5.2 Group C2 – Recovery of coordinator node near to_timer_done

This test case has an informational nature, and its result should not influence the final test outcome. This test case provides information about the functionality of the PLCA, whether the DUT detects or overlooks invalid patterns and whether or not it goes into the respective recovery states. Invalid patterns capable of asserting CRS cannot necessarily be distinguished from noise in high noise environments.

Purpose	The purpose of this test case is to test the ability of the DUT to correctly recover from a collision in the DUTs transmit opportunity near the expiration of to_timer
Reference	[1], Figure 148–3—PLCA Control state diagram, Transition between states RESYNC and EARLY_RECEIVE
Prerequisites	1. DUT with the capability to reset and configure its PHY. 2. DUT shall be able to be configured either as Coordinator node or as Follower node. 3. DUT must be able to indicate PLCA status via its status registers. 4. DUT must be able to send frames in the respective transmit opportunity.
DUT set-up	1. This test case is conducted with H2 topology (3 node mixing segment) 2. This test case is conducted with an arbitrary waveform generator capable to emulate a sent package (Node#1). 3. DUT should be configured as Coordinator node with • aPLCALocalNodeID = 0 • aPLCANodeCount = 3 • aPLCATransmitOpportunityTimer = 32 4. DUT shall be ready to transmit before BEACON. 5. The used *MessageTransfer_M3* is defined in section 7.3.  *Figure 10 1: Topology for test group C2.1*
Test description	1. Once the configuration in all nodes is completed, enable the PLCA reconciliation sublayer functionality at Follower Node 2. DUT imitates the PLCA Cycle as coordinator transmitting BEACON, no data is sent, so all TO slots are empty, i.e. without transmission. 3. Initiate the transmission of the disturbance pattern 1111 (edge transition each 40ns) with a length of 1200ns from Node #1 following the criteria of the different test case instances 4. Observe the transmission of the DUT with an oscilloscope.
Pass criteria	Whether or not the DUT detects the invalid pattern can result in two different scenarios: • If the DUT sends the BEACON regularly, with a similar interval between BEACONs, with a duration of about BEACON_TIMER + number of empty TOs *

	TO_TIMER, it means that the invalid pattern was filtered out as it could not be distinguished from noise. • If the DUT sends the BEACON after the invalid pattern with a delay longer than the normal one, with a duration much longer than BEACON_TIMER + number of empty TOs * TO_TIMER, it means that the DUT was able to detect the invalid pattern.
Test iterations	Amount of test repetitions: n.a.
Notes	

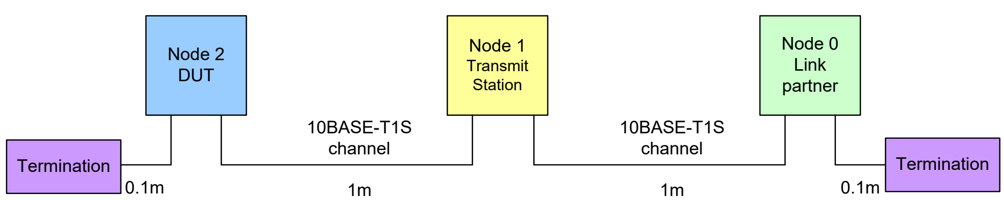
Table 23: Main test structure of Group C2

Instance Test Case #	Description	Parameter	Condition
C2.1	Disturbance close to “to_timer_done”-condition of DUT	Delayed disturbance violating DUT’s transmit opportunity from (to_timer-20) to (to_timer-10) bit times before “to_timer_done”	– The disturbance in test step 3 gets sent delayed cyclically in step of 1 bit time – Repeat test case until the delayed disturbance is sent at (to_timer-10) bit times before “to_timer_done”. Starting from the end of BEACON transmission.

Table 24 - Test case instances definition for Group C2 - Tests case C2.1

8.5.3 Group C3 – Recovery of follower node near to_timer_done

This test case has an informational nature, and its result should not influence the final test outcome. This test case provides information about the functionality of the PLCA, whether the DUT detects or overlooks invalid patterns and whether it goes into the respective recovery states. Invalid patterns capable of asserting CRS cannot necessarily be distinguished from noise in high noise environments.

Purpose	The purpose of this test case is to test the ability of the DUT to correctly recover from a collision in the DUTs transmit opportunity near the expiration of to_timer.
Reference	[1], Figure 148–3—PLCA Control state diagram, Transition between states RESYNC and EARLY_RECEIVE
Prerequisites	1. DUT with the capability to reset and configure its PHY. 2. DUT shall be able to be configured either as Coordinator node or as Follower node. 3. DUT must be able to indicate PLCA status via its status registers. 4. DUT must be able to send frames in the respective transmit opportunity. 5. The Link Partner configured as Coordinator node shall be able to filter out or ignore the invalid pattern, otherwise it will also enter in recovery, and this would defeat the purpose of this test, which is to analyze whether or not the DUT, configured as a Follower, enters recovery after an invalid pattern.
DUT set-up	1. This test case is conducted with H2 topology (3 node mixing segment) 2. This test case is conducted with an arbitrary waveform generator capable to emulate a sent package (Node#1). 3. DUT should be configured as Follower node with • aPLCALocalNodeID = 1 • aPLCANodeCount = 3 • aPLCATransmitOpportunityTimer = 32 4. DUT shall be ready to transmit before BEACON. 5. The used *MessageTransfer_M1A* is defined in section 7.3. 6. To avoid having the test being affected by the MAC inter-packet gap, allow at least 10us of line idle (no transmissions) before starting the test.  *Figure 8-12: Topology for test group C3*
Test description	1. Once the configuration in all nodes is completed, enable the PLCA reconciliation sublayer functionality at Follower Node 2. Initiate the transmission of a BEACON from Node #0

	3. Initiate the transmission of the disturbance invalid pattern 1111 (edge transition each 40ns) with a length of 1200ns from Node #1 following the criteria of the different test case instances. 4. Observe the transmission of the DUT with an oscilloscope.
Pass criteria	DUT shall never transmit in a misaligned transmit opportunity. – If the DUT sends its message in the current PLCA cycle, it means that the invalid pattern was filtered out as it could not be distinguished from noise. – If the DUT does not send its message in the disturbed PLCA cycle (test step 3) but resynchronizes and sends its message in the next undisturbed PLCA cycle starting "2 * to_timer" after the BEACON ends, it means that the DUT was able to detect the invalid pattern.
Test iterations	Amount of test repetitions: n.a.
Notes	

Table 25: Main test structure of Group C3

Instance Test Case #	Description	Parameter	Condition
C3.1	Disturbance close to “to_timer_done”-condition of DUT	Delayed disturbance violating the TO before DUT’s transmit opportunity from (to_timer-20) to (to_timer-12) bit times before “to_timer_done”	– The disturbance in test step 3 gets sent delayed cyclically in step of 1 bit time – Repeat test case until the delayed disturbance is sent at (to_timer-12) bit times before “to_timer_done”. Starting from the end of BEACON transmission. – Collision could happen if the DUT is able to filter out the invalid pattern and the delay plus invalid pattern duration are longer than the to_timer.

Table 26 - Test case instances definition for Group C3 - Tests case C3.1

9 APPENDIX

9.1 Test station setup

The test station for 10BASE-T1S PLCA tests consists of 3 types of nodes and can perform all tests that are specified in this document:

- Transmit Station.
- DUT
- Link partner

Additionally, there is an oscilloscope connected to the 10BASE-T1S channel to observe the communication as needed in the respective test cases.

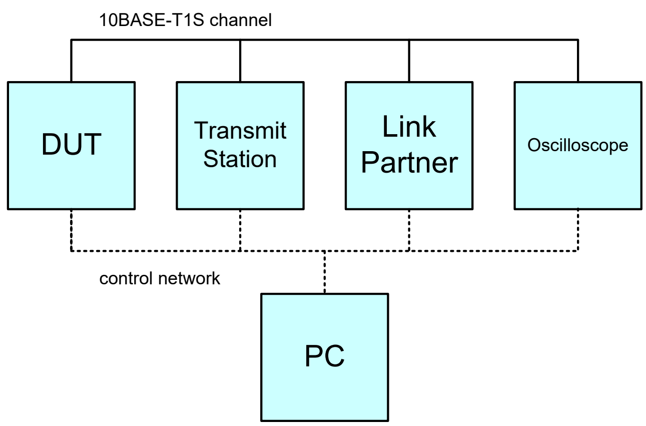


Figure 9-1: Test station setup for 10BASE-T1S PLCA tests

The actual test station configuration is described in the test case setup of each test case.

9.1.1 Transmit Station

The 10BASE-T1S Transmit Station node consists of software and hardware that is capable of transmitting precisely timed and formatted packets or dedicated patterns on to the 10BASE-T1S network.

It consists of an FPGA board/Pattern Generator with attached PMD-transceiver which is running the lower tester software. It gets controlled by the test system according to the executed test case requirements. The Transmit Station is denoted with a resolution of at least 20 ns per data point.

9.1.2 DUT

The 10BASE-T1S DUT node will consist of software and hardware that is capable of controlling and supervising the DUT.

The DUT node setup is shown in Figure 9-2 and Figure 9-3. It consists of a host board with attached DUT which is running the upper tester software. It gets controlled by the test system according to the executed test case requirements.

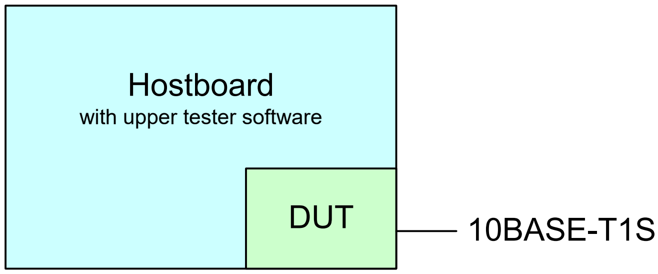


Figure 9-2: DUT setup for MII or MACPHY 10BASE-T1S Implementation

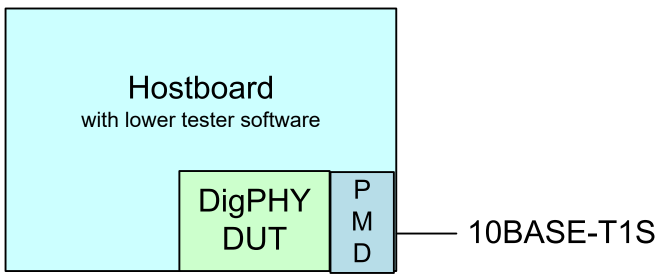


Figure 9-3: DUT setup for DigPHY 10BASE-T1S Implementation

9.1.3 Link partner

The 10BASE-T1S Link partner will consist of software and hardware that is capable of controlling and supervising a 10BASE-T1S PHY to participate on the 10BASE-T1S network.

The link partner node setup is shown in Figure A.1. It consists of a host board with attached DUT which is running the lower tester software. It gets controlled by the test system according to the executed test case requirements.

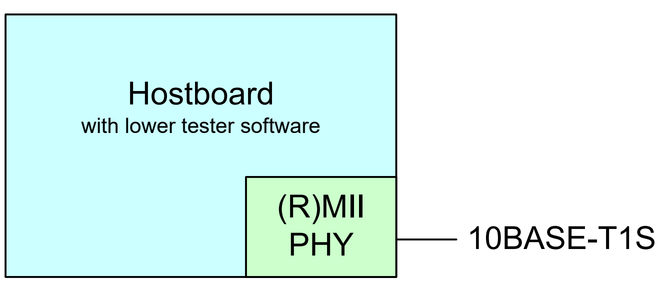


Figure 9-4: 10BASE-T1S Link partner setup

9.2 List of Tables

9.3 List of Figures