OPEN Alliance 10BASE-T1S PMD Transceiver Interface

TC14 – Interoperability Specifications

Author & Company	See Contributing Members on Page 2
Title	OPEN Alliance 10BASE-T1S PMD Transceiver Interface
Version	1.5
Date	November 8th, 2022
Status	Final
Restriction Level	Public

Version Control of Document

Version	Author	Description	Date
0.1	Piergiorgio Beruto	First Version	2019-07-08
0.2	Piergiorgio Beruto	Minor fixes	2019-07-12
0.3	Piergiorgio Beruto	Add management interface specification	2019-07-19
0.4	Piergiorgio Beruto	Comments resolution #1	2019-09-20
0.5	Piergiorgio Beruto	Editorial Clean-up	2019-10-30
1.2	Piergiorgio Beruto	Comments resolution #2	2019-11-25
1.3	Matthias Muth	Pinning recommendations added	2020-05-18
1.4	Piergiorgio Beruto	Editorial cleanup	2020-07-22
1.5	Piergiorgio Beruto	Add Topology discovery, RX pin RZ-I encoding, ED pin filtering, and Wake/Sleep support.	2022-11-08

Restriction level history of Document

Version	Restriction Level	Description	Date
0.1	OPEN Members Only	First Version	2019-07-08
0.2	OPEN Members Only	Minor fixes	2019-07-12
0.3	OPEN Members Only	Add management interface specification	2019-07-19
0.4	OPEN Members Only	Comments resolution #1	2019-09-20
0.5	OPEN Members Only	Editorial Clean-up	2019-10-30
1.2	OPEN Members Only	Comments resolution #2	2019-11-25
1.3	OPEN Members Only	Pinning recommendations added	2020-05-18
1.4	OPEN Members Only	Editorial cleanup	2020-07-22
1.5	Public	Add Topology discovery, RX pin RZ-I encoding, ED pin filtering, and Wake/Sleep support.	2022-11-08

Contributing Members

Name	Company
Piergiorgio Beruto [Author]	onsemi
Matthias Muth	NXP
Clemens De Haas	NXP
Venkat Iyer	Microchip
Tim Baggett	Microchip
Pablo Ventura	ADI
John Cullinane	ADI
Tobias Belitz	Renesas
Antonio Orzelli	Canova Tech
Pierluigi Dito	Canova Tech
Marko Moch	Cariad
Magnus Maria Hell	Infineon

OPEN Alliance Specification Copyright Notice and Disclaimer

A. OPEN Specification Ownership and Usage Rights

As between OPEN Alliance and OPEN Alliance Members whose contributions were incorporated in this OPEN Specification (the "Contributing Members"), the Contributing Members own the worldwide copyrights in and to their given contributions. Other than the Contributing Members' contributions, OPEN Alliance owns the worldwide copyrights in and to compilation of those contributions forming this OPEN Specification. For OPEN Alliance Members (as that term is defined in the OPEN Alliance Bylaws), OPEN Alliance permits the use of this OPEN Specification on the terms in the OPEN Alliance Intellectual Property Rights Policy and the additional applicable terms below. For non-members of OPEN Alliance, OPEN Alliance permits the use of this OPEN Specification on the terms in the OPEN Alliance Specification License Agreement (available here: http://www.opensig.org/Automotive-Ethernet-Specifications/) and the additional applicable terms below. The usage permissions referenced and described here relate only to this OPEN Specification and do not include or cover a right to use any specification published elsewhere and referred to in this OPEN Specification. By using this OPEN Specification, you hereby agree to the following terms and usage restrictions:

A.i. Rights and Usage Restrictions Specific to OPEN Alliance Members

FOR OPEN ALLIANCE MEMBERS ONLY: In addition to the usage terms and restrictions granted to Members in the OPEN Alliance Intellectual Property Rights Policy, Members' use of this OPEN Specification is subject this Copyright Notice and Disclaimer. Members of OPEN Alliance have the right to use this OPEN Specification solely (i) during the term of a Member's membership in OPEN Alliance and subject to the Member's continued membership in good standing in OPEN Alliance; (ii) subject to the Member's continued compliance with the OPEN Alliance governance documents, Intellectual Property Rights Policy, and the applicable OPEN Alliance Promoter or Adopter Agreement, as applicable; and (iii) for internal business purposes and solely to use the OPEN Specification for implementation of this OPEN Specification in the Member's products and services, but only so long as Member does not distribute, publish, display, or transfer this OPEN Specification to any third party, except as expressly set forth in Section 11 of the OPEN Alliance Intellectual Property Rights Policy. Except and only to the extent required to use this OPEN Specification internally for implementation of this OPEN Specification in Member's products and services, Member shall not modify, alter, combine, delete portions of, prepare derivative works of, or create derivative works based upon this OPEN Specification. If Member creates any modifications, alterations, or other derivative works of this OPEN Specification as permitted to use the same internally for implementation of this OPEN Specification in Member's products and services, all such modifications, alterations, or other derivative works shall be deemed part of, and licensed to such Member under the same restrictions as, this OPEN Specification. For the avoidance of doubt, Member shall not include all or any portion of this OPEN Specification in any other technical specification or technical material, product manual, marketing material, or any other material without OPEN Alliance's prior written consent. All rights not expressly granted to Member in the OPEN Alliance Intellectual Property Rights Policy are reserved;

A.ii. Rights and Usage Restrictions Specific to Non-members of OPEN Alliance

FOR NON-MEMBERS OF OPEN ALLIANCE ONLY: Use of this OPEN Specification by anyone who is not a Member in good standing of OPEN Alliance is subject to your agreement to the OPEN Alliance Specification License Agreement (available here: http://www.opensig.org/Automotive-Ethernet-Specifications/) and the additional terms in this Copyright Notice and Disclaimer. Non-members have the right to use this OPEN Specification solely (i) subject to the non-member's continued compliance with the OPEN Alliance Specification License Agreement; and (ii) for internal business purposes and solely to use the OPEN Specification for implementation of this OPEN Specification in the non-member's products and services, but only so long as non-member does not distribute, publish, display, or transfer this OPEN Specification to any third party, unless and only to the extent expressly set forth in the OPEN Alliance Specification License Agreement. Except and only to the extent required to use this OPEN Specification internally for implementation of this OPEN Specification in non-member's products and services, non-member shall not modify, alter, combine, delete portions of, prepare derivative works of, or create derivative works based upon this OPEN Specification. If non-member creates any modifications, alterations, or other derivative works of this OPEN Specification as permitted to use the same internally for implementation of this OPEN Specification in non-member's products and services, all such modifications, alterations, or other derivative works shall be deemed part of, and licensed to such non-member under the same restrictions as, this OPEN Specification. For the avoidance of doubt, non-member shall not include all or any portion of this OPEN Specification in any other technical specification or technical material, product manual, marketing material, or any other material without OPEN Alliance's prior written consent. All rights not expressly granted to non-member in the OPEN Alliance Specification License Agreement are reserved.

B. Terms Applicable to both Members and Non-members of OPEN Alliance

B.i. Patents, Trademarks, and other Rights:

OPEN Alliance has received no Patent Disclosure and Licensing Statements related to this OPEN Specification. Therefore, this OPEN Specification contains no specific disclaimer related to third parties that may require a patent license for their Essential Claims. Having said that, the receipt of this OPEN Specification shall not operate as an assignment of or license under any patent, industrial design, trademark, or other rights as may subsist in or be contained in or reproduced in this OPEN Specification; and the implementation of this OPEN Specification could require such a patent license from a third party. You may not use any OPEN Alliance trademarks or logos without OPEN Alliance's prior written consent.

B.ii. Disclaimers and Limitations of Liability:

THIS OPEN SPECIFICATION IS PROVIDED ON AN "AS IS" BASIS, AND ALL REPRESENTATIONS, WARRANTIES, AND GUARANTEES, EITHER EXPLICIT, IMPLIED, STATUTORY, OR OTHERWISE, ARE EXCLUDED AND DISCLAIMED UNLESS (AND THEN ONLY TO THE EXTENT THEY ARE) MANDATORY UNDER LAW. ACCORDINGLY, OPEN ALLIANCE AND THE CONTRIBUTING MEMBERS MAKE NO REPRESENTATIONS OR WARRANTIES OR GUARANTEES WITH REGARD TO THIS OPEN SPECIFICATION OR THE INFORMATION (INCLUDING ANY SOFTWARE) CONTAINED HEREIN. OPEN ALLIANCE

AND ALL CONTRIBUTING MEMBERS HEREBY EXPRESSLY DISCLAIM ANY AND ALL SUCH EXPRESS, IMPLIED, STATUTORY, AND ALL OTHER REPRESENTATIONS, WARRANTIES, AND GUARANTEES, INCLUDING WITHOUT LIMITATION ANY AND ALL WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR USE, TITLE, NON-INFRINGEMENT OF OR ABSENCE OF THIRD PARTY RIGHTS, AND/OR VALIDITY OF RIGHTS IN THIS OPEN SPECIFICATION; AND OPEN ALLIANCE AND THE CONTRIBUTING MEMBERS MAKE NO REPRESENTATIONS AS TO THE ACCURACY OR COMPLETENESS OF THIS OPEN SPECIFICATION OR ANY INFORMATION CONTAINED HEREIN. WITHOUT LIMITING THE FOREGOING, OPEN ALLIANCE AND/OR CONTRIBUTING MEMBERS HAS(VE) NO OBLIGATION WHATSOEVER TO INDEMNIFY OR DEFEND YOU AGAINST CLAIMS RELATED TO INFRINGEMENT OR MISAPPROPRIATION OF INTELLECTUAL PROPERTY RIGHTS.

OPEN ALLIANCE AND CONTRIBUTING MEMBERS ARE NOT, AND SHALL NOT BE, LIABLE FOR ANY LOSSES, COSTS, EXPENSES, OR DAMAGES OF ANY KIND WHATSOEVER (INCLUDING WITHOUT LIMITATION DIRECT, INDIRECT, SPECIAL, INCIDENTAL, CONSEQUENTIAL, PUNITIVE, AND/OR EXEMPLARY DAMAGES) ARISING IN ANY WAY OUT OF USE OR RELIANCE UPON THIS OPEN SPECIFICATION OR ANY INFORMATION HEREIN. NOTHING IN THIS DOCUMENT OPERATES TO LIMIT OR EXCLUDE ANY LIABILITY FOR FRAUD OR ANY OTHER LIABILITY WHICH IS NOT PERMITTED TO BE EXCLUDED OR LIMITED BY OPERATION OF LAW.

B.iii. <u>Compliance with Laws and Regulations</u>:

NOTHING IN THIS DOCUMENT OBLIGATES OPEN ALLIANCE OR CONTRIBUTING MEMBERS TO PROVIDE YOU WITH SUPPORT FOR, OR RELATED TO, THIS OPEN SPECIFICATION OR ANY IMPLEMENTED PRODUCTS OR SERVICES. NOTHING IN THIS OPEN SPECIFICATION CREATES ANY WARRANTIES OR GUARANTEES, EITHER EXPRESS OR IMPLIED, STATUTORY OR OTHERWISE, REGARDING ANY LAW OR REGULATION. OPEN ALLIANCE AND CONTRIBUTING MEMBERS EXPRESSLY DISCLAIM ALL LIABILITY, INCLUDING WITHOUT LIMITATION, LIABILITY FOR NONCOMPLIANCE WITH LAWS, RELATING TO USE OF THE OPEN SPECIFICATION OR INFORMATION CONTAINED HEREIN. YOU ARE SOLELY RESPONSIBLE FOR THE COMPLIANCE OF IMPLEMENTED PRODUCTS AND SERVICES WITH ANY SUCH LAWS AND REGULATIONS, AND FOR OBTAINING ANY AND ALL REQUIRED AUTHORIZATIONS, PERMITS, AND/OR LICENSES FOR IMPLEMENTED PRODUCTS AND SERVICES RELATED TO SUCH LAWS AND REGULATIONS WITHIN THE APPLICABLE JURISDICTIONS.

IF YOU INTEND TO USE THIS OPEN SPECIFICATION, YOU SHOULD CONSULT ALL APPLICABLE LAWS AND REGULATIONS. COMPLIANCE WITH THE PROVISIONS OF THIS OPEN SPECIFICATION DOES NOT CONSTITUTE COMPLIANCE TO ANY APPLICABLE LEGAL OR REGULATORY REQUIREMENTS. IMPLEMENTERS OF THIS OPEN SPECIFICATION ARE SOLELY RESPONSIBLE FOR OBSERVING AND COMPLYING WITH THE APPLICABLE LEGAL AND REGULATORY REQUIREMENTS. WITHOUT LIMITING THE FOREGOING, YOU SHALL NOT USE, RELEASE, TRANSFER, IMPORT, EXPORT, AND/OR RE-EXPORT THIS OPEN SPECIFICATION OR ANY INFORMATION CONTAINED HEREIN IN ANY MANNER PROHIBITED UNDER ANY APPLICABLE LAWS AND/OR REGULATIONS, INCLUDING WITHOUT LIMITATION U.S. EXPORT CONTROL LAWS.

B.iv. Automotive Applications Only: Without limiting the foregoing disclaimers or limitations of liability in any way, this OPEN Specification was developed for automotive applications only. This OPEN Specification has neither been developed, nor tested for, non-automotive applications.

B.v. Right to Withdraw or Modify:
OPEN Alliance reserves the right to (but is not obligated to) withdraw, modify, or replace this OPEN Specification at any time, without notice.

Contents

Introduction

The 10BASE-T1S is a 10 Mbps Ethernet PHY defined by the IEEE 802.3cg project (Clause 147). It is capable of operating in full/half duplex point-to-point or half-duplex multidrop mode over a single unshielded twisted pair (UTP) cable up to 25m long.

Furthermore, the IEEE802.3cg project defines the new Physical Layer Collision Avoidance (PLCA) Reconciliation Sublayer (Clause 148) meant to provide improved determinism to the CSMA/CD media access method. PLCA works in conjunction with the 10BASE-T1S PHY operating in multi-drop mode.

The 10BASE-T1S PHY is intended to cover the low-speed/low-cost applications in industrial and automotive environments. The large number of pins (16) required by the MII interface specified by the IEEE 802.3 in Clause 22 is one of the major cost factors that must be addressed to fulfill this objective.

The 10BASE-T1S PMD Transceiver is a CAN-like solution suited for embedded systems where the digital portion of the PHY is fully integrated into an MCU, an Ethernet switch core, or any other suitable host where only the analog part is left into a separate chip (i.e., the PMD transceiver).

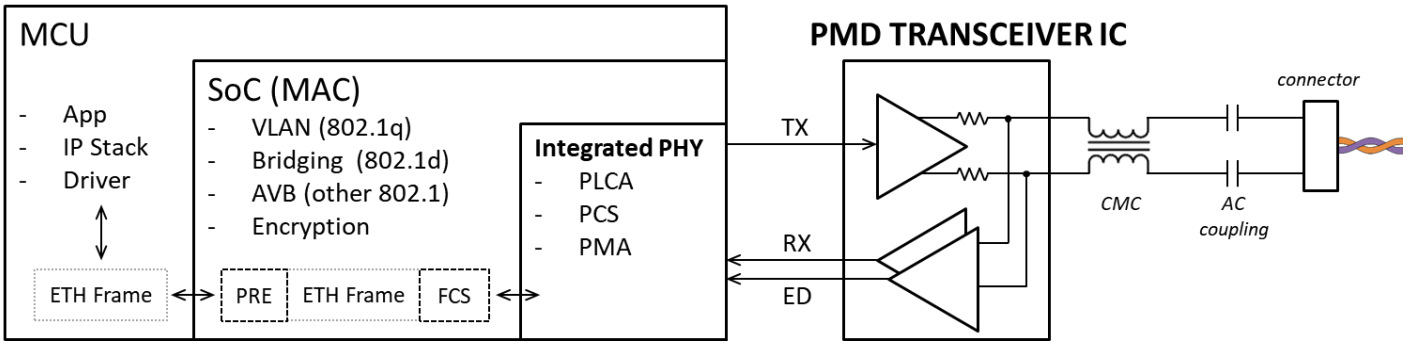


Figure 1: Example of a 10BASE-T1S integrated PHY with an external PMD transceiver

This solution, similar to the well-known CAN and FlexRay transceiver approach, features a simple and cost-effective 3-pin clock-less interface between the host controller and the PMD transceiver chip.

The PMD transceiver may support half-duplex, full-duplex, or both modes of operation.

Abbreviation/Symbols

*****	May indicate either the arithmetical multiply operation or the logical AND function
+	May indicate either the arithmetical sum operation or the logical OR function
BER	Bit Error Rate
CAN	Controller Area Network
DME	Differential Manchester Encoding
IC	Integrated Circuit
MCU	Micro Controller Unit
MDC	MDIO Clock
MDIO	Management Data Input/Output
PCB	Printed Circuit Board
PMD	Physical Medium Dependent
POR	Power On Reset
NRZ	Non-Return to Zero encoding
RX	Receive
RZI	Return to Zero Inverted encoding
TX	Transmit
WUD	Wake-Up Detect
WUP	Wake-Up Pulse
WUT	Wake-Up Tone

1 Scope

The purpose of this document is to specify a clock-less interface between a 10BASE-T1S PMA (herein called host controller) and an analog frontend device (herein called “PMD transceiver”, or just “transceiver”). The normative requirements are provided in the form of interworking specifications, including the behavior and timings of the signals. The definition of the actual implementation of the transceiver and the host controller is beyond the scope of this document.

The detailed specification numbers shall be understood from the perspective of the related device and not as global signals specifications.

2 Normative References

The following documents are referred to in the text in such a way that some or all of their content constitutes the requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

[1] IEEE 802.3cg Task Force, "IEEE Std 802.3cg™-2019, Amendment 5: Physical Layer Specifications and Management Parameters for 10 Mb/s Operation and Associated Power Delivery over a Single Balanced Pair of Conductors," IEEE Standards Association, New York, 2019.

[2] IEEE Computer Society, "IEEE Standard for Ethernet," IEEE Standards Association, New York, 2018.

3 Terms and Definitions

For the purposes of this document, the terms and definitions given in [1] and [2] apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

— ISO Online browsing platform: available at https://www.iso.org/obp

— IEC Electropedia: available at http://www.electropedia.org/

3.1
rise time

The time a signal takes to rise from 20% to 80% of its nominal reference voltage.

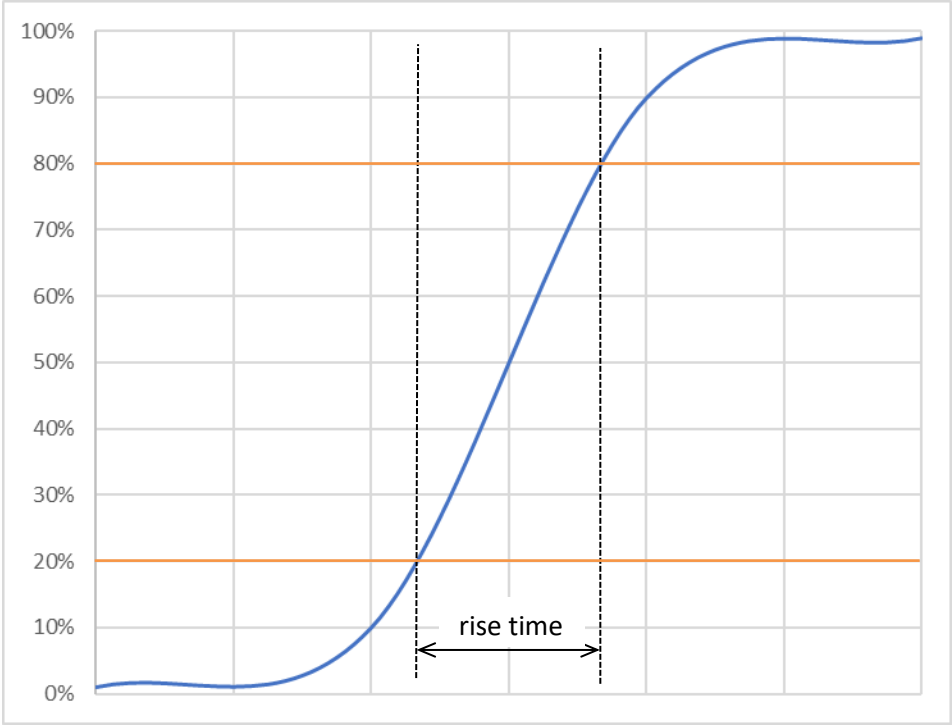


Figure 2: Signal rise time definition

3.2
fall time

The time a signal takes to fall from 80% to 20% of its nominal reference voltage.

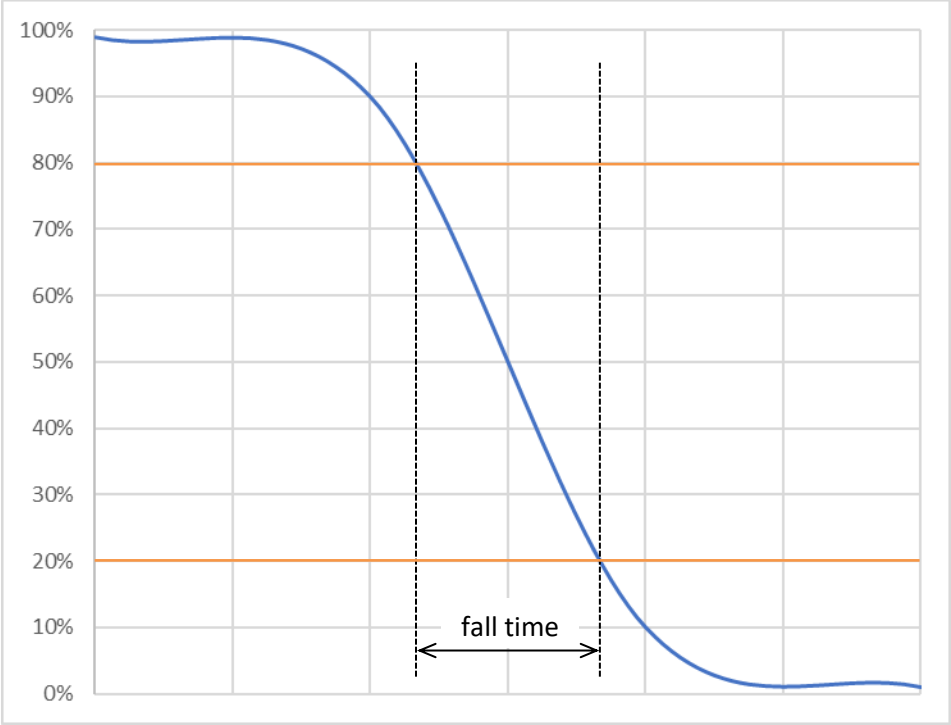


Figure 3: Signal fall time definition

4 Interface Definition

4.1 Overview

The interface between the 10BASE-T1S PMD transceiver and the digital host consists of three pins, one for the transmit path and two for the receive path.

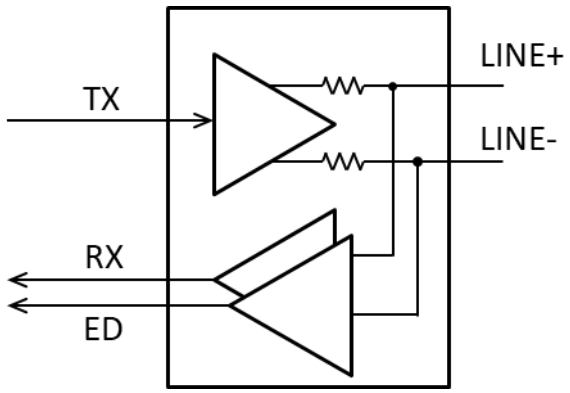


Figure 4: PMD Transceiver Pins

The TX pin encodes the "data" and "data enable" logic functions. According to DME rules defined in Clause 147.4.2 of [1], those are needed to drive the line interface with either a positive/negative differential voltage or high impedance. The TX pin is also used to enter or leave the low-power and configuration modes.

The RX pin produces a low pulse each time the differential voltage at the LINE pins switches from positive to negative or vice-versa, following an RZI encoding scheme.
The ED pin is essentially the filtered output of a window comparator that indicates whether the differential voltage at the LINE pins is contained within a specific amplitude band centered around zero.

The host controller uses the RX and ED pins to decode DME data, detect activity, and detect collisions[1] at the line interface.

Additionally, when the PMD transceiver is set to configuration mode, the RX and ED pins are used as MII management interface (MIIM).

All digital I/O signals should be implemented according to the appropriate JEDEC digital interface standard for the desired I/O voltage.

[1] When PLCA is enabled, physical collisions are not expected to happen.

4.2 Functional Modes

The transceiver interface features a single TX pin to perform the required transmission functions and to convey the following commands:

- TRANSMIT
- RESET
- LOWPWRRQ
- CONFIG

The working principle of the TX interface is that the host controller generates pulses of different duration to drive the transceiver into the different modes of operation. The transceiver operations are stateful and clock-less to minimize power consumption and electromagnetic emissions.

The TRANSMIT command causes the transceiver to actively drive the line interface and encode subsequent pulses on the TX pin into a DME stream. The line interface is released (high-Z) when a RESET command is issued, or the jabber timer expires (see 4.2.1.2).

The host can issue a RESET command anytime it is powered to ensure proper alignment of the host controller state with the transceiver state. This allows, for example, protection against spurious resets of the controller and recovering from unwanted state changes in case of HW/SW faults. For recommendations on how to achieve safe operation of the transceiver, see chapter 5.

The LOWPWRRQ command can be used to put the transceiver in a low-power mode. This is represented by the transceiver being in LOW_POWER state. From the LOW_POWER state, the transceiver goes into the LOW_POWER_WAKE state upon detecting a local or remote wakeup condition. The LOW_POWER_WAKE state can be left using a RESET command when the ED pin is low. While the low power mode is in effect, the transceiver provides status information to the host via the RX and ED pins, as shown in Figure 5. For a description of low power mode, see chapter 7.

The CONFIG command can be used to enter configuration mode. While in configuration mode, the RX and ED pins are used as the MDC and MDIO pins of a standard MIIM interface to access configuration registers. The configuration mode can be left using a RESET command. For a description of configuration mode, see chapter 6.

Both the CONFIG and LOWPWRRQ commands can only be issued when the transceiver is in NORMAL state.

After power-on reset (POR), the transceiver enters the LOW_POWER_WAKE state and waits for a RESET command to enter NORMAL operating mode.

4.2.1 PMD State Diagram

The transceiver shall comply with the state diagram in Figure 5 to switch between the different functional modes.

Note that the PMD transceiver shall never drive a differential voltage at the line interface unless it is in the TRANSMITTING state and the loop-back mode is disabled.

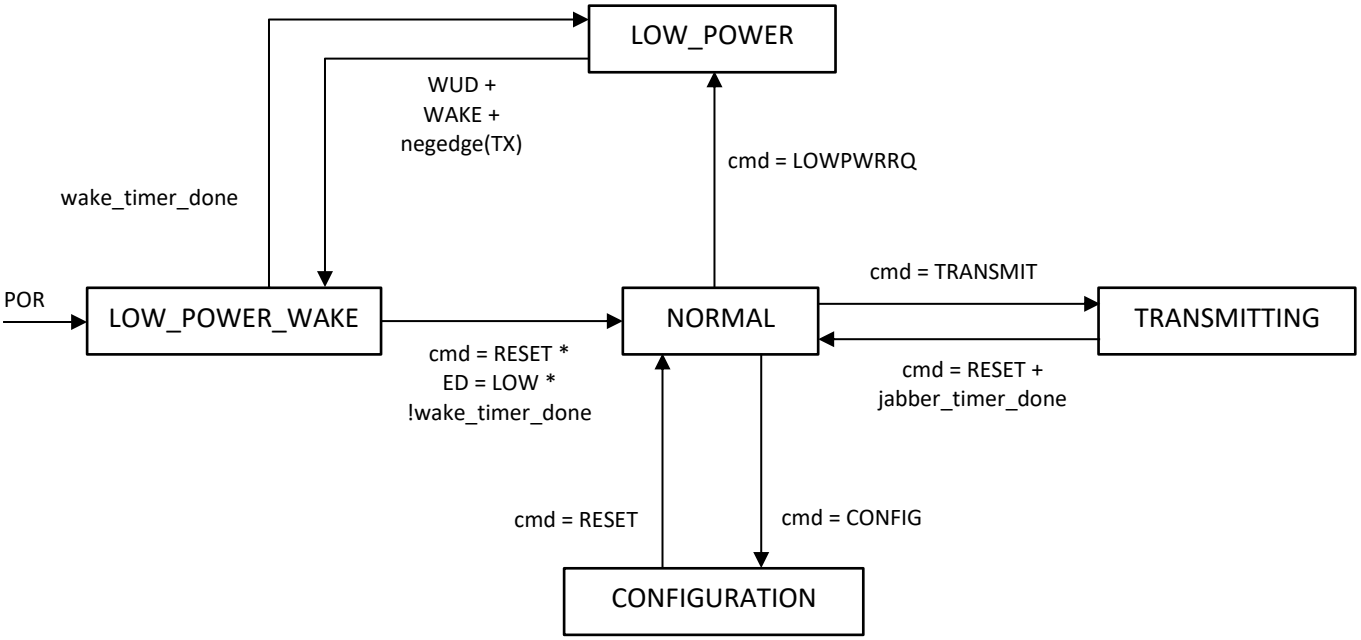


Figure 5: PMD Transceiver functional modes

4.2.1.1 Variables

cmd

Command conveyed by the host controller to the transceiver.
The encoding for the "cmd" variable is defined in 4.3.
Values: RESET, LOWPWRRQ, CONFIG, TRANSMIT, or NONE.

POR

Power-On-Reset[2].
This variable is initialized to TRUE when the transceiver is powered up. It is reset to FALSE upon entering NORMAL state.
Values: TRUE or FALSE

ED

The transceiver ED pin.
In the LOW_POWER_WAKE state, the transceiver shall drive the ED pin low as soon as it is ready to accept a RESET command.
Values: LOW or HIGH

TX

The transceiver TX pin (driven by the host).
Values: LOW or HIGH

[2] POR is defined as a transition from a state where no power was applied and no configuration was loaded into the device

WAKE

Optional, implementation-defined, external wake-up request event (e.g., asserting the WAKE pin in Figure 28 and Figure 29). If the external wake-up request functionality is not implemented, this variable is constantly set to FALSE.
Values: TRUE or FALSE

WUD

Wake-Up Detect, set to TRUE when the transceiver detects the WUT as explained in the OPEN Alliance TC10/TC14 documentation.
Values: TRUE or FALSE

4.2.1.2 Timers

jabber_timer

The jabber timer starts when entering the TRANSMITTING state and is reset each time the TX pin is pulsed low. The "jabber_timer_done" variable becomes TRUE when the jabber timer expires.
Duration: 8 µs
Tolerance: ± 6 µs

wake_timer

The wake timer is started when entering the LOW_POWER_WAKE state, and it is reset when leaving it. The "wake_timer_done" variable becomes TRUE when the wake timer expires.
Duration: 2 s
Tolerance: ± 1 s

4.2.1.3 Functions

negedge(x)

This function returns TRUE when the 'x' argument transitions from HIGH to LOW state. It returns FALSE otherwise.

4.3 Transmit Path

During NORMAL state, the host controller shall drive the TX pin high (de-asserted) until a command is conveyed to the transceiver. Besides, the value of the "cmd" variable defined in 4.2.1.1 is "NONE" until a command is initiated.

A command is initiated when the TX pin is asserted low after a minimum de-assertion time. The next subchapters provide normative encoding for all the supported commands. Note that all timings are related to the host PMA clock; therefore are subject to deviations due to jitter and I/O pins slope times.

4.3.1 RESET command encoding

The host controller conveys the RESET command by asserting the TX pin low for the length of one DME encoded "0" (80ns). A RESET command can be initiated at any time.

The host controller shall comply with the timings specified in Figure 6 and Table 1 when issuing a RESET command[3].

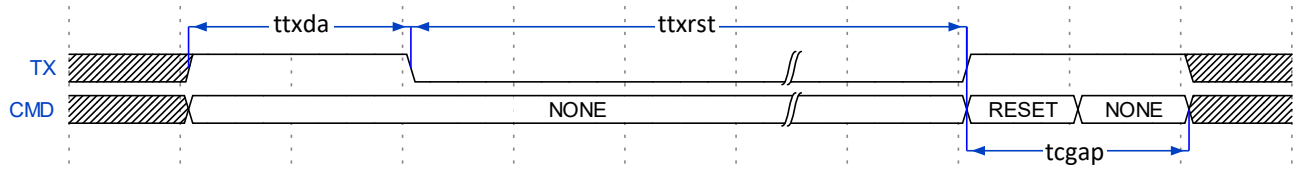


Figure 6: RESET command encoding

Table 1: RESET command timings

PARAM	MIN	NOM	MAX	UNIT	DESCRIPTION
ttxda	20	-	-	ns	TX pin de-assertion time before initiating a RESET
ttxrst	-	80	-	ns	TX pin assertion time to convey a valid RESET command
tcgap	20	-	-	ns	Inter-command gap time

NOTE: This is a normative requirement for the host controller. The transceiver can decode a RESET command for values of "ttxrst" different than the ones specified in Table 1, as long as other commands are not confused with a RESET.

4.3.2 TRANSMIT command encoding

The TRANSMIT command is conveyed by the host controller by a sequence of two low pulses of the TX pin, as shown in Figure 7. The TRANSMIT command can only be issued when the transceiver is in the NORMAL state.

The host controller shall comply with the timings specified in Figure 7 and Table 2 when issuing a TRANSMIT command.

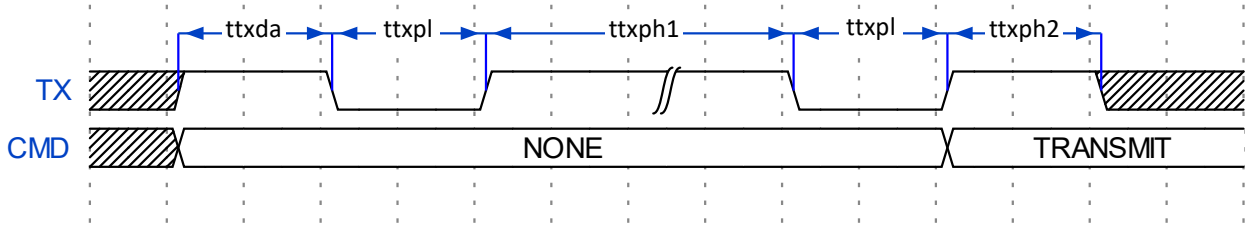


Figure 7: TRANSMIT command encoding

Note that the TRANSMITTING command shall take effect on the second positive edge of the TX pin.

[3] The CMD waveform in Figure 6 is informative to help in the understanding of the state diagram in Figure 5.

Table 2: TRANSMIT command timings

PARAM	MIN	NOM	MAX	UNIT	DESCRIPTION
ttxda	20	-	-	ns	TX de-assertion time before initiating a TRANSMIT
ttxpl	-	20	-	ns	TX low pulse duration
ttxph1	-	180	-	ns	TX high pulse duration
ttxph2	-	20	-	ns	TX gap before data or command

When the transceiver is in the TRANSMITTING state, the PMD shall drive a differential voltage at the line interface. Any subsequent falling edge of the TX pin shall invert the polarity of the differential voltage driven onto the line. When the TRANSMITTING state is left (either because of a RESET or because the jabber timer expires), the transceiver must stop driving the line interface within 40 ns to fulfill the requirement defined in clause 147.4.2 of the IEEE specifications [1].

The host controller shall comply with the timings specified in Figure 8 and Table 2 when transmitting the DME data. Timings for the DME are defined in clause 147.4.2 of [1].

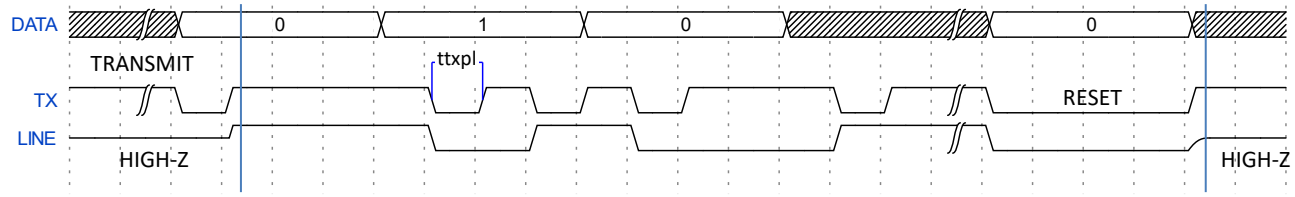


Figure 8: Transmitting DATA

In Figure 8, the duration of the high pulse on the TX pin is governed by the DME requirements. Therefore, the duration of the low TX pulse "ttxpl" is the only additional (normative) requirement here.

4.3.3 LOWPWRRQ command encoding

The host controller conveys the LOWPWRRQ command by asserting the TX pin low, as shown in Figure 9. The transceiver can only accept the LOWPWRRQ command during NORMAL state.

The host controller shall comply with the timings specified in Figure 9 and Table 3 when issuing a LOWPWRRQ command.

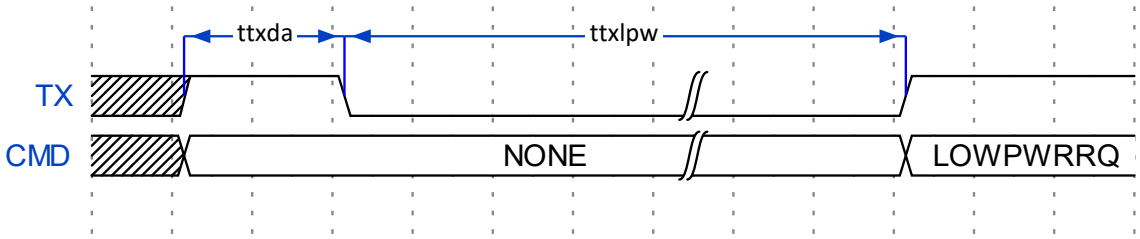


Figure 9: LOWPWRRQ command encoding

When receiving the LOWPWRRQ command, the transceiver shall provide a high logical level on the RX and ED pins within 1us from the positive edge of the TX pin that indicates the end of the command (end of ttxlpw).

The logical level, however, is not required if the host power is removed (e.g., when VIO in Figure 28 and Figure 29 is unpowered).

Table 3: LOWPWRRQ command timings

PARAM	MIN	TYP	MAX	UNIT	DESCRIPTION
ttxda	20	-	-	ns	TX de-assertion time before initiating a LOWPWRRQ command
ttxlpw	16	-	-	µs	TX low-assertion time to convey a valid LOWPWRRQ command

When the transceiver is in the LOW_POWER state, the line shall not be driven (high-Z).

The limit for the line impedance value when the driver is in high-Z state is defined by the MDI electrical specification in Clause 147.9.2 of [1].

4.3.4 CONFIG command encoding

The host controller conveys the CONFIG command by pulsing the TX pin low and asserting the TX pin low, as shown in Figure 10. The CONFIG command can only be issued when the transceiver is in the NORMAL state.

The host controller shall comply with the timings specified in Figure 10 and Table 4 when issuing a CONFIG command.

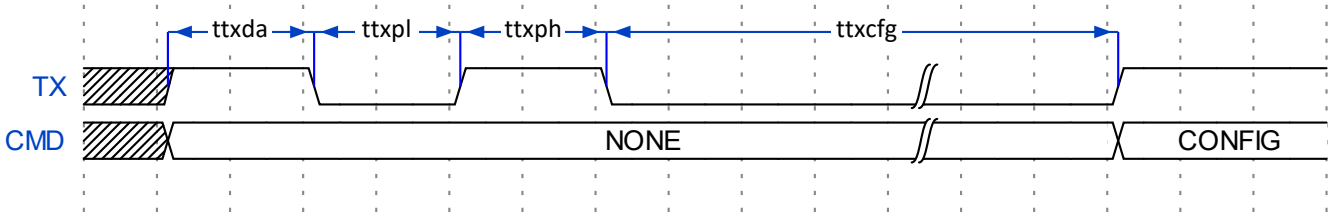


Figure 10: CONFIG command encoding

The CONFIG command shall take effect on the second positive edge of the TX pin.

Note that the CONFIG command differs from the LOWPWRRQ command only by an additional short TX pulse preceding the long pulse (see Figure 9 and Figure 10). A transceiver implementation must distinguish these cases by giving precedence to decoding the CONFIG command when a nominal 20ns low followed by 20ns high transition on the TX pin is detected.

Table 4: CONFIG command timings

PARAM	MIN	TYP	MAX	UNIT	DESCRIPTION
ttxda	20	-	-	ns	TX de-assertion time before initiating a CONFIG command
ttxpl	-	20	-	ns	TX low pulse duration
ttxph	-	20	-	ns	TX high pulse duration
ttxcfg	16	-	-	µs	TX assertion time to convey a valid CONFIG command

When the transceiver is in the CONFIGURATION state, no differential voltage shall be driven to the line (high-Z). The CONFIGURATION state can be exited using a RESET command.

4.4 Receive path

Two pins convey received data to the host controller: the receive pin (RX) and the energy detection pin (ED).

When the transceiver is in configuration mode, the RX pin becomes the MDC input of the management interface, while the ED pin becomes the associated bidirectional MDIO pin.

When the transceiver is in low power mode, the RX pin distinguishes between LOW_POWER (high) and LOW_POWER_WAKE (low) states, while the ED pin is used to report the transceiver status to the host.

When the transceiver operates in data mode (i.e., NORMAL or TRANSMITTING state), the following specifications apply.

4.4.1 RX pin specifications

The RX pin is the RZI-encoded output of a polarity-change detector centered around zero.

By default, the transceiver shall drive the RX pin high.

Anytime the differential voltage at the LINE pins changes polarity, the transceiver shall (in order):

1. drive the RX pin low for at least 12 ns
2. drive the RX pin high for at least 12 ns

During that time, If the polarity of the differential voltage at the LINE pins changes again, the transceiver shall convey a new low-pulse on the RX pin as soon as the previous sequence is completed, following the same rules above. Therefore, the low/high pulse sequence is atomic and uninterruptible.

Additionally, the transceiver must be ready to generate a new low pulse on the RX pin within the nominal DME baud rate (40 ns ± 100 ppm) to support the network bit rate and comply with the jitter specifications.

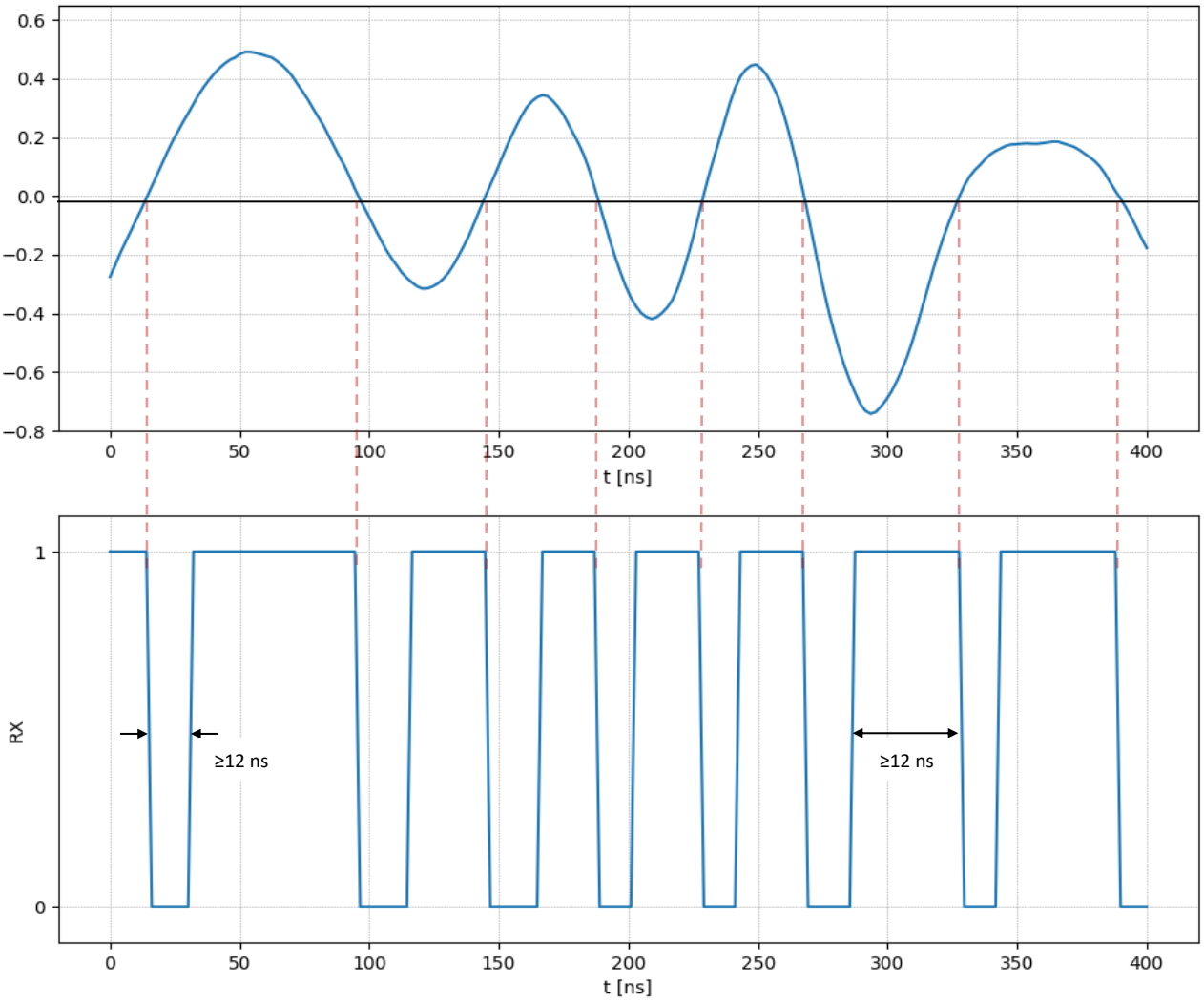


Figure 11: RX pin behavior with RZI encoding

4.4.2 ED pin specifications

When the transceiver operates in TRANSMITTING state, the ED pin reports collision detection information to the host according to the following rules:

- The ED pin shall be driven high upon entering the TRANSMITTING state
- If the transceiver detects a collision during the transmission, it shall drive the ED pin low for at least 30 ns ± 30% ns and up to the duration of the collision event[4].
- The method for detecting collisions is implementation-defined.

When the transceiver operates in NORMAL state (receiving), the following specifications apply.

The ED pin shall be asserted (logic-high) when the differential voltage present at the input of the LINE pins is greater than $V_{bh,}$ or it is less than V_{bl} for at least 30 ns ± 30%.

The ED pin shall be de-asserted (logic-low) when the differential voltage present at the input of the LINE pins is between V_{bl} and V_{bh} for at least 30 ns ± 30%.

In other words, the ED pin is the output of a window comparator with a deglitch filter of 30 ns (nominal). Figure 12 shows an example where the signal at point "A" dwells within V_{bh} and V_{bl} for more than 30ns.

[4] The ED pulse is measured from 50% to 50% of the I/O voltage level

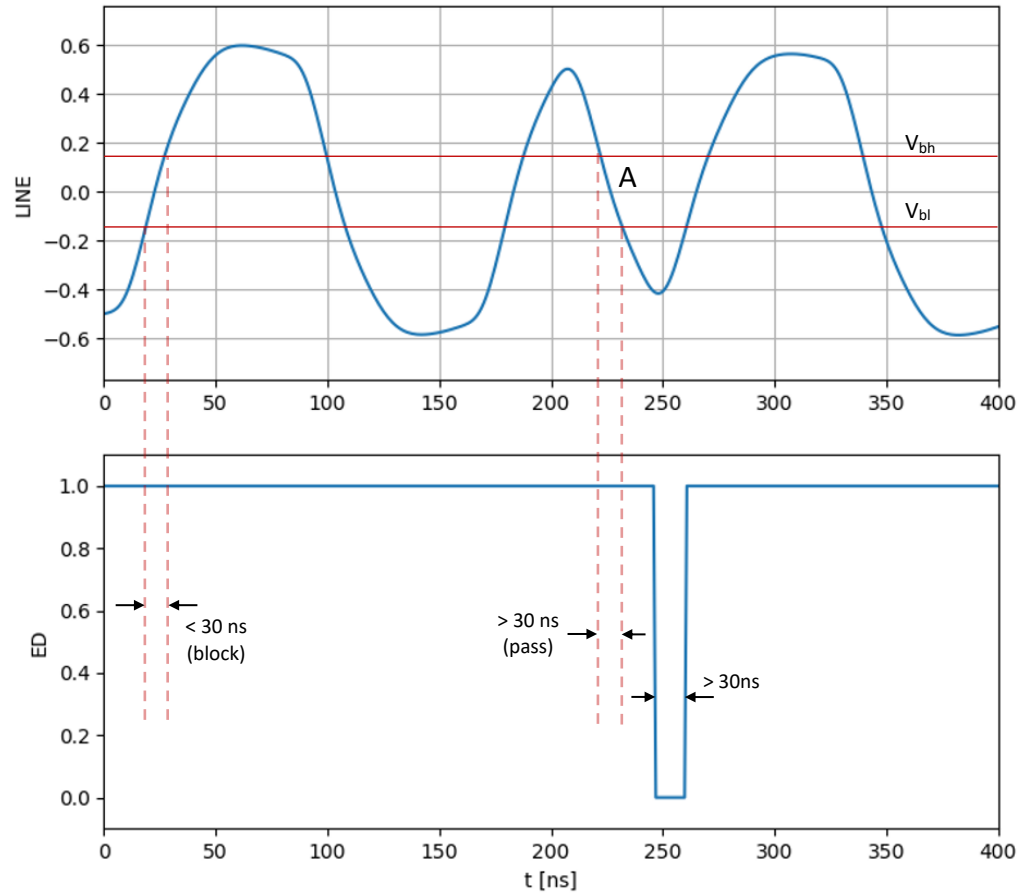


Figure 12: ED pin behavior

The values of V_{bh} and V_{bl} shall conform to Table 5.

Table 5: ED thresholds

PARAM	MIN	TYP	MAX	UNIT	DESCRIPTION
(V_{bh} – V_{bl})	270	300	330	mV	comparator windows amplitude
(V_{bh} + V_{bl})	-30	0	30	mV	comparator window offset

5 Functional Requirements

This chapter contains a set of additional requirements, recommendations, and clarifications to ensure proper operation of the 10BASE-T1S host controller and transceiver.

5.1 Boot

When the host controller is first powered up, or if for any reason it is rebooted, its first action towards the transceiver shall be a RESET command. This is required to achieve functional safety requirements and ensure the transceiver is always in a known state at all times.

Since the host controller may go through a reset while the transceiver is in low power mode, the host shall also check that the ED pin of the transceiver was low at the beginning of the RESET command. If not, the host controller shall keep sending RESET commands until the ED pin is low at the start of the command. The rate at which the host re-iterates the RESET commands is implementation-defined.

A weak pull-up resistor on the TX pin is recommended to avoid spurious transitions during power-up. Glitches could be interpreted as commands by the transceiver, so it is essential to prevent those from happening and disrupting the communication on the shared bus. The weak pull-up resistor also ensures that the line will not be driven if the TX pin is left floating. This may happen, for example, because of permanent failure of the host.

After a POR, the transceiver enters the LOW_POWER_WAKE state as described in 4.2.1, forcing the ED pin low as soon as it is ready to accept a RESET command.

5.2 Loop-back mode

To comply with the IEEE PMA specifications, the transceiver must support a loop-back mode.

To enter loop-back mode, the host performs the following operations:

1. enter CONFIGURATION mode (see chapter 6)
2. set the LOOPBACK bit in register CTRL0 (see 6.1.3.4)
3. leave CONFIGURATION mode using a RESET command (see Figure 5)

During loop-back mode, the TX pin shall work as normal, performing the functions described in chapter 4.2.

When the transceiver is in TRANSMITTING state and loop-back mode is enabled, the RX and ED pins shall function as follows:

- The ED pin is driven high
- The RX pin generates a low pulse of at least 12 ns at each falling edge of the TX pin (i.e., regardless of the signal at the line pins)

When the transceiver is in NORMAL state and loop-back mode is enabled, the RX and ED pins shall function as follows:

- The ED pin is driven low
- The RX pin is driven high

While in loop-back mode, the transceiver shall not drive a differential voltage at the line interface with low impedance, as if it was in NORMAL state.

5.3 Considerations of possible failures

Several kinds of failures may affect the communication on the shared media. These are related mainly to the status of the TX pin in case, for example, of an unexpected reset of the host controller or physical failure of the pins.

5.3.1 TX pin stuck at VCC

If the host controller resets unexpectedly (or fails permanently) so that the TX pin is driven high, no commands are conveyed to the transceiver. If the transceiver was in any state other than TRANSMITTING, then communication on the line is unaffected. Instead, if the transceiver was in the TRANSMITTING state, the line will be driven with low impedance for the duration of the jabber timer. During this short time, the effective BER on the bus may increase.

5.3.2 TX pin stuck at GND

If the host controller resets unexpectedly (or fails permanently) so that the TX pin is driven low, the transceiver may interpret this as a command. If the transceiver goes in any state other than TRANSMITTING, then the communication on the line is unaffected. Instead, if the transceiver switches to the TRANSMITTING state, the line will be driven with low impedance for the duration of the jabber timer. During this very short time, the effective BER of the bus may increase. If the host recovers from the failure, the initial RESET command will restore the normal operation of the transceiver.

5.3.3 TX pin left floating

If the host controller resets unexpectedly (or fails permanently) so that the TX pin is left in high impedance, the transceiver may interpret this as a command. To prevent this from happening, a weak pull-up resistor on the TX pin, either internal or external, is recommended (see also 5.1).

6 Management Interface

Configuration mode allows the host controller to perform basic management operations on the transceiver, such as identification, diagnostic, and vendor-defined functions.

Configuration mode can only be enabled using a CONFIG command as described in 4.2.1 and 4.3.4. Configuration mode can only be disabled using a RESET command as described in 4.2.1 and 4.3.1 or by a power cycle.

During configuration mode, the transceiver does not drive any differential voltage at the line interface with low impedance, regardless of any activity on the TX pin. The RX and ED pins are used respectively as the MDC clock input and the MDIO data input/output of an MII management interface (MIIM).

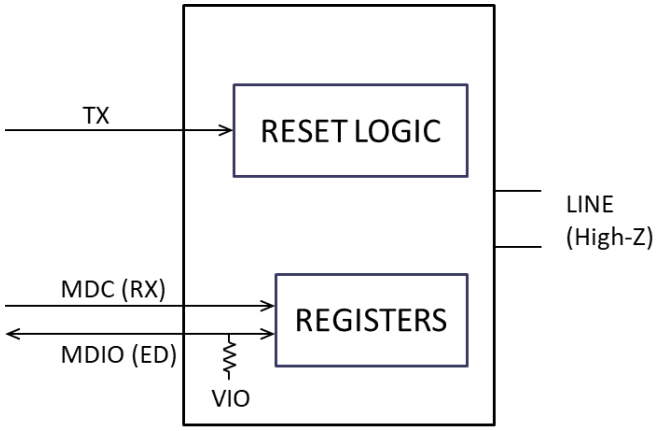


Figure 13: Transceiver pins function during CONFIGURATION mode

The MIIM interface specification shall comply with Clause 22.2.4.5 of [2]. The MIIM timings shall comply with Clause 22.3.4 of [2], although the transceiver can optionally support higher MDC clock rates.

The transceiver shall always respond to the MIIM address (PHYAD) 0x01.

The transceiver should include an internal weak pull-up resistor on the ED pin while operating in configuration mode.

The management registers definition for the transceiver shall comply with chapter 6.1.

As a general rule, reads to undefined, unimplemented, and reserved addresses shall result in reading all zeroes. Writes to such addresses shall have no effect. The same applies to individual bits in defined registers that are not assigned a function.

6.1 Registers Map

The map of the transceiver registers is defined in Table 6. The data width of the MIIM registers is 16.

Table 6: MIIM Registers map

Address	Name	Description
0x00	MIIMCTL	MIIM Control Register
0x01	-	Reserved (Std. MIIM)
0x02-0x03	PHYID	MIIM PHY Identification Registers
0x04-0x0F	-	Reserved (Std. MIIM)
0x10	PMDCTL	PMD Control Register
0x11-0x1F	-	Vendor Defined Space

6.1.1 MIIMCTL – MIIM Control Register

The assignment of bits in the control register #0 is shown in Table 7.

Table 7: MIIMCTL register bits definition

Bit(s)	Name	Description	R/W [a]	Default/Value
15	RESET	Reset	RW	0
14	LOOPBACK	Loop-back mode enable	RW	0
13:0	-	Reserved	RO	0x0000

NOTE

[a] RO = read-only, RW = read-write, SC = self-clearing

6.1.1.1 RESET

When the transceiver leaves the CONFIGURATION state, if this bit is set to '1', the transceiver shall reset all registers to their default values and return to the LOW_POWER_WAKE state, as if a POR condition occurred.

6.1.1.2 LOOPBACK

When the LOOPBACK bit is set, the transceiver operates in loop-back mode upon entering the TRANSMITTING state, as explained in chapter 5.2. When cleared (default), the transceiver operates in normal data mode.

The value of this bit shall have no effect on the PMD transceiver when the TPEN bit in the PMDCTL register is set to 1.

6.1.2 PHYID – PHY identification registers (0x02-0x03)

The combination of the two registers at address 0x02 and 0x03 constitute the 32-bit wide PHYID register. The PHYID register is read-only and shall follow the same definition as the homonymous register in clause 22.2.4.3.1 of [2].

6.1.3 PMDCTL – PMD control register

The assignment of bits in the PMD control register is shown in Table 8.

Table 8: CTRL0 register bits definition

Bit(s)	Name	Description	R/W [a]	Default/Value
15	FDCAP	Full-Duplex capability	RO	-
14	HDCAP	Half-Duplex capability	RO	-
13:2	-	Reserved	RO	0x0000
1	TPREFN	TPD measured/reference node select	RW	0
0	TPEN	Topology Discovery Enable	RW	0

NOTE

[a] RO = read-only, RW = read-write, SC = self-clearing

6.1.3.1 FDCAP

When FDCAP is set, the PMD transceiver supports full-duplex mode of operation. When cleared, full-duplex mode is not supported. A valid PMD transceiver implementation shall set at least one of the FDCAP and HDCAP bits.

6.1.3.2 HDCAP

When HDCAP is set, the PMD transceiver supports half-duplex mode of operation. When cleared, half-duplex mode is not supported. A valid PMD transceiver implementation shall set at least one of the FDCAP and HDCAP bits.

6.1.3.3 TPREFN

The TPREFN bit sets the topology discovery internal scrambler function to "measured" or "reference" node, as per the following table:

0: Local node is the measured node
1: Local node is the reference node

6.1.3.4 TPEN

When TPEN is set, the transceiver operates in "Topology Discovery Mode" upon entering the TRANSMITTING state, as explained in chapter 8. When cleared (default), the transceiver operates in normal data mode.

7 Low-Power Mode

Low power mode allows the transceiver to support the sleep/wakeup requirements described in the OPEN Alliance TC10/TC14 JWG specifications.

Low power mode can be enabled only using a LOWPWRRQ command as described in 4.2.1 and 4.3.3.

The transceiver shall not drive the line with low impedance during low power mode, which includes both the LOW_POWER and LOW_POWER_WAKE states.

To support the remote wakeup feature with partial networking, the RX and ED pins provide a status indication to the host controller according to the following rules:

- When the LOW_POWER state is entered, both the RX and the ED pins shall be driven high or high-impedance with a weak pull-up.
- During LOW_POWER state, if the wakeup tone (WUT) signal is present on the line, the transceiver transitions to LOW_POWER_WAKE. The method for detecting the WUT is implementation-defined.
- During LOW_POWER state, if the host asserts the TX pin low, the transceiver transitions to LOW_POWER_WAKE state.
- Entering LOW_POWER_WAKE state, the transceiver shall drive the RX pin low. In typical applications, this enables the main power supply.
- During LOW_POWER_WAKE state, as soon as the transceiver is ready to support a change to NORMAL state, the transceiver shall drive the ED pin low. The host uses this information to stop sending RESET commands (see below).
- During LOW_POWER_WAKE state, if the wake_timer expires before the transceiver receives a complete RESET command, the transceiver shall drive the ED and RX pins high while transitioning to LOW_POWER state.

When the host controller awakens, it shall perform a RESET command as the first action toward the transceiver to restore normal operation. If the ED pin was high at the start of the RESET, the host must assume that the transceiver was not ready to accept the command. Therefore it shall keep sending RESET commands until the ED pin is low at the start of the command. The rate at which the host controller re-iterates the RESET commands is implementation-defined.

7.1 Wake-up Timings

The transceiver shall comply with the timings reported in Figure 14, Figure 15, and Table 9 when a remote or local wake-up condition is detected.

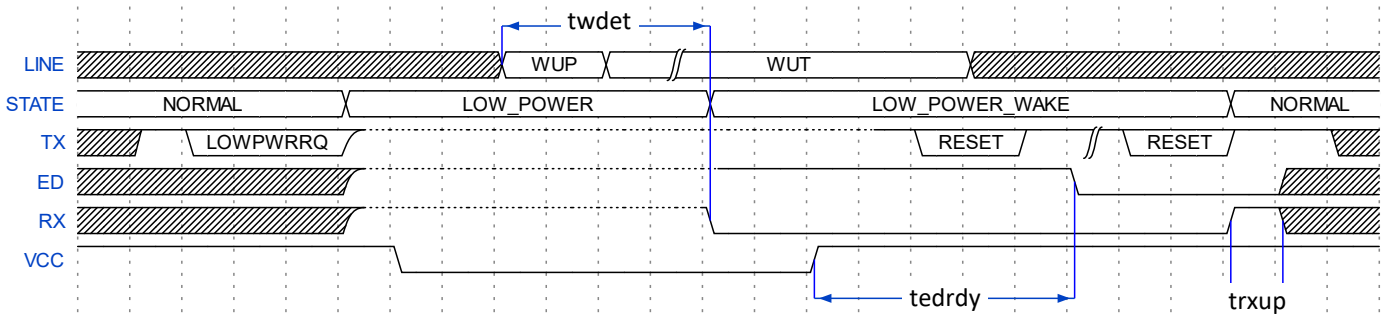


Figure 14: Remote wake-up

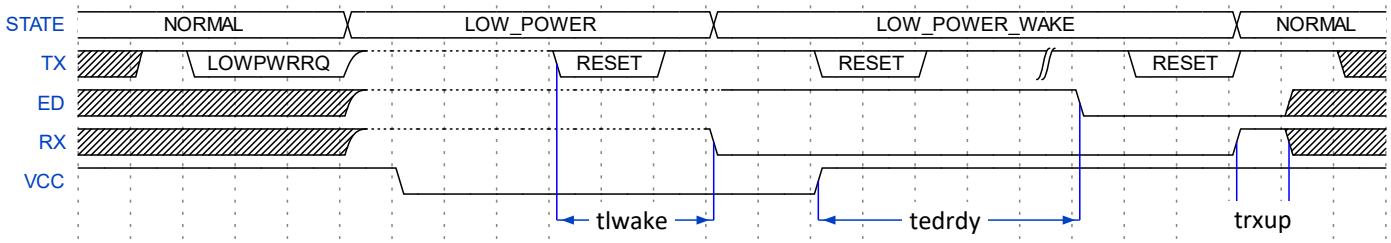


Figure 15: Local wake-up

Table 9: wake-up timings

PARAM	MIN	MAX	UNIT	DESCRIPTION
twdet	-	35	µs	Remote wake-up detection time[5]
tedrdy	-	1	ms	Transceiver initialization time after wake-up
trxup	12	-	ns	Minimum RX high time after initialization
tlwake	-	15	µs	Local wake-up detection time

[5] Measured from the first transition of the WUP on the line

8 Support for Topology Discovery

A transceiver implementation shall support the topology discovery feature described in the OPEN Alliance TC14 Topology Discovery specifications. This chapter defines specific requirements for a PMD Transceiver implementation to support the topology discovery feature.

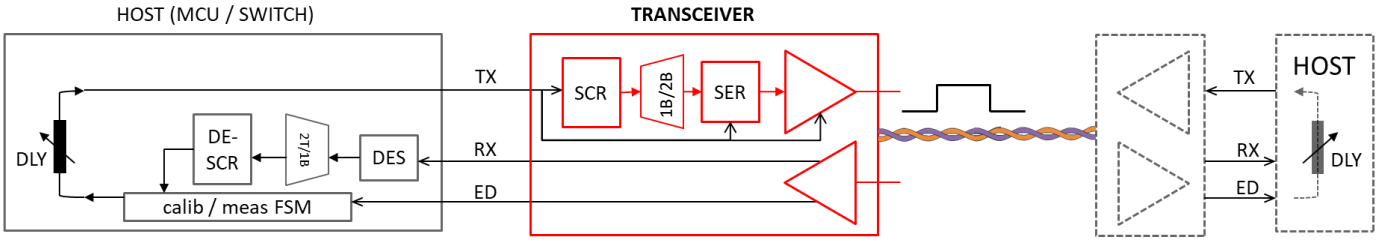


Figure 16: Topology Discovery Support Overview

When the host enters topology discovery mode, it also configures the transceiver for topology discovery operation, following these steps:

1. enter CONFIGURATION mode (see chapter 6)
2. set the TPEN bit and configure the TPREFN bit in register CTRL0 (see 6.1.3.4 and 6.1.3.3)
3. leave CONFIGURATION mode using a RESET command (see Figure 5)

In topology discovery mode, the RX pin shall indicate the polarity of the differential signal at the line pins, using an NRZ coding instead of the default RZI coding. That is, the transceiver shall drive the RX pin high if the differential line voltage is greater than 0. Otherwise, it shall drive the RX pin low.

The ED pin works as specified in 4.4.2, except that no filtering shall be applied.

NOTE: this means that the ED pin is the output of an unfiltered window comparator with V_{bh} and V_{bl} defined by Table 5 (see also 4.4.2).

When the TRANSMITTING state is entered, however, the TX pin function is changed to match the features depicted in Figure 16:

- On the falling edge of the TX pin, the transceiver shall start driving the line with low impedance and polarity set after the serializer output, as defined in the Topology Discovery specifications.
- The duration of the pulse driving the line is timed by the PMD transceiver and not by the duration of the TX pin low-pulse. The actual width of the pulse generated at the line interface shall match the TD_pulse duration reported in the Topology Discovery specifications.
- After 20 ns to 30 ns (nominal time) from the initial TX pin falling edge, the host shall drive the TX pin at a logical high level. This is how the host produces a single TD_pulse, hence the PMD transceiver must not confuse the TX pulse with a RESET command.
- At the end of the pulse at the line interface, the scrambler, the 1B/2B encoder, and the serializer blocks shall be updated to prepare for the next TD_pulse, as specified in the Topology Discovery specifications.

The method to produce a TD_pulse of the required length is implementation-defined.

Note that the transceiver must still decode RESET commands conveyed on the TX pin as specified in 4.3.1 to exit the TRANSMITTING state and return to NORMAL state.

9 Electrical Characteristics

The electrical characteristic of the LINE pins of the transceiver shall comply with the ones specified in this chapter.

All defined values shall be supported by implementations within their specified supply tolerance range.

9.1 DC characteristics

9.1.1 Differential line voltage amplitude

The maximum peak-to-peak differential voltage (V_{tx}) shall be the one specified in Clause 147.5.4.1 (Transmitter output voltage) of [1].

9.1.2 Interface pins voltage

The reference voltage for the TX, RX, and ED pins of the transceiver should conform to the appropriate JEDEC digital interface specification.

9.2 AC Characteristics

The AC characteristics test conditions are defined by the circuit in Figure 17.

Note: V_{LINE} is the differential voltage between the LINE+ and LINE- pins

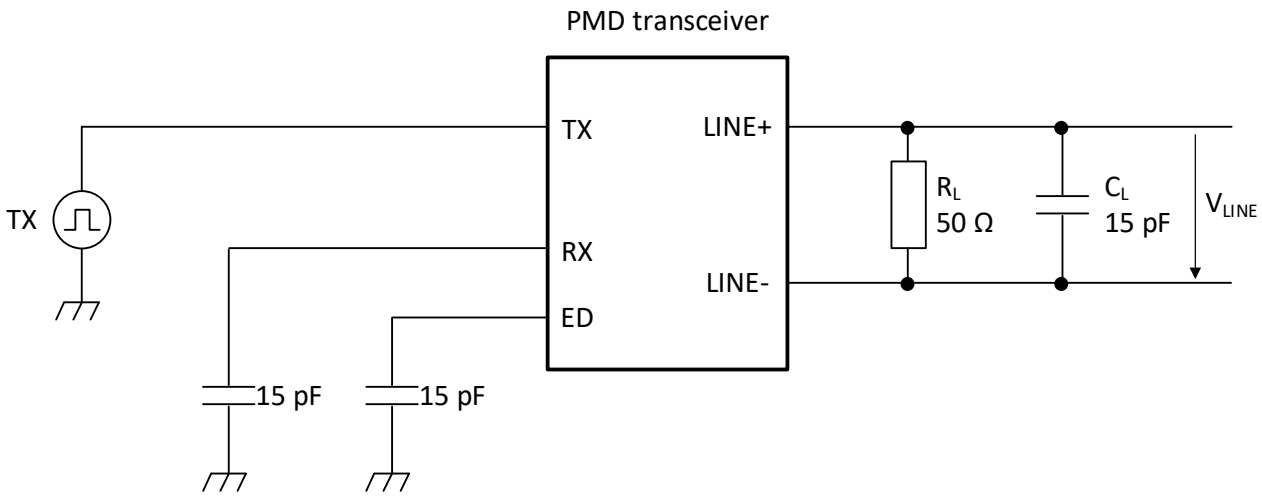


Figure 17: Timing test circuit

9.2.1 TX pin rise/fall timings

When driven by the host controller, the rise time of the TX pin, regardless of the reference voltage, shall be less than 6 ns.

When driven by the host controller, the fall time of the TX pin, regardless of the reference voltage, shall be less than 6 ns.

On the transceiver IC it is recommended to implement a glitch filter of less than 10ns over the TX pin assertion to protect against spurious spikes which may occur, for example, because of imperfections of the PCB layout.

9.2.2 RX and ED pins rise/fall timings

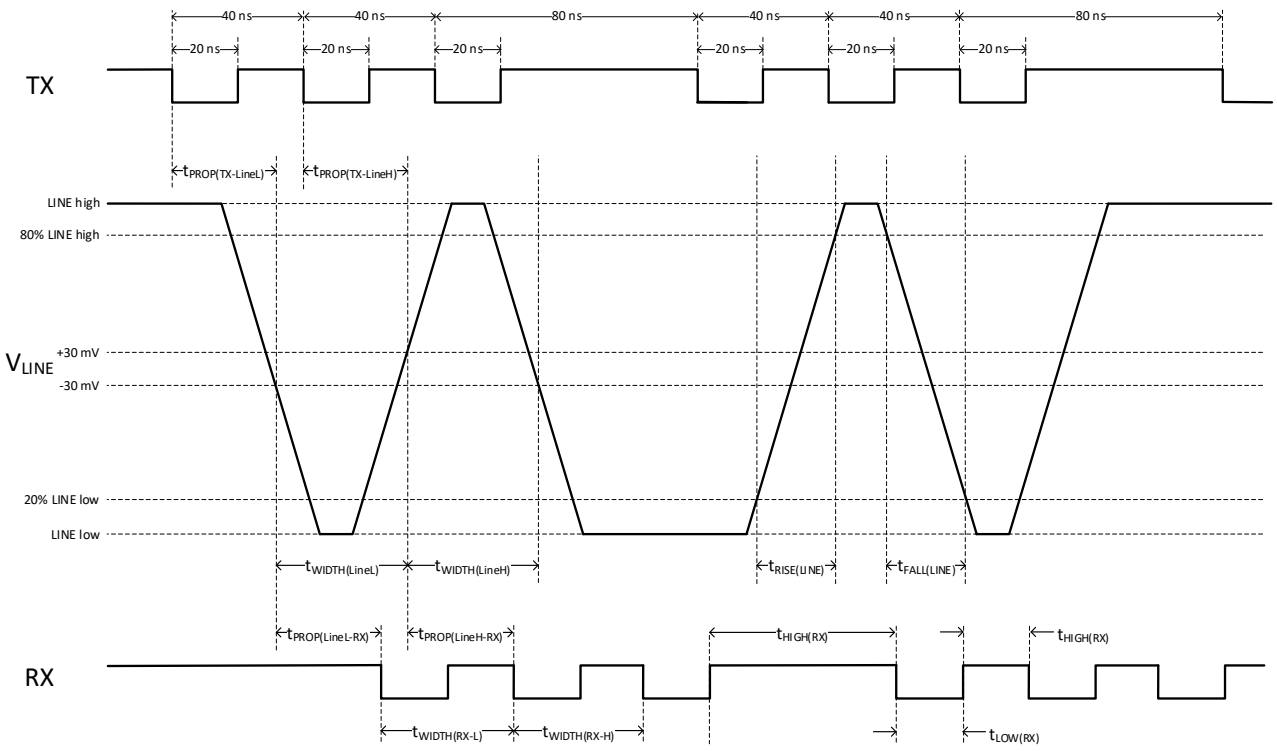
When driven by the transceiver, both the rise and fall times of the RX and ED pins, regardless of the reference voltage, shall be less than 6 ns.

9.2.3 Timings in CONFIGURATION state

The total time between the CONFIG command issued[6] and the transceiver entering the configuration mode shall be less than 80 ns. Note that this implies that the transceiver must set the RX and ED pins as inputs (MDC, MDIO) within that time to avoid contentions.

When the transceiver is in CONFIGURATION state and the host issues a RESET command, the transceiver shall set the RX and ED pins back to outputs within 80 ns after the TX pin is asserted high.

9.2.4 Timings in NORMAL and TRANSMITTING state



[6] Measured form the last rising edge of the TX pin

Figure 18: Timings in TRANSMITTING or NORMAL state

Parameter	Notation	Min [ns]	Max [ns]	Remark
Transmitter specification in TRANSMITTING state				
Propagation delay from TX falling edge to LINE high level	$t_{PROP(TX\text{-}LineH)}$	-	50	Measured from falling edge crossing 50% level on TX to a LINE rising voltage crossing of +30 mV (see Figure 18)
Propagation delay from TX falling edge to LINE low level	$t_{PROP(TX\text{-}LineL)}$	-	50	Measured from falling edge crossing 50% level on TX to a LINE falling voltage crossing of -30 mV (see Figure 18)
Width LINE low level	$t_{WIDTH(LineL)}$	36	44	Measured from LINE falling voltage crossing of -30 mV to LINE rising voltage crossing of +30 mV during a DME 1 symbol (see Figure 18)
Width LINE high level	$t_{WIDTH(LineH)}$	36	44	Measured from LINE rising voltage crossing of +30 mV to LINE falling voltage crossing of -30 mV during a DME 1 symbol (see Figure 18)
Receiver specification in NORMAL and TRANSMITTING state				
Propagation delay from LINE low level to RX	$t_{PROP(LineL\text{-}RX)}$	-	80	Measured from a LINE falling voltage crossing -30 mV to falling edge crossing 50% level on RX (see Figure 18)
Propagation delay from LINE low level to RX	$t_{PROP(LineH\text{-}RX)}$	-	80	Measured from a LINE rising voltage crossing +30 mV to falling edge crossing 50% level on RX (see Figure 18)
Low time RX	$t_{LOW(RX)}$	12	-	Low time RX (see Figure 18)
High time RX	$t_{HIGH(RX)}$	12	-	High time RX (see Figure 18)
Receiver timing symmetry LINE low level	t_{REC_LOW}	-4	+4	Calculated as $t_{REC\_LOW} = t_{WIDTH(RX\text{-}L)} - t_{WIDTH(LineL)}$ (see Figure 18) during a DME 1 symbol
Receiver timing symmetry LINE high level	t_{REC_HIGH}	-4	+4	Calculated as $t_{REC\_HIGH} = t_{WIDTH(RX\text{-}H)} - t_{WIDTH(LineH)}$ (see Figure 18) during a DME 1 symbol

Table 10 Timing in NORMAL and TRANSMIT state

9.2.5 Timing from NORMAL to TRANSMITTING state

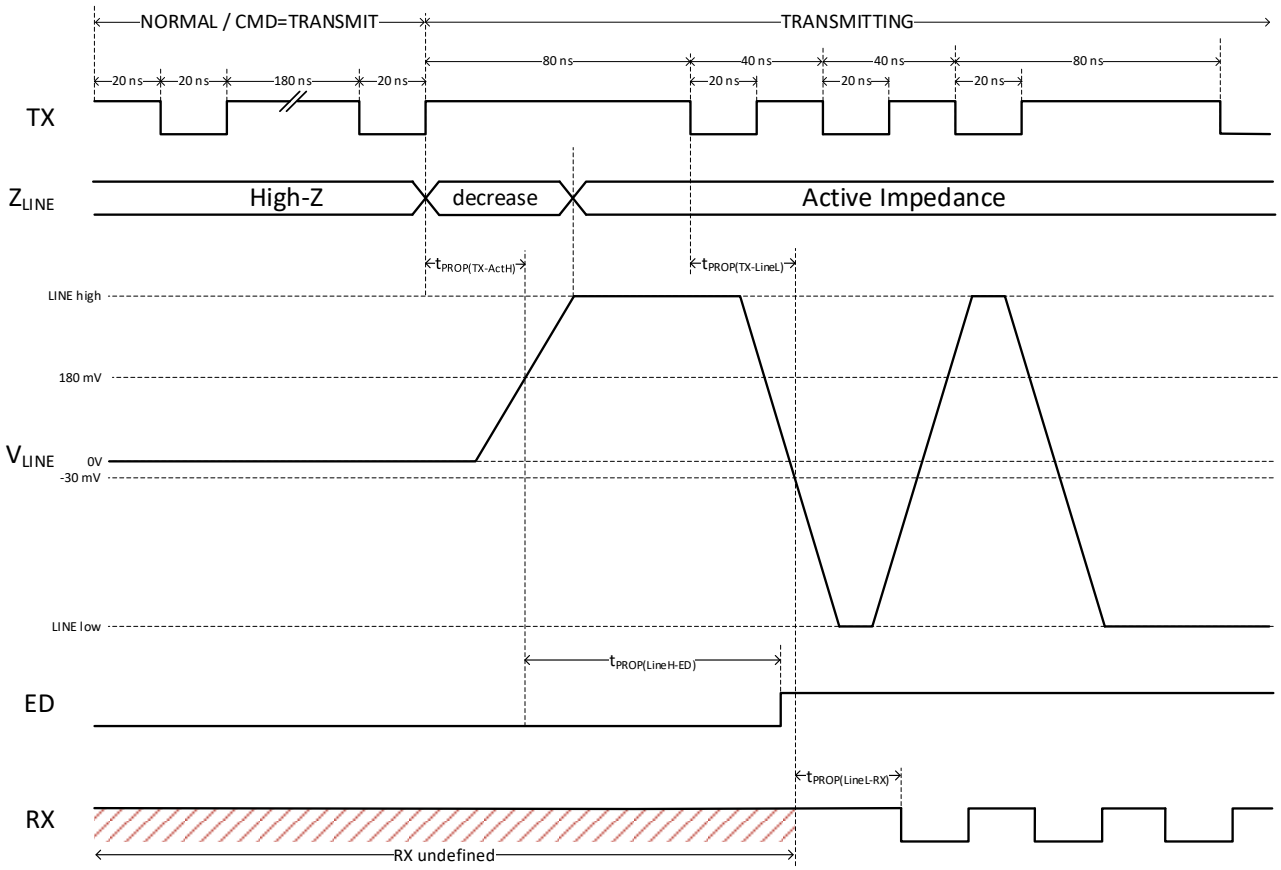


Figure 19: Timing from NORMAL to TRANSMITTING state LINE high level starting with DME 0 symbol

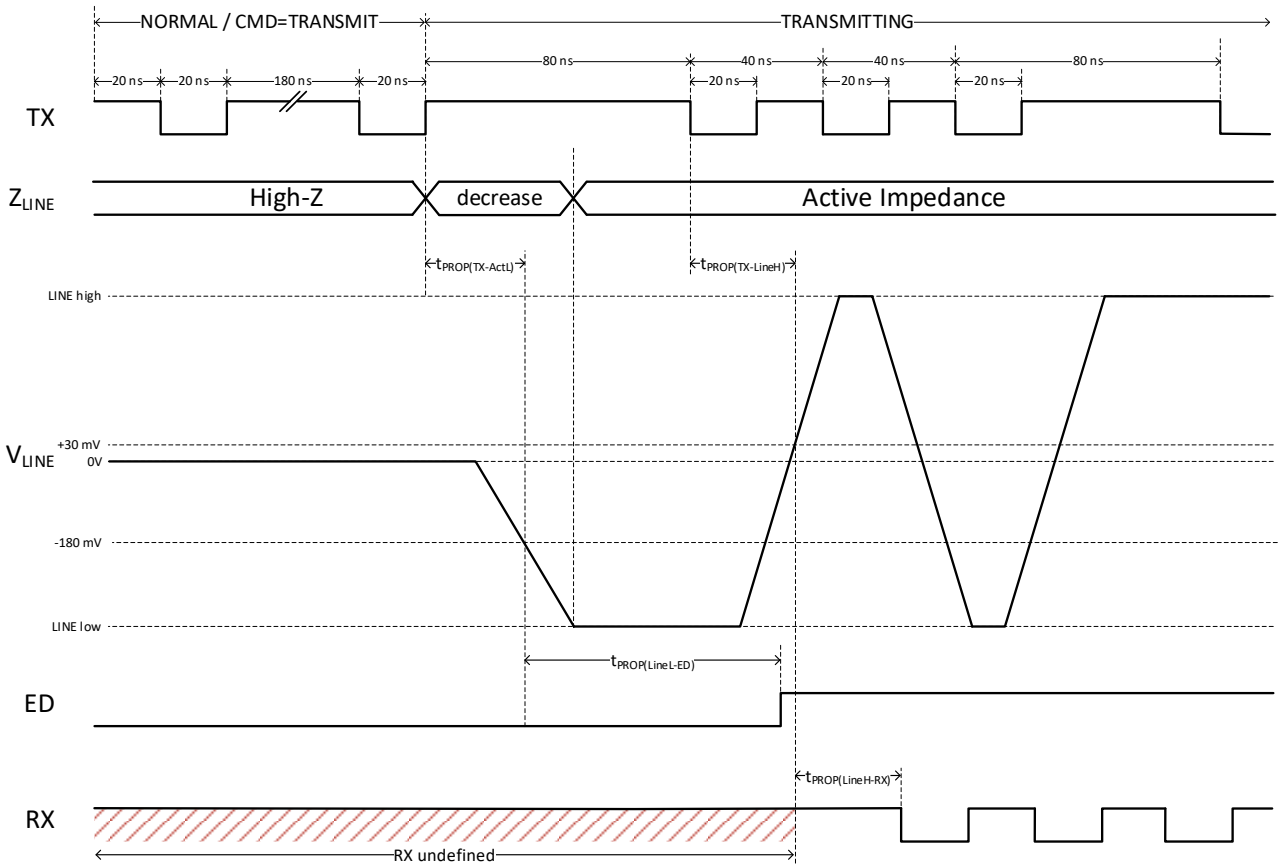


Figure 20: Timing from NORMAL to TRANSMITTING state LINE low level starting with DME 0 symbol

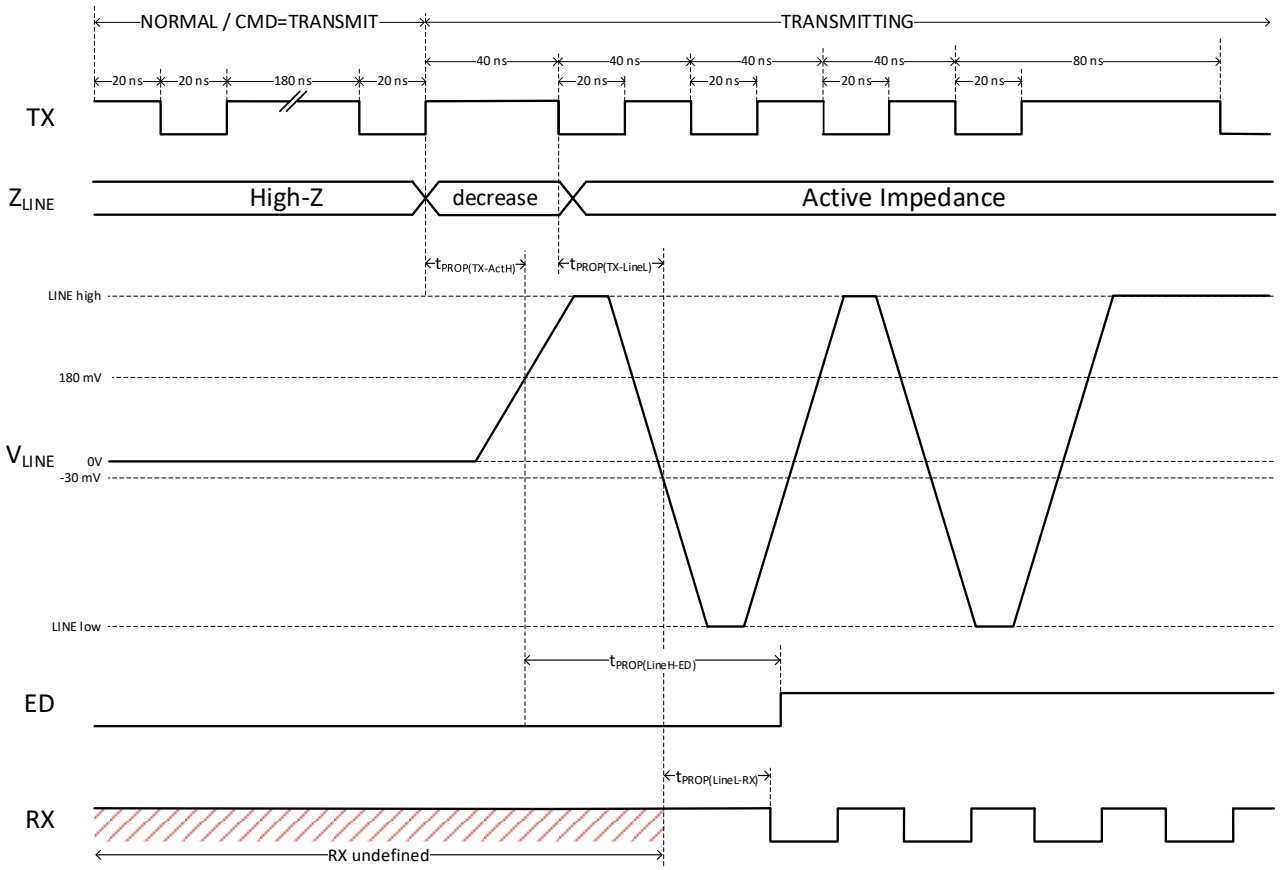


Figure 21: Timing from NORMAL to TRANSMITTING state LINE high level starting with DME 1 symbol

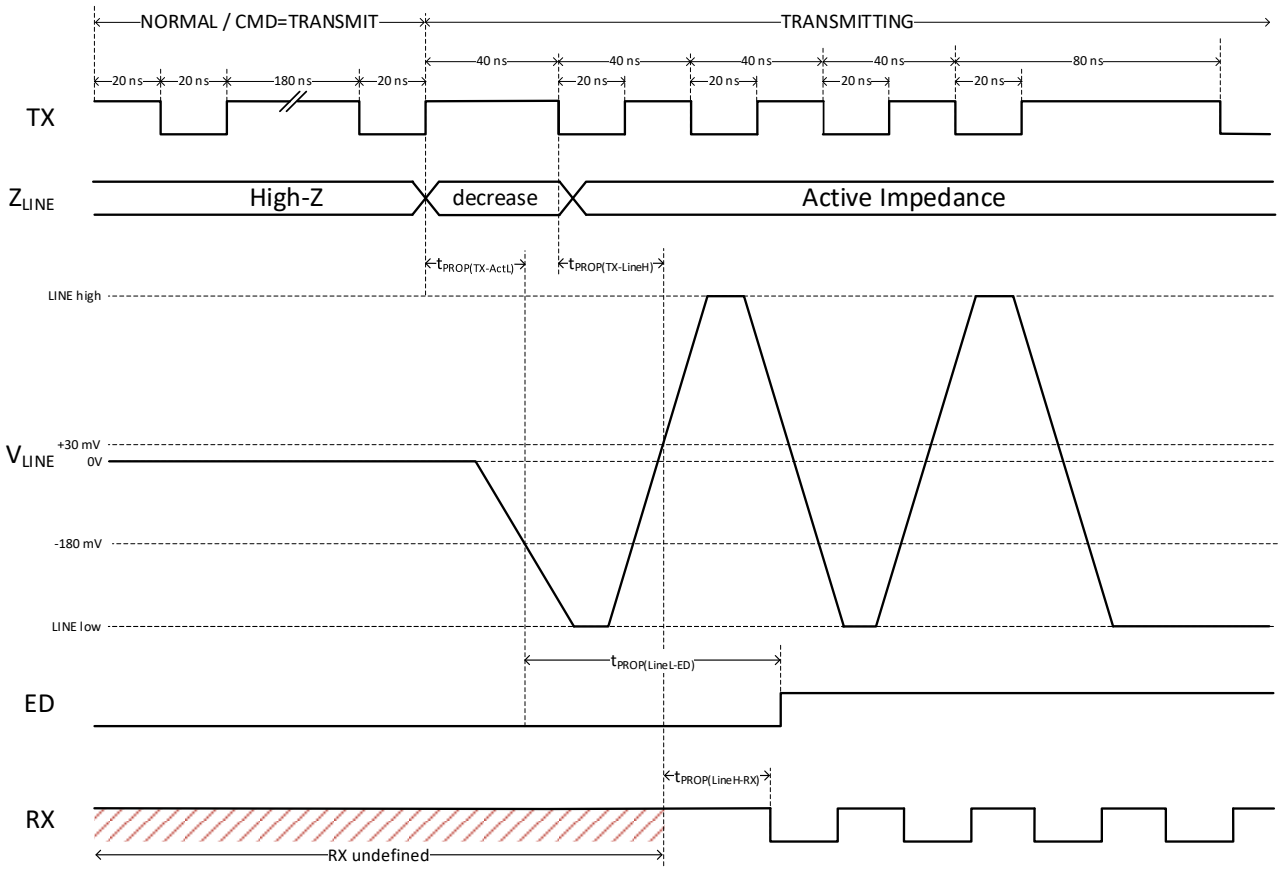


Figure 22: Timing from NORMAL to TRANSMITTING state LINE low level starting with DME 1 symbol

Parameter	Notation	Min [ns]	Max [ns]	Remark
Transmitter specification from NORMAL to TRANSMITTING state				
Propagation delay from TX to active LINE high [a]	$t_{PROP(TX-ActH)}$	-	50	Measured from rising edge crossing 50% level on TX at the end of TRANSMIT command to a LINE rising voltage crossing of +180 mV starting from High-Z (see Figure 19)
Propagation delay from TX to active LINE low [a]	$t_{PROP(TX-ActL)}$	-	50	Measured from rising edge crossing 50% level on TX at the end of TRANSMIT command to a LINE falling voltage crossing of -180 mV starting from High-Z (see Figure 20)
Difference between LINE active and LINE low-level propagation delay [b, d]	$t_{PROP(ActH,LineL)}$	-	30	Calculated as $t_{PROP(TX-ActH)}$ - $t_{PROP(TX-LineL)}$ (see Figure 19 and Table 10)
Difference between LINE active and LINE high-level propagation delay [b, d]	$t_{PROP(ActL,LineH)}$	-	30	Calculated as $t_{PROP(TX-ActL)}$ - $t_{PROP(TX-LineH)}$ (see Figure 20 and Table 10)

ED specification from NORMAL to TRANSMITTING state				
Propagation delay from LINE high level to ED high [a]	$t_{PROP(LineH-ED)}$	-	130	Measured from a LINE rising voltage crossing +180 mV to rising edge crossing 50% level on ED
Propagation delay from LINE low level to ED high [a]	$t_{PROP(LineL-ED)}$	-	130	Measured from a LINE falling voltage crossing -180 mV to rising edge crossing 50% level on ED
Difference between LINE high to ED propagation delay and LINE low level to RX propagation delay [c,d]	$t_{PROP(ED,LineL-RX)}$	-	50	Calculated as $t_{PROP(LineH-ED)}$ - $t_{PROP(LineL-RX)}$ (see Figure 19 and Table 10)
Difference between LINE low to ED propagation delay and LINE high level to RX propagation delay [c,d]	$t_{PROP(ED,LineH-RX)}$	-	50	Calculated as $t_{PROP(LineL-ED)}$ - $t_{PROP(LineH-RX)}$ (see Figure 20 and Table 10)

Table 11 Timing from NORMAL to TRANSMITTING state

[a] The first transition from high-Z to active can be either driving the LINE high or the LINE low. If an implementation drives the line interface in only one direction, the opposite direction specification does not need to be tested.

[b] The difference between TX-to-LINE active propagation delay and TX-to-LINE high/LINE low propagation delay is required to guarantee the detection of the first full transition on the LINE by the digital PHY in case of a DME 0 symbol.

[c] The difference between LINE-to-ED propagation delay and LINE-to-RX propagation delay is required to guarantee the detection of the first full transition on the LINE by the digital PHY in case of a DME 0 symbol.

[d] If the first transmitted symbol is a DME 1 symbol, the transceiver will not be able to guarantee proper signaling on the ED for the HOST to decode the data edge on the LINE reliably.

9.2.6 Timing from TRANSMITTING to NORMAL state

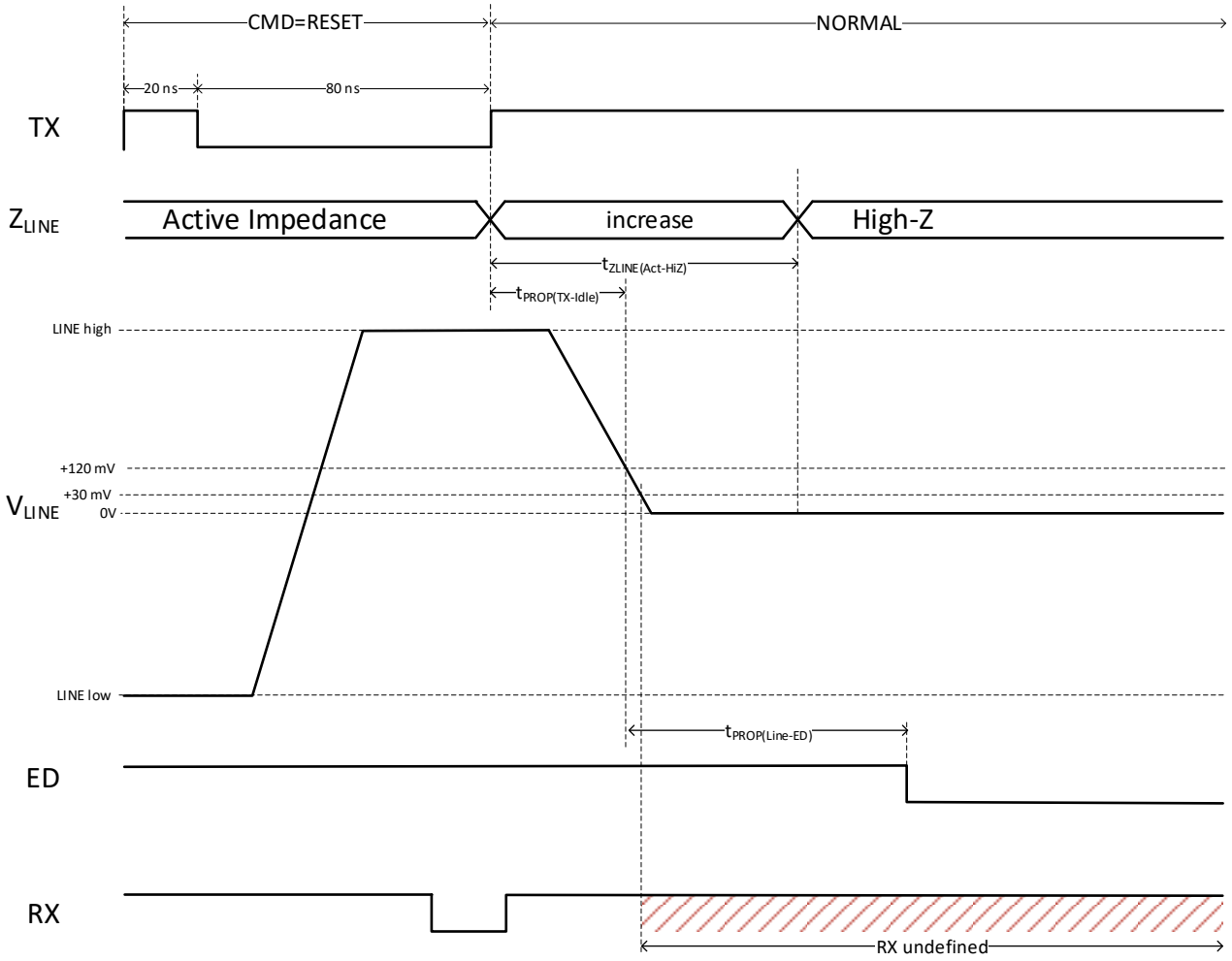


Figure 23: Timing from TRANSMITTING LINE high level to NORMAL state

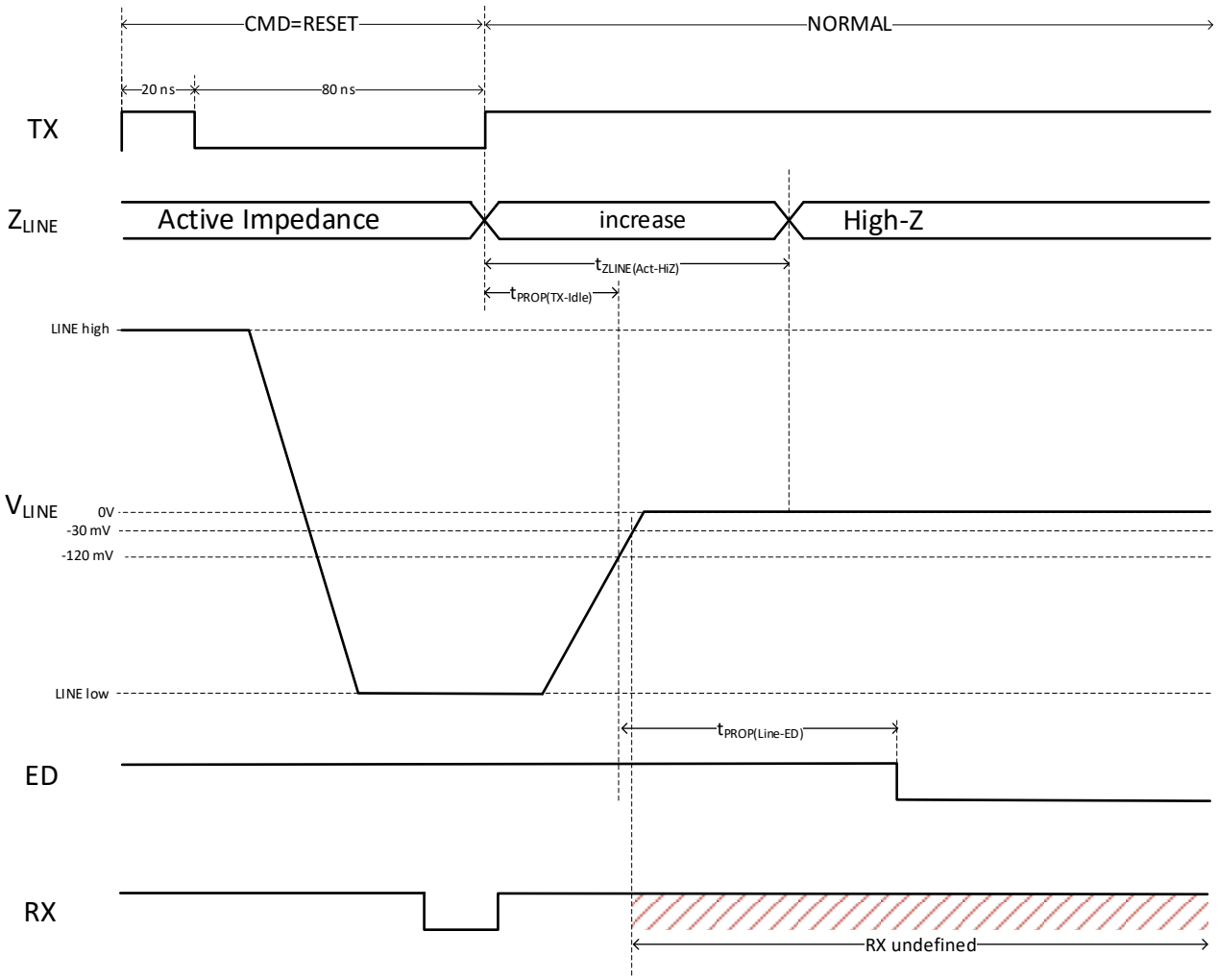


Figure 24: Timing from TRANSMITTING LINE low level to NORMAL state

Parameter	Notation	Min [ns]	Max [ns]	Remark
Transmitter specification from TRANSMITTING to NORMAL state				
Propagation delay from TX to LINE zero level[a]	$t_{PROP(TX-Idle)}$	-	65	Measured from rising edge crossing 50% level on TX at the end of RESET command to a LINE falling voltage crossing of +120 mV or a LINE rising voltage crossing of -120 mV (see Figure 23 and Figure 24)
Delay from TX to driving LINE with high impedance[a]	$t_{ZLINE(Act-HiZ)}$	-	110	Measured from rising edge crossing 50% level on TX at the end of RESET command to driving the LINE with high impedance (> minimum specified input impedance) (see Figure 23 and Figure 24)
ED specification from TRANSMITTING to NORMAL state				
Propagation delay from LINE zero level to ED high[a]	$t_{PROP(Line-ED)}$	-	130	Measured from a LINE falling voltage crossing of +120 mV or a LINE rising voltage crossing of -120 mV to falling edge crossing 50% level on ED (see Figure 23 and Figure 24)

Table 12 Timing from TRANSMITTING to NORMAL state

[a] The last transition from active to high-z can be either driving V_{LINE} from LINE high or LINE low.

9.2.7 Timing of ED in TRANSMITTING state

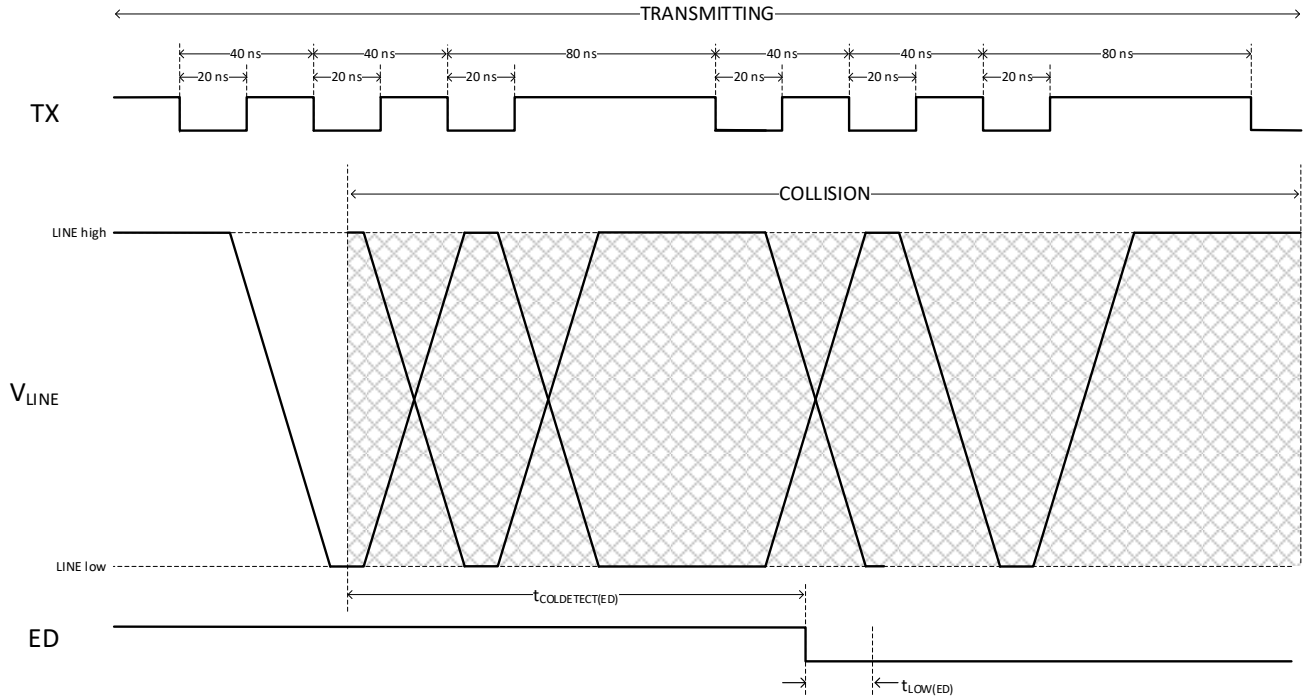


Figure 25: Timing of collision detect in TRANSMITTING state

Parameter	Notation	Min [ns]	Max [ns]	Remark
ED specification in TRANSMITTING state				
Collision detect delay time	$t_{COLDETECT(ED)}$	-	4500	Measured from the start of the corrupted transmitted signal at the LINE (see Figure 25)
Low time ED	$t_{LOW(ED)}$	21	-	Minimum low time ED after collision detection (see Figure 25)

Table 13 Timing of collision detect in TRANSMITTING state

9.2.8 Timing of ED in NORMAL state

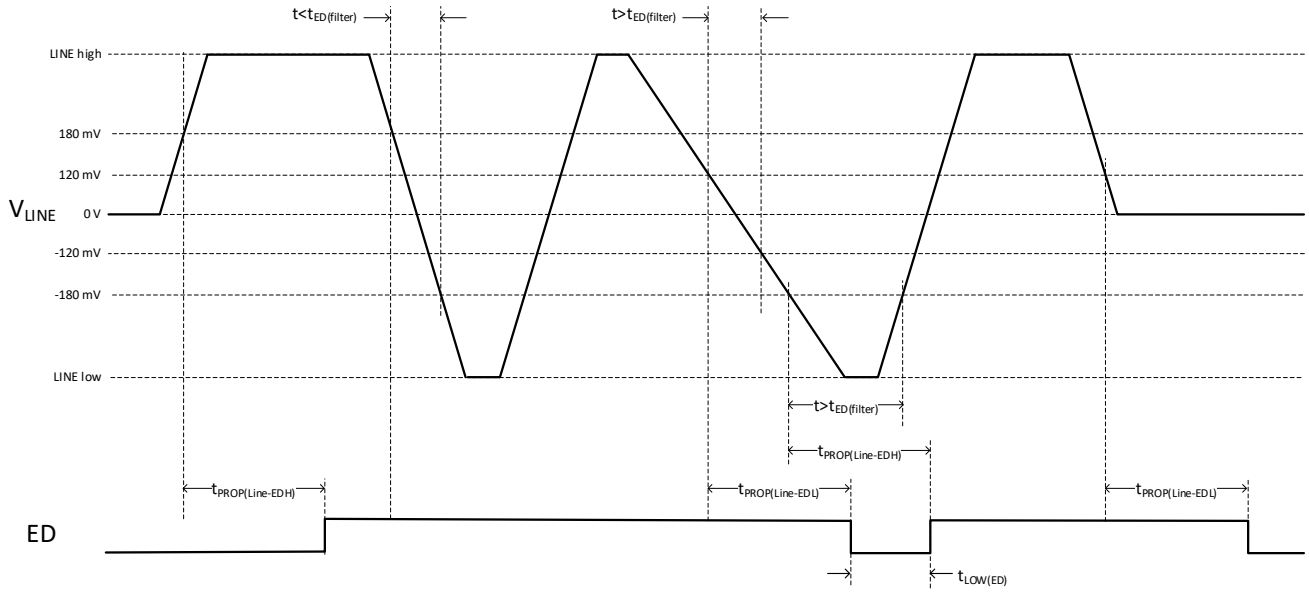


Figure 26: Timing of ED in NORMAL state with LINE high-level transition to/from idle

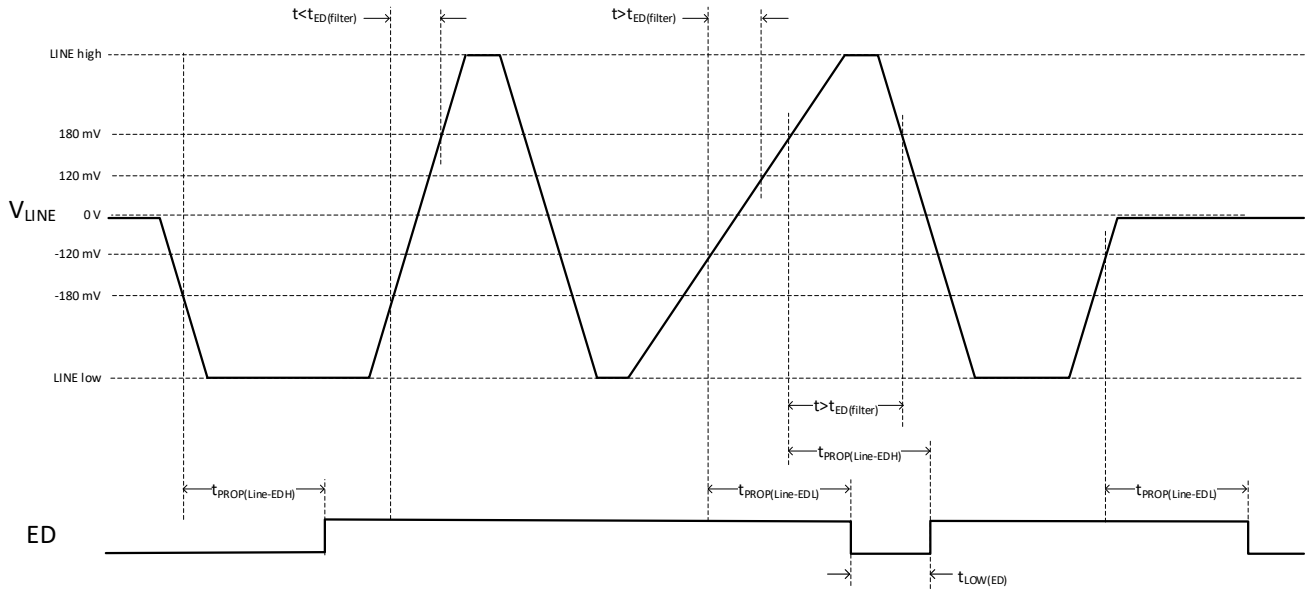


Figure 27: Timing of ED in NORMAL state with LINE low-level transition to/from idle

Parameter	Notation	Min [ns]	Max [ns]	Remark
ED specification in NORMAL state				
Propagation delay from LINE level to ED high[a]	$t_{PROP(Line-EDH)}$	-	130	Measured from a LINE rising voltage crossing +180 mV or a LINE falling voltage crossing -180 mV to rising edge crossing 50% level on ED (see Figure 26 and Figure 27)
Propagation delay from LINE level to ED low[a]	$t_{PROP(Line-EDL)}$	-	130	Measured from a LINE rising voltage crossing +120 mV or a LINE falling voltage crossing -120 mV to rising edge crossing 50% level on ED (see Figure 26 and Figure 27)
ED filter time[ab]	$t_{ED(filter)}$	21	39	Filter time when the LINE voltage is outside the +180 mV / -180 mV window or is inside the +120 mV / -120 mV window (see Figure 26 and Figure 27)
Low time ED[a]	$t_{LOW(ED)}$	21	-	Minimum low time ED after no carrier detection (see Figure 26 and Figure 27)

[a] The transitions between active and idle can be either driving the LINE from/to high or from/to LINE low.

[b] If the filter time is not reached ($t<t_{ED(filter)}$), the ED pin stays HIGH.

10 Appendix

10.1 Recommended 8-pin layout

For optimum EMC performance, a package with an exposed die pad is recommended. The exposed die pad shall be connected to GND. The optional pin 5 may act as a second GND line for better failure analysis capabilities (e.g., if the device needs to be decapsulated from the backside). During low power mode, the VIO pin shall be used as an "always on" supply to detect the WUT and power the RX and ED pins.

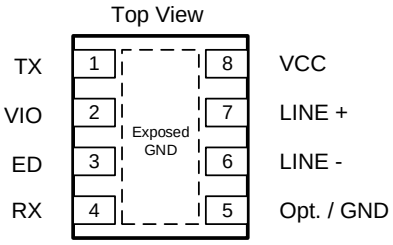


Figure 28: 8-pin layout recommendation

10.2 Recommended 14-pin layout

Devices with enhanced low-power functionality should be footprint compatible with the 8-pin derivatives. A battery supply input terminal should be included, used to supply the wakeup capability in case there is no other supply available (VCC and VIO may be unsupplied). The pin INH provides a battery-related high-side activation signal, e.g., external voltage regulators indicating the wakeup event. The WAKE pin may act as an additional local wakeup source and shall be battery tolerant. The assertion of WAKE shall produce on the PMD transceiver the same effect as the WUD (wake-up tone detected on the line). Additionally, the WAKE pin can be used to perform active wake forwarding, as described in the OPEN Alliance TC10 documentation[7]. The remaining pins (5 to 7) may be used for device-specific functionality. If a dedicated MDIO interface is implemented, pins 6 and 7 shall be used as MDIO and MDC respectively, as shown in Figure 29.

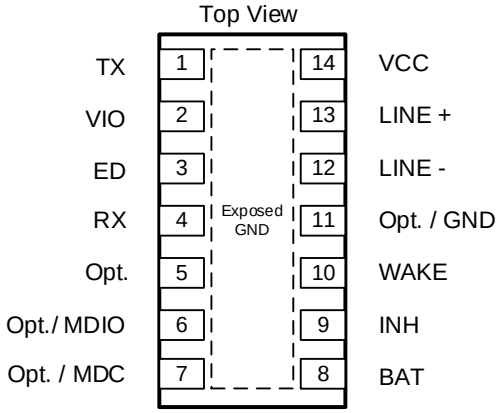


Figure 29: 14-pin layout recommendation

[7] At the time of writing this specification, the exact functionality of WAKE forwarding is not fully defined in TC10