IEEE 1000BASE-T1 Physical Media Attachment Test Suite

Version 1.1

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This suite of tests has been developed to help implementers evaluate the functionality of their IEEE 802.3bp 1000BASE-T1 Physical Media Attachment (PMA) based products.

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0.96	OPEN Technical Members only	• Updated 5.1.3 test procedure to include phase-noise analyzer • Added definition of 1518-byte packet to 5.2.1, 5.2.2, and 5.2.3 • Updated A.4 to describe voltage source minimum SFDR. Exact value not decided, marked as TBD. • Updated A.5 to include 5 MHz bandpass filter, and description of phase-noise analysis with 2.5 MHz integration bandwidth • Updated Appendix B with 1000BASE-T1 images provided by Keysight	09/29/2020
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2 INTRODUCTION

2.1 Overview

This particular suite of tests has been developed to help implementers evaluate the functionality of the PMA sublayer of their 1000BASE-T1 device, specifically the electrical specifications.

These tests are designed to determine if a product conforms to specifications defined in IEEE802.3 Clause 97. Successful completion of all tests contained in this suite does not guarantee that the tested device will operate with other devices. However, combined with satisfactory operation when tested in accordance with the OPEN Alliance 1000BASE-T1 Interoperability Test Suite, these tests provide a reasonable level of confidence that the Device Under Test (DUT) will function properly in many 1000BASE-T1 automotive environments.

The tests contained in this document are organized in such a manner as to simplify the identification of information related to a test, and to facilitate in the actual testing process. Tests are organized into groups, primarily in order to reduce setup time in the lab environment, however the different groups typically also tend to focus on specific aspects of device functionality. A three-part numbering system is used to organize the tests, where the first number indicates the section of the IEEE 802.3 Standard on which the test suite is based. The second and third numbers indicate the test's group number and test number within that group, respectively. This format allows for the addition of future tests to the appropriate groups without requiring the renumbering of the subsequent tests.

2.2 Normative References

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEEE 802.3-2018, Clause 97. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 1000BASE-T1

OPEN Alliance TC12 1000BASE-T1 system implementation specification– Version 1.1

OPEN Alliance TC9 Channel and component requirements for 1000BASE-T1 link segment Type A – Version 2.0

2.3 Terms and definitions

DUT Device Under Test

3 Organization of Tests

The test definitions themselves are intended to provide a high-level description of the motivation, resources, procedures, and methodologies pertinent to each test.

3.1 Elementary Test Structure

Specifically, each test description consists of the following fields as shown in Table 3.1. A brief description of each field is provided.

Table 3.1 – Elementary Test Structure

Purpose	The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.
References	This section specifies source material *external* to the test suite, including specific subsections pertinent to the test definition, or any other references that might be helpful in understanding the test methodology and/or test results. External sources are always referenced by number when mentioned in the test description. Any other references not specified by number are stated with respect to the test suite document itself.
Resource Requirements	The requirements section specifies the test hardware and/or software needed to perform the test. This is generally expressed in terms of minimum requirements; however, in some cases specific equipment manufacturer/model information may be provided.
Discussion	The discussion covers the assumptions made in the design or implementation of the test, as well as known limitations. Other items specific to the test are covered here.
Test Setup	The setup section describes the initial configuration of the test environment. Small changes in the configuration should not be included here, and are generally covered in the test procedure section, below.
Test Procedure	The procedure section of the test description contains the systematic instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.
Observable Results	This section lists the specific observables that can be examined by the tester in order to verify that the DUT is operating properly. When multiple values for an observable are possible, this section provides a short discussion on how to interpret them. The determination of a pass or fail outcome for a particular test is generally based on the successful (or unsuccessful) detection of a specific observable.
Potential Issues	This section contains a description of known issues with the test procedure, which may affect test results in certain situations. It may also refer the reader to test suite appendices and/or whitepapers that may provide more detail regarding these issues.

3.2 Test Reference Table

<table>
<tr><th colspan="2">Test Name</th><th>OA
Test Number</th><th>IEEE 802.3bp References</th></tr>
<tr><td colspan="4">Group 1: Electrical Measurements</td></tr>
<tr><td colspan="2">Maximum Output Droop</td><td>Test 97.1.1</td><td>97.5.3.1 – Transmitter output droop
97.7.2 – Test modes
97.5.2.1 – Test fixtures</td></tr>
<tr><td colspan="2">Transmitter Distortion</td><td>Test 97.1.2</td><td>97.5.3.2 – Transmitter distortion
97.7.2 – Test modes
97.5.2.1 – Test fixtures</td></tr>
<tr><td rowspan="3">Transmitter Timing Jitter</td><td>Case 1: MASTER</td><td rowspan="3">Test 97.1.3</td><td rowspan="3">97.5.3.3 – Transmitter timing jitter
97.7.2 – Test modes
97.5.2.1 – Test fixtures</td></tr>
<tr><td>Case 2: SLAVE</td></tr>
<tr><td>Case 3: MDI</td></tr>
<tr><td colspan="2">Transmitter Power Spectral Density</td><td>Test 97.1.4</td><td>97.5.2 - Test modes
97.5.2.1 - Test fixtures
97.5.3.4 - Transmitter power spectral density (PSD) and power level</td></tr>
<tr><td colspan="2">Transmitter Peak Differential Output</td><td>Test 97.1.5</td><td>97.5.2 - Test modes
97.5.2.1 - Test fixtures
97.5.3.5 - Transmitter peak differential output</td></tr>
<tr><td colspan="2">Transmit Clock Frequency</td><td>Test 97.1.6</td><td>97.5.3.6 - Transmitter clock frequency</td></tr>
<tr><td colspan="4">Group 2: PMA Receive Tests</td></tr>
<tr><td colspan="2">Bit Error Rate Verification</td><td>Test 97.2.1</td><td>97.5.4.1 - Receiver differential input signals
97.6 – Link segment characteristics</td></tr>
<tr><td colspan="2">Alien Crosstalk Noise Rejection</td><td>Test 97.2.2</td><td>97.5.4.2 - Alien crosstalk noise rejection
97.6 – Link segment characteristics</td></tr>
<tr><td colspan="2">Receiver Frequency Tolerance</td><td>Test 97.2.3</td><td>97.5.4.1 - Receiver differential input signals
97.5.3.6 – Transmitter clock frequency
97.6 – Link segment characteristics</td></tr>
<tr><td colspan="4">Group 3: MDI Impedance Requirements</td></tr>
<tr><td colspan="2">MDI Return Loss</td><td>Test 97.3.1</td><td>97.7.2.1 – MDI return loss</td></tr>
<tr><td colspan="2">MDI Mode Conversion Loss</td><td>Test 97.3.2</td><td>97.7.2.2 – MDI mode conversion loss</td></tr>
</table>

3.3 DUT Requirements

For the purposes of this test suite, the DUT is one port of a 1000BASE-T1 capable device that includes a 1000BASE-T1 PHY mounted on a PCB with an MDI connector and any necessary circuitry such as a low pass filter or common mode choke. All tests will be performed at the MDI connector of the DUT.

Please see the additional requirements listed in table 3.3:

Table 3.3 –DUT Requirements

Test Number and Name		Required Capabilities
Group 1: Electrical Measurements		
Test 97.1.1 – Maximum Output Droop		Test Mode 6
Test 97.1.2 – Transmitter Distortion		Test Mode 4
Test 97.1.3 – Transmitter Timing Jitter	Case 1: MASTER	Test Mode 1 (TX_TCLK125 access) MASTER/SLAVE configuration
	Case 2: SLAVE	
	Case 3: MDI	Test Mode 2
Test 97.1.4 – Transmitter Power Spectral Density		Test Mode 5
Test 97.1.5 – Transmitter Peak Differential Output		Test Mode 5
Test 97.1.6 – Transmit Clock Frequency		Test Mode 2
Group 2: PMA Receive Tests		
Test 97.2.1 – Bit Error Rate Verification		The ability to send and receive frames MASTER/SLAVE configuration
Test 97.2.2 – Alien Crosstalk Noise Rejection		The ability to send and receive frames MASTER/SLAVE configuration
Test 97.2.3 – Receiver Frequency Tolerance		The ability to send and receive frames MASTER/SLAVE configuration
Group 3: MDI Impedance Requirements		
Test 97.3.1 – MDI Return Loss		SLAVE configuration (active transmitter)
Test 97.3.2 – MDI Mode Conversion Loss		SLAVE configuration (active transmitter)

NOTE: Enabling test modes shall only change the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation.

4 List of Abbreviations and Definitions

ADC	Analog to Digital Converter
Automotive Cable	Balance 100Ω one pair cable having characteristics defined in Subclause 97.6 of the IEEE 802.3bp Physical Layer Specifications and Management Parameters for 1 Gb/s Operation over a Single Balanced Twisted-Pair Copper Cable (1000BASE-T1). Including Channel Type A.1, A.2, and A.3 defined in OPEN Alliance TC12 1000BASE-T1 System Implementation Specification.
BI_DA	Bi-directional Data Signal Pair A
BER	Bit Error Rate
DUT	Device Under Test
DSO	Real-time Digital Storage Oscilloscope
DSP	Digital Signal Processing
ECU	Electronic Control Unit
LCL	Longitudinal Conversion Loss
LCTL	Longitudinal Conversion Transmission Loss
LP	Link Partner
MDI	Medium Dependent Interface
MDI Test Head	Collection of fixturing used to connect the DUT MDI to the test equipment. Defined in TC9 Channel and component requirements for 1000BASE-T1 link segment Type A
PCB	Printed Circuit Board
PHY	Physical Layer
PLL	Phase Locked Loop
PPM	Parts Per Million
PSD	Power Spectral Density
SA	RF Spectral Analyzer
TDR	Time Domain Reflectometer
TIE	Time Interval Error
UI	Unit Interval
VNA	Vector Network Analyzer

5 Test cases

The following test cases shall be performed on all 1000BASE-T1 PHYs.

5.1 GROUP 1: Electrical Measurements

The tests defined in this section verify the voltage parameters defined for 1000BASE-T1 capable PHY's in IEEE 802.3bp Physical Layer Specifications and Management Parameters for 1 Gb/s Operation over a Single Twisted-Pair Copper Cable (1000BASE-T1).

5.1.1 Test 97.1.1 – Maximum Output Droop

Table 5.1.1 – Maximum Output Droop

Purpose	To verify that the transmitter output level does not droop more than the maximum specified amount.
References	[1] IEEE Std. 802.3-2018, subclause 97.5.2 - Test modes [2] Ibid., subclause 97.5.2.1 - Test fixtures [3] Ibid., subclause 97.5.3.1 - Maximum output droop
Resource Requirements	DSO MDI Test Head
Discussion	Reference [1] states that a 1000BASE-T1 device shall implement 6 test modes. These test modes are provided to measure electrical characteristics and verify compliance. Reference [2] defines the test fixture to be used to perform the test. Reference [1] defines the operation of a device while in test mode 6, and reference [3] provides a specification for the maximum allowable droop for the transmitter. This test requires the DUT to operate in transmitter test mode 6. While in test mode 6, the DUT shall generate a sequence of 15 +1 symbols followed by 15 -1 symbols continually transmitted. Since 1000BASE-T1 PHY's operate with a 750 MHz clock source, the Test Mode 6 transmit sequence results in a 25 MHz signal. Droop is calculated after measuring the voltage 4 ns after the initial zero crossings (V_{init}) and the voltage 16 ns after the zero crossing (V_{delay}). The difference $V_d = V_{init} - V_{delay}$. Droop = V_d/V_{init} * 100%. This is performed on both the positive and negative peaks of the waveform transmitted by test mode 1. The magnitude of the droop should be less than 10.0%.
Test Setup	Refer to test suite appendix **A**
Test Procedure	1. Configure the DUT so that it is operating in transmitter test mode 6. 2. Connect BI_DA from the MDI to Test Fixture 1. 3. Find the rising-edge zero crossing, then measure the voltage 4 ns after the zero crossing (V_{init}) in the waveform. 4. Measure the amplitude of the waveform at 16 ns after the zero crossing (V_{delay}) to find the droop voltage (V_d). 5. Compute the droop between V_{init} and V_d. 6. For enhanced accuracy, repeat steps 3-5 multiple times and average the results. 7. Repeat using a falling edge reference.
Observable Results	a. The magnitude of both the positive and negative droop shall be less than 10.0%.
Potential Issues	None.

5.1.2 Test 97.1.2 – Transmitter Distortion

Table 5.1.2 – Transmitter Distortion

Purpose	To verify that the distortion of the transmitter is within the conformance limits.
References	[1] IEEE Std. 802.3-2018, subclause 97.5.2 - Test modes [2] Ibid., subclause 97.5.2.1 - Test fixtures [3] Ibid., subclause 97.5.3.2 - Transmitter distortion
Resource Requirements	DSO Balun (if necessary) MDI Test Head
Discussion	Reference [1] states that a 1000BASE-T1 device shall implement 6 test modes. These test modes are provided to measure electrical characteristics and verify compliance. Reference [2] defines the test fixture to be used to perform the test, as well as the disturbing signal characteristics. Reference [1] defines the operation of a device while in test mode 4, and reference [3] provides a specification for the maximum allowable distortion for the transmitter. In this test, the peak distortion is measured by capturing the test mode 4 waveform and finding the least mean squared error. The peak error between the ideal reference and the observed symbols is the peak transmitter distortion. Reference [3] provides Matlab code for determining the peak distortion, note this code assumes the disturber signal and the data acquisition clock of the oscilloscope are frequency locked to the DUT TX_TCLK.
Test Setup	Refer to test suite appendix **A**
Test Procedure	1. Configure the DUT so that it is operating in transmitter test mode 4. 2. Configure the disturber source as described in [2]. 3. Connect BI_DA from the MDI to Test Fixture 2. 4. Capture 40 us of consecutive symbols in the test mode 4 waveform. 5. Using the code provided in [3], process the 40 us capture in Matlab to calculate the peak distortion at 10 uniformly spaced phase offsets over 1 UI.
Observable Results	a. The peak transmitter distortion should be less than 15mV for all of the sampled phase offsets over 1 UI.
Potential Issues	If the TX_TCLK125 of the DUT is not accessible or the DUT does not have an external clock input, the test equipment will not be able to synchronize internal sampling clocks. Because of this, phase offsets will occur in test equipment and measured distortion values will most likely be worse than if the DUT's TX_TCLK125 was available.

5.1.3 Test 97.1.3 – Transmitter Timing Jitter

Table 5.1.3 – Transmitter Timing Jitter

Purpose	To verify that the transmitter timing jitter of the PMA is within the conformance limits.
References	[1] IEEE Std. 802.3-2018, subclause 97.5.2 - Test modes [2] Ibid., subclause 97.5.2.1 - Test fixtures [3] Ibid., subclause 97.5.3.3 - Transmit timing jitter
Resource Requirements	DSO or SA with phase-noise measurement capabilities, bandpass bandwidth of the capturing device shall be larger than 5 MHz MDI Test Head
Discussion	Reference [1] states that a 1000BASE-T1 device shall implement 6 test modes. These test modes are provided to measure electrical characteristics and verify compliance. Reference [2] defines the test fixture to be used to perform the test. Reference [3] provides a specification for the maximum allowable timing jitter for the transmitter. *<u>Case 1 – MASTER transmitter timing jitter</u>* When configured for test mode 1 the DUT is in normal operation but a reduced version of the transmit symbol clock (TX_TCLK125) is exposed for testing purposes. The TX_TCLK125 signal is a 125 MHz signal, and the RMS TIE jitter measured on the TX_TCLK125 when the DUT is configured as MASTER shall be less than 5 ps. Additionally, the Peak-to-Peak TIE jitter measured on the TX_TCLK125 when the DUT is configured as MASTER shall be less than 50 ps. The jitter is measured over a time interval of at least 1 ms. *<u>Case 2 – SLAVE transmitter timing jitter</u>* When configured for test mode 1 the DUT is in normal operation but a reduced version of the transmit symbol clock (TX_TCLK125) is exposed for testing purposes. The TX_TCLK125 signal is a 125 MHz signal, and the RMS TIE jitter measured on the TX_TCLK125 when the DUT is configured as SLAVE shall be less than 10 ps. Additionally, the Peak-to-Peak TIE jitter measured on the TX_TCLK125 when the DUT is configured as SLAVE shall be less than 100 ps. The jitter is measured over a time interval of at least 1 ms. *<u>Case 3 – MDI transmitter timing jitter</u>* When in test mode 2, the PHY transmits three +1 symbols followed by three -1 symbols continuously. In this mode, the transmitter output should be a 125 MHz signal and the RMS TIE jitter measured at the PHY MDI output shall be less than 5 ps. Additionally, the Peak-to-Peak TIE jitter measured at the PHY MDI output shall be less than 50 ps. The jitter is measured over a time interval of at least 1 ms.
Test Setup	Refer to test suite appendix **A**

<table>
<tr><td>Test Procedure</td><td><u>Case 1 – MASTER transmitter timing jitter</u>
1. Configure the DUT so that it is operating in transmitter test mode 1, forced to MASTER.
2. Configure the LP so that it is operating in transmitter test mode 1, forced to SLAVE.
3. Connect the DUT TX_TCLK125 to the DSO or SA, as described in Test Fixture 3.
4. Measure
    a. For DSO approach: Capture at least 1 ms and process the capture through a 5 MHz bandpass filter to determine the RMS TIE jitter.
    b. For SA approach: Configure the SA for an integration bandwidth of 2.5 MHz, and capture at least 1 ms to determine the RMS TIE jitter.
5. For enhanced accuracy, repeat step 4 multiple times.

<u>Case 2 – SLAVE transmitter timing jitter</u>
6. Configure the DUT so that it is operating in transmitter test mode 1, forced to SLAVE.
7. Configure the LP so that it is operating in transmitter test mode 1, forced to MASTER.
8. Connect the DUT TX_TCLK125 to the DSO, as described in Test Fixture 3.
9. Measure
    a. For DSO approach: Capture at least 1 ms and process the capture through a 5 MHz bandpass filter to determine the RMS TIE jitter.
    b. For SA approach: Configure the SA for an integration bandwidth of 2.5 MHz, and capture at least 1 ms to determine the RMS TIE jitter.
10. For enhanced accuracy, repeat step 4 multiple times.

<u>Case 3 – MDI transmitter timing jitter</u>
11. Configure the DUT so that it is operating in transmitter test mode 2.
12. Connect BI_DA from the MDI to Test Fixture 4.
13. Capture at least 1 ms and process the capture through a 5 MHz bandpass filter to determine the RMS TIE jitter.
14. For enhanced accuracy, repeat step 3 multiple times.</td></tr>
<tr><td>Observable Results</td><td><u>Case 1 – MASTER transmitter timing jitter</u>
a. The RMS TIE jitter measured on the TX_TCLK125 should not exceed 5 ps.
b. The Peak-to-Peak TIE jitter measured on the TX_TCLK125 should not exceed 50 ps.

<u>Case 2 – SLAVE transmitter timing jitter</u>
c. The RMS TIE jitter measured on the TX_TCLK125 should not exceed 10 ps.
d. The Peak-to-Peak TIE jitter measured on the TX_TCLK125 should not exceed 100 ps.

<u>Case 3 – MDI transmitter timing jitter</u>
e. The RMS TIE jitter measured at the MDI should not exceed 5 ps.
f. The Peak-to-Peak TIE jitter measured at the MDI should not exceed 50 ps.</td></tr>
<tr><td>Potential Issues</td><td>If the DUT does not provide access to the TX_TCLK125, MASTER jitter (case 1) and SLAVE jitter (case 2) testing cannot be performed.</td></tr>
</table>

5.1.4 Test 97.1.4 – Transmitter Power Spectral Density

Table 5.1.4 – Transmitter Power Spectral Density

Purpose	To verify the transmitter power spectral density and power level are within the conformance limits.
References	[1] IEEE Std. 802.3-2018, subclause 97.5.2 - Test modes [2] Ibid., subclause 97.5.2.1 - Test fixtures [3] Ibid., subclause 97.5.3.4 - Transmitter power spectral density (PSD) and power level
Resource Requirements	SA, or DSO with spectral measurement capabilities Balun (if necessary) MDI Test Head
Discussion	Reference [1] states that a 1000BASE-T1 device shall implement 6 test modes. These test modes are provided to measure electrical characteristics and verify compliance. Reference [2] defines the test fixture to be used to perform the test. Reference [1] defines the operation of a device while in test mode 5, and reference [3] provides transmitter PSD mask and power level.
Test Setup	Refer to test suite appendix **A**
Test Procedure	1. Configure the DUT so that it is operating in transmitter test mode 5. 2. Connect BI_DA from the MDI to Test Fixture 5. 3. Configure the SA settings as follows: RBW = 100 KHz, VBW = 300 KHz, Sweep time > 1 second, and RMS Detector. If using a DSO, perform equivalent setup. 4. Capture the spectrum of the transmitted test mode waveform using a SA (or DSO). 5. Compute the transmitter PSD and power level.
Observable Results	a. The PSD of the transmitter output while operating in test mode 5 shall fit within the transmitter PSD mask defined in [3]. b. The transmit power level shall be less than 5 dBm.
Potential Issues	None.

5.1.5 Test 97.1.5 – Transmitter Peak Differential Output

Table 5.1.5 – Transmitter Peak Differential Output

Purpose	To verify that the peak-to-peak differential amplitude does not exceed the specified amount.
References	[1] IEEE Std. 802.3-2018, subclause 97.5.2 - Test modes [2] Ibid., subclause 97.5.2.1 - Test fixtures [3] Ibid., subclause 97.5.3.5 - Transmitter peak differential output
Resource Requirements	DSO MDI Test Head
Discussion	Reference [3] states that any 1000BASE-T1 transmitter peak-to-peak differential amplitude shall be less than 1.3 V_{PP} when measured with a 100 Ω termination. It also states that this is to be true for all transmit modes including SEND_S, SEND_T, SEND_I, and SEND_N modes. However, when a PHY is operating in Test Mode 5, as described in [1], the DUT is required to "transmit as in non-test operation and in the MASTER data mode with data set to normal Inter-Frame idle signals. Therefore Test Mode 5 should be sufficient for this test. Test Fixture 1, defined in [3], should be used to measure transmitter peak differential output.
Test Setup	Refer to test suite appendix **A**
Test Procedure	1. Configure the DUT so that it is operating in transmitter test mode 5. 2. Connect BI_DA from the MDI to Test Fixture 1. 3. Measure the peak-to-peak amplitude of the waveform. 4. For enhanced accuracy, repeat step 3 multiple times.
Observable Results	a. The maximum differential peak-to-peak amplitude of the waveform shall be less than 1.3 V_{PP}.
Potential Issues	None.

5.1.6 Test 97.1.6 – Transmit Clock Frequency

Table 5.1.6 – Transmit Clock Frequency

Purpose	To verify that the frequency of the Transmit Clock is within the conformance limits.
References	[1] IEEE Std. 802.3-2018, subclause 97.5.3.6 - Transmitter clock frequency
Resource Requirements	DSO MDI Test Head
Discussion	Reference [1] states that all 1000BASE-T1 devices must have a symbol transmission rate of 750 MHz ± 100ppm while operating in MASTER timing mode. This corresponds to a transmit clock of 749.925 MHz to 750.075 MHz. The reference clock used in this test is the one obtained in test 5.1.3, Transmitter Timing Jitter - Case 3. The frequency of this clock, extracted from the transmitted test mode 2 waveform, shall have a base frequency of 750 MHz ± 100ppm.
Test Setup	Refer to test suite appendix **A**
Test Procedure	1. Configure the DUT for test mode 2 operation. 2. Connect BI_DA from the MDI to Test Fixture 1. 3. Using a narrow-bandwidth PLL, extract the clock frequency from the transmitted symbols. 4. For enhanced accuracy, repeat step 3 multiple times. 5. Measure the frequency of the transmit clock.
Observable Results	a. The transmit clock generated by the DUT shall have a frequency between 749.925 MHz and 750.075 MHz.
Potential Issues	None.

5.2 GROUP 2: PMA Receive Tests

This section verifies the integrity of the 1000BASE-T1 PMA Receiver through frame reception tests.

5.2.1 Test 97.2.1 – Bit Error Rate Verification

Table 5.2.1 – Bit Error Rate Verification

Purpose	To verify that the DUT can maintain a BER of less than 10^{-10}.
References	[1] IEEE Std. 802.3-2018, subclause 97.5.4.1 - Receiver differential input signals [2] Ibid., subclause 97.6 – Link segment characteristics [3] IOL TP-PMD Test Suite Appendix 25.D [4] OPEN Alliance 1000BASE-T1 Interoperability Test Suite section 3.3 Channels definition
Resource Requirements	Packet transmit/monitoring station Automotive grade cables, minimum required channels defined in [4]
Discussion	Reference [1] states that a 1000BASE-T1 capable PHY shall not exceed a BER of less than 10^{-10}. The cables used for receiver BER testing are automotive grade cables, conformant to the characteristics described in [2] but representative of a worst case channel. Additionally, [4] describes three specific channels (A1, A2, A3) defined as test use cases for OPEN Alliance conformance testing. Packet transmit and monitoring stations are used to verify the BER of the DUT. Based on the analysis given in reference [3], if more than 7 errors are observed in 3×10^{10} bits (about 2,470,000 1,518-byte packets), it can be concluded that the error rate is greater than 10^{-10} with less than a 5% chance of error. Note that if no errors are observed, it can be concluded that the BER is no more than 10^{-10} with less than a 5% chance of error. For the purposes of this test, the packets received by the DUT are defined to include 6-byte Destination Address, 6-byte Source Address, 2-byte Length, 1500-byte Payload, and 4-byte CRC. Totaling to the described 1518-byte size.
Test Setup	Refer to test suite appendix A
Test Procedure	1. Configure the DUT as MASTER. 2. Connect the packet monitoring station to the automotive cable. 3. Connect the DUT to the automotive cable. 4. Send 2,470,000 1,518-byte packets (for a 10^{-10} BER) and the monitor will count the number of packet errors. 5. Repeat step 4 for the remaining automotive cables. 6. Repeat steps 4-5 with the DUT configured as SLAVE.
Observable Results	a. The DUT shall maintain a BER of less than 10^{-10} for all automotive cable lengths.
Potential Issues	None.

5.2.2 Test 97.2.2 – Alien Crosstalk Noise Rejection

Table 5.2.2 – Alien Crosstalk Noise Rejection

Purpose	To verify that the DUT can maintain a bit error rate of less than 10^{-10} in the presence of a crosstalk noise source.
References	[1] IEEE Std. 802.3-2018, subclause 97.5.4.2 - Alien crosstalk noise rejection [2] Ibid., subclause 97.6 – Link segment characteristics [3] OPEN Alliance 1000BASE-T1 Interoperability Test Suite section 3.3 Channels definition
Resource Requirements	Packet transmit/monitoring station Automotive grade cables, minimum required channels defined in [3] Noise Source (Gaussian distribution, bandwidth of 550 MHz and magnitude of –100 dBm/Hz)
Discussion	Reference [1] defines a test cable which uses a resistive network to inject crosstalk noise into the receive path of the DUT. Reference [1] goes on to state that a 1000BASE-T1 capable PHY shall not exceed a BER of less than 10^{-10}, even with alien crosstalk noise present. The cables used for receiver frequency tolerance testing are automotive cables, conformant to the characteristics described in [2] but representative of a worst case channel. Additionally, [3] describes three specific channels (A1, A2, A3) defined as test use cases for OPEN Alliance conformance testing. For the purposes of this test, the packets received by the DUT are defined to include 6-byte Destination Address, 6-byte Source Address, 2-byte Length, 1500-byte Payload, and 4-byte CRC. Totaling to the described 1518-byte size.
Test Setup	Refer to test suite appendix **A**
Test Procedure	1. Configure the DUT as MASTER. 2. Connect the packet monitoring station to the automotive cable. 3. Connect the DUT to the worst case automotive crosstalk noise injection cable. 4. Send 2,470,000 1,518-byte packets (for a 10^{-10} BER) and the monitor will count the number of packet errors. 5. Repeat steps 4 with the DUT configured as SLAVE.
Observable Results	a. The DUT shall maintain a BER of less than 10^{-10} when using the worst case automotive crosstalk noise injection cable with a Gaussian signal generator as the noise source.
Potential Issues	None.

5.2.3 Test 97.2.3 – Receiver Frequency Tolerance

Table 5.2.3 – Receiver Frequency Tolerance

Purpose	To verify that the DUT can properly accept incoming data with the symbol rate of 750 MHz +/- 100ppm.
References	[1] IEEE Std. 802.3-2018, subclause 97.5.4.1 - Receiver differential input signals [2] Ibid., subclause 97.5.3.6 – Transmitter clock frequency [3] Ibid., subclause 97.6 – Link segment characteristics [4] OPEN Alliance 1000BASE-T1 Interoperability Test Suite section 3.3 Channels definition
Resource Requirements	Packet transmit/monitoring station Automotive grade cables, minimum required channels defined in [4]
Discussion	Reference [1] states that a 1000BASE-T1 capable PHY shall not exceed a BER of less than 10^{-10}. Reference [2] states that a 1000BASE-T1 compliant PHY may have a transmitter clock frequency of 750 MHz +/- 100 ppm. This corresponds to a transmit clock of 749.925 MHz to 750.075 MHz. The cables used for receiver frequency tolerance testing are automotive cables, conformant to the characteristics described in [3] but representative of a worst case channel. Additionally, [4] describes three specific channels (A1, A2, A3) defined as test use cases for OPEN Alliance conformance testing. Packet transmit and monitoring stations are used to verify the BER of the DUT. For the purposes of this test, the packets received by the DUT are defined to include 6-byte Destination Address, 6-byte Source Address, 2-byte Length, 1500-byte Payload, and 4-byte CRC. Totaling to the described 1518-byte size.
Test Setup	Refer to test suite appendix **A**
Test Procedure	1. Configure the DUT as MASTER. 2. Connect the packet monitoring station to the automotive cable. 3. Connect the DUT to the automotive cable. 4. Configure the packet transmit/monitoring station to transmit data with a clock of 749.925 MHz 5. Send 2,470,000 1,518-byte packets (for a 10^{-10} BER) and the monitor will count the number of packet errors. 6. Repeat step 5 with the remaining automotive cables. 7. Repeat steps 5-6 with the DUT configured as SLAVE. 8. Repeat steps 1-7 using a transmit clock of 750.075 MHz.
Observable Results	a. The DUT shall maintain a BER of less than 10^{-10} for all automotive cable lengths.
Potential Issues	None.

5.3 GROUP 3: MDI Impedance Requirements

Overview:

The tests defined in this section verify the impedance characteristics of the MDI defined in Clause 97 of IEEE 802.3bp.

5.3.1 Test 97.3.1 – MDI Return Loss

Table 5.3.1 – MDI Return Loss

Purpose	To measure the return loss at the MDI.
References	[1] IEEE Std. 802.3-2018, subclause 97.7.2.1 – MDI return loss
Resource Requirements	VNA, TDR with frequency domain capabilities, or DSO with frequency domain capabilities Balun (if necessary) MDI Test Head
Discussion	A compliant 1000BASE-T1 device shall ideally have a differential characteristic impedance of 100Ω. This is necessary to match the characteristic impedance of the automotive cabling. Any difference between these impedances will result in a partial reflection of the transmitted signals. Return loss is a measure of the signal power that is reflected due to the impedance mismatch. Reference [1] specifies the conformance limits for the reflected power measured at the MDI.
Test Setup	Refer to test suite appendix **A**
Test Procedure	1. Configure the DUT for SLAVE mode operation. 2. Calibrate the VNA (or TDR, or DSO) to remove the effects of the test jig and connecting cable. 3. Connect the BI_DA from the MDI to the test equipment. 4. Measure the reflections at the MDI referenced to a 100Ω characteristic impedance.
Observable Results	a. The return loss measured at the MDI shall be at least 18-18*log10(20/f) dB from 2 to 20 MHz, and at least 18 dB from 20 to 100 MHz, and at least 18-16.7*log10(f/100) dB from 100 to 600 MHz when referenced to a characteristic impedance of 100 Ω.
Potential Issues	None.

5.3.2 Test 97.3.2 – MDI Mode Conversion Loss

Table 5.3.2 – MDI Mode Conversion Loss

Purpose	To measure the mode conversion loss at the MDI.
References	[1] IEEE Std. 802.3-2018, subclause 97.7.2.2 – MDI mode conversion loss
Resource Requirements	VNA, TDR with frequency domain capabilities, or DSO with frequency domain capabilities MDI Test Head
Discussion	A compliant 1000BASE-T1 device shall ideally have a differential characteristic impedance of 100Ω, however mismatches in the positive and negative polarities of the MDI output will introduce mode conversion. Reference [1] specifies the conformance limits for the mode conversion measured at the MDI.
Test Setup	Refer to test suite appendix **A**
Test Procedure	1. Configure the DUT for SLAVE mode operation. 2. Calibrate the VNA (or TDR, or DSO) to remove the effects of the test jig and connecting cable. 3. Connect the BI_DA from the MDI to the test equipment. 4. Measure the reflections at the MDI referenced to a 100Ω characteristic impedance.
Observable Results	a. The mode conversion loss measured at the MDI shall be at least 55 dB from 10 to 80 MHz, at least 77-11.51*log10(f) dB from 80 to 600 MHz when referenced to a characteristic impedance of 100 Ω.

6 Appendix A – 1000BASE-T1 Transmitter Test Fixtures

Purpose: To provide a reference implementation of Test Fixtures 1 through 5 as well as other transmit and receive test setups.

References:

[1] IEEE Std. 802.3bp, subclause 97.5.2.1 - Test fixtures
[2] Ibid., subclause 97.6 – Link segment characteristics
[3] Ibid., subclause 97.7.2 – MDI electrical specification
[4] Ibid., subclause 97.5.4.2 – Alien crosstalk noise rejection
[5] Ibid., subclause 97.5.3.3 - Transmitter timing jitter
[6] OPEN Alliance TC12 1000BASE-T1 system implementation specification– Version 1.1
[7] OPEN Alliance TC9 Channel and component requirements for 1000BASE-T1 link segment Type A – Version 2.0

Resource Requirements:

- DSO: Capable of 2 GHz bandwidth and a sampling rate of 7.5 GS/s or higher.
- SA: Capable of operating up to 600 MHz with a dynamic range of 50 dBm or higher, or equivalent Digital oscilloscope with spectral measurement capabilities.
- VNA: Capable of measuring from 1 MHz to 1 GHz or higher, or equivalent TDR with frequency domain capabilities
- Packet transmit/monitoring system
- Differential probe, or MDI Test Head (ie 2-pin to SMA adapter, Transmitter distortion adapter)
- High Impedance Differential Probe: Capable of operating up to 2 GHz or higher.
- Balun: Capable of operating from 1 MHz to 1 GHz, minimum bandwidth requirement.
- Disturbing signal generator: Capable of producing a sinusoid with differential amplitude of 3.6 Vpp and a frequency of 125 MHz
- Channel Type A.1, A.2, A.3
- Worst case automotive crosstalk noise injection cable
- Noise Source: Gaussian distribution, bandwidth of 550 MHz and magnitude of -100 dBm/Hz

Discussion:

A.1- Introduction

Reference [1] defines five test fixtures to be used in the verification of 1000BASE-T1 transmitter specifications. The purpose of this appendix is to present a reference implementation of these test fixtures, however the implementations described here are not the only acceptable method of performing the test cases defined in this document. This appendix describes test setups that can be used as Test Fixtures 1 through 5, a setup for MDI Return Loss, a setup for MDI Mode Conversion Loss, and Group 2: PMA Receive Test measurements.

A.2 – Cabling and Adapters

Reference [2] states that 1000BASE-T1 is designed to operate over 100 Ω one pair cable (automotive cable), and [3] defines the MDI connector can be any connector currently used in the automotive industry that does not degrade a signal worse than a 15 meter 100 Ω one pair cable. Leaving the choice of cabling and MDI connector up to the DUT manufacturer; because of this, flexibility is required in the development of the test setups and several different fixtures may be needed to perform all testing. Regardless of the design, it is vital that any fixtures and cabling included in the test setup meet the MDI Test Head requirements in [7]. While the reference diagrams of the MDI Test Head in [7] depict coax cabling it is still valid to use differential probes when performing Group 1 and Group 3 test cases as long as the remaining fixtures and components meet the stated requirements. Figure A.1 illustrates an example of a fixture that when paired with a short cable can represent a MDI Test Head used to connect the DUT to test equipment

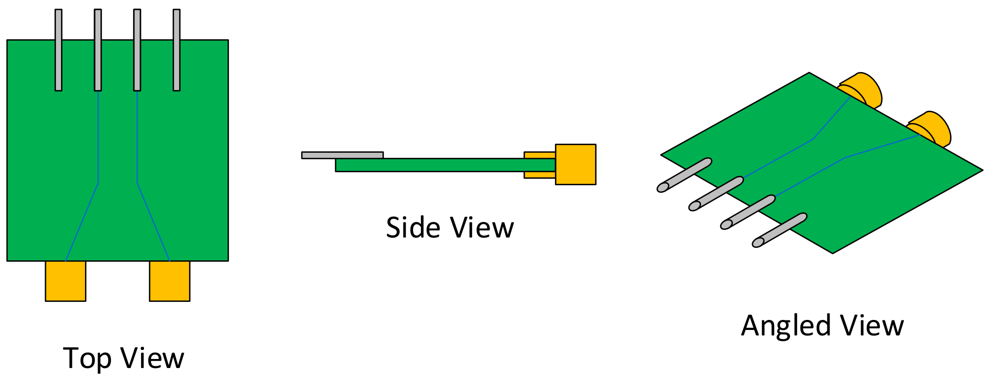

Figure A.1: 2-pin to SMA Adapter

Due to the wide variety of connectors that could be tested, a single cable cannot be used to connect every DUT to the SMA adapter. A short automotive cable with a connector that can mate with the DUT MDI on one end and can connect to the two pins on the SMA adapter, described above, on the other end will be used. By doing this a different cable can be used for each DUT and allow calibrating out the loss of the cable and adapter so that the test point will be at the devices MDI.

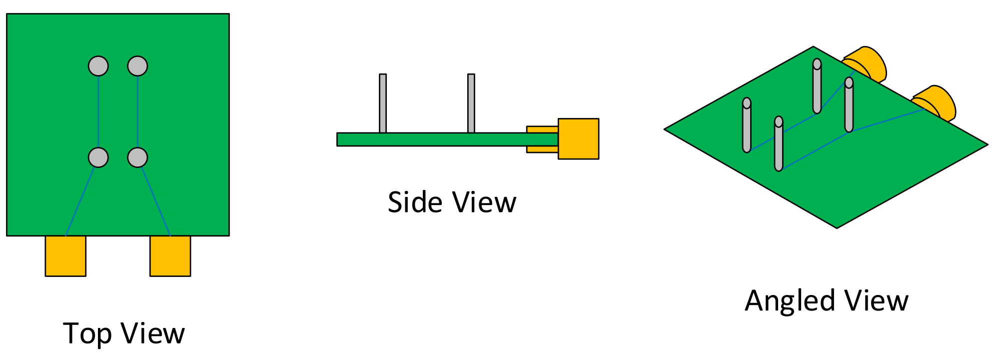

Figure A.2: Transmitter Distortion Adapter

To measure distortion an additional probing point is needed so that the disturbing sine wave can be delivered to the DUT, as well as measure the sum of the test mode 4 pattern and the disturbed voltage with a high impedance differential probe. Figure A.2 illustrates an example of such a fixture. This adapter is incorporated into the Test Fixture 2 test setup described in Figure A.4, and is still expected to meet the MDI Test Head requirements in [7].

Note: Any test fixture implementation that utilizes a balun (such as PSD or Return Loss measurements) in the transmit path from the DUT to the oscilloscope needs to de-embedded the associated losses of the balun from the conformance measurement.

A.3 – Test Fixture 1

Test Fixture 1 described in [1] will be used for maximum transmitter output droop, transmitter peak differential output, and transmitter timing jitter (Case 3: MDI transmitter timing jitter). Figure A.3 shows a diagram of the Test Fixture 1 setup.

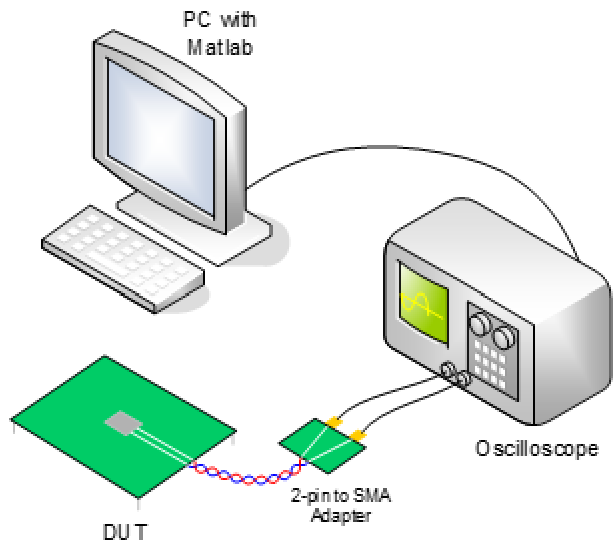

Figure A.3: Droop, Peak Output, Jitter (MDI transmitter timing jitter) Test Setup (Test Fixture 1)

The DUT is connected to the DSO using a MDI Test Head. The test mode waveforms are downloaded to a pc where Matlab scripts post-process the data. Alternatively, a differential probe and 100 Ω termination may be used instead of the 2-pin to SMA fixture and 50 Ω cables.

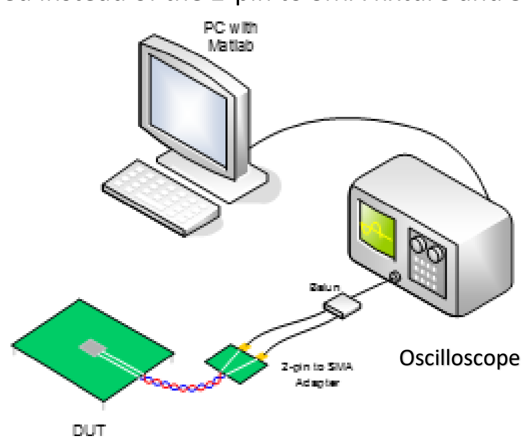

Figure A.4: MDI Jitter Test Setup (Test Fixture 4)

Additionally, [1] defines Test Fixture 4 which is specified as the setup used to measure MDI transmitter timing jitter. Test Fixture 1 and Test Fixture 4 are fundamentally similar, and can be considered equivalent, but Test Fixture 1 uses a high impedance differential probe while Test Fixture 4 uses a balun. Both setups are acceptable for measuring MDI transmitter timing jitter, however if Test Fixture 4 is used the balun will be in the transmit path from the DUT to the oscilloscope and should be de-embedded from the measurement. Since Test Fixture 1 can be used to perform this measurement it is recommended to not use test Fixture 4.

A.4 – Test Fixture 2

In Test Fixture 2, the DUT is directly connected to a 100 Ω differential voltage generator. The voltage generator transmits a sine wave of specific frequency and amplitude; which is referred to as the disturbing signal, V_d. An oscilloscope monitors the output of the DUT through a high impedance differential probe. Characteristics of the voltage generator and disturbing sine wave are given in Table A-1.

Table A-1: Characteristics of disturber waveform

V_d Amplitude	V_d Frequency	Voltage Generator Minimum SFDR
3.6 V peak-to-peak	125 MHz	40 dB

The purpose of V_d is to simulate the presence of a remote transmitter. If the DUT is not sufficiently linear, the disturbing signal will cause significant distortion products to appear in the DUT output. As such, the disturber source also needs to be sufficiently linear itself, as to not introduce additional distortion into the test setup. For this reason, it is recommended that the spurious-free dynamic range (SFDR) of the voltage generator be at least 40 dB below the fundamental frequency (V_d), as listed in Table A-1.

Due to the mixing of the V_d signal and Test Mode 4 at the probing point in Test Fixture 2, the oscilloscope will capture the sum of the V_d and the DUT output. However, only the DUT Test Mode 4 output is of interest. Therefore post-processing, or hardware filtering, is required to remove the disturbing signal from the measured waveform. If a hardware filter is employed to remove V_d from the measured waveform it must be positioned such that the DUT MDI receives V_d while being removed from the differential probe path.

Upon looking at the Test Fixture 2 definition shown in [1], it is important to note that V_d is defined as the voltage before the 50Ω resistors. Thus, the amount of voltage seen at the transmitter under test is 50% of the original amplitude of V_d. While Figure 4.A depicts a Distortion Generator with a differential output, it is also acceptable to use a single-ended source coupled with a balun. Such a setup would still be required to meet the V_d requirements listed in Table A-1.

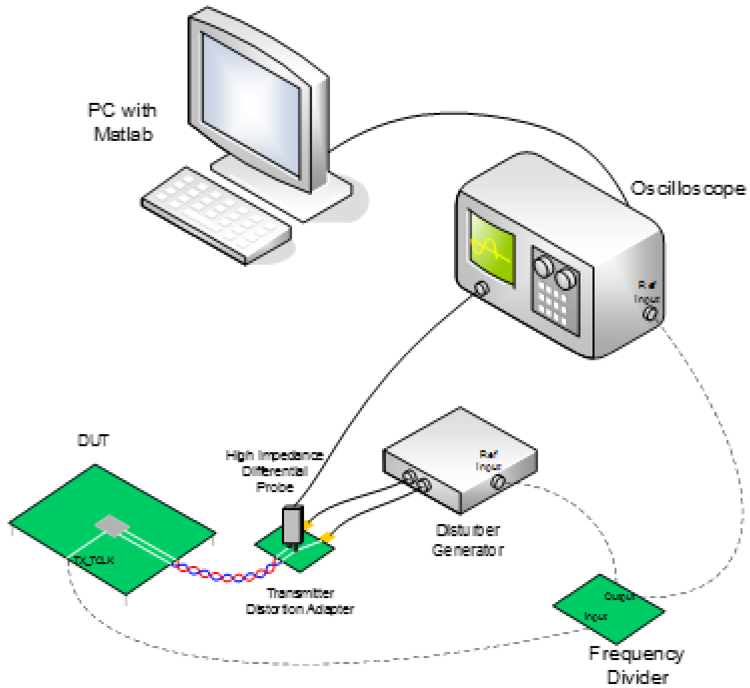

Figure A.5: Distortion Test Setup (Test Fixture 2)

The IEEE 802.3bp specification requires the test equipment used for transmit distortion measurements be synchronized with the DUT's TX_TCLK125, this guarantees that the internal sampling clock of each piece of equipment shares a common clock source and is phase locked. How to generate a reference clock from the TX_TCLK125 is not defined but can be achieved in several ways. Using a frequency divider to generate a 10 MHz clock from the 125 MHz TX_CLK125 is one such technique. This is depicted in Figure A.4 with a dashed line. However, depending on the DUT's design and form factor the TX_TCLK may not be exposed or brought out to a probe-able pin. Alternatively, it may be possible to provide a reference clock, which is synchronized with the test equipment, to the DUT. This is an equally sufficient and acceptable approach; however, it requires the DUT to be capable of using an external reference clock. This is not an IEEE specified requirement. When the TX_TCLK is not accessible, and an external clock cannot be used, distortion testing will need to be tested without test equipment synchronization. Because of this phase offsets will occur between the clock sources of each test equipment, and measured distortion values will most likely be worse than if the DUT's TX_TCLK125 was available.

A.5 – Test Fixture 3

Test Fixture 3 described in [1] will be used for MASTER and SLAVE transmitter timing jitter measurements. When performing this testing it is necessary to include a remote PHY to act as a 1000BASE-T1 link partner, allowing for the PHY under test to achieve and maintain a link during testing. The TIE jitter is measured on the DUT's TX_TCLK125 signal, for both MASTER and SLAVE test cases, while being processed through a 5 MHz bandpass filter. The filter is defined to have a center frequency of 125 MHz, and -3dB points at 122.5 MHz and 127.5 MHz. The DUT is forced to link and the MDI is connected to the MDI of the LP using an automotive cable. The TX_TCLK125 of the DUT is then connected to the

DSO. See Figure A.5 for this setup. If the TX_TCLK125 of the DUT is not accessible the MASTER and SLAVE jitter cannot be performed as described in [5].

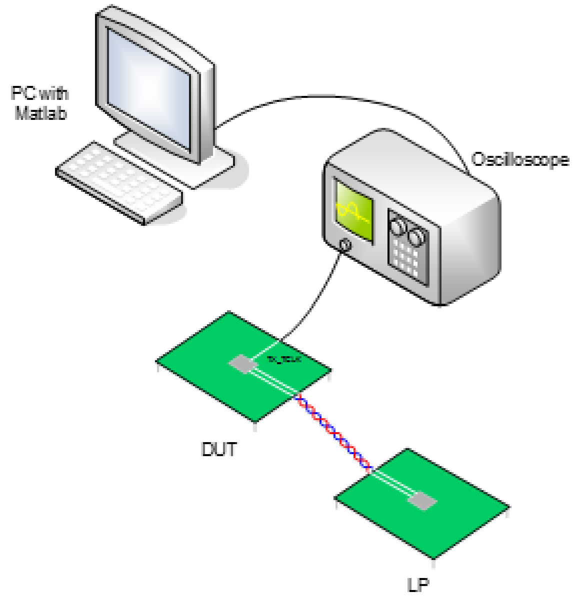

Figure A.6: Jitter (SLAVE) Test Setup

Alternatively, a SA can be used to measure the transmit jitter in the frequency domain as phase-noise. This can be done by connecting the TX_TCLK125 signal to the input of the SA instead of a DSO, however it is still necessary to collect the phase-noise through a bandpass filter. It is recommended that the integration bandwidth of the phase-noise analyzer is configured for 2.5 MHz to achieve equivalent results to a DSO approach using a 5 MHz bandpass filter.

A.6 – Test Fixture 5

Test Fixture 5 described in [1] will be used for transmitter PSD measurements. The PSD profile is downloaded from the SA and post-processed in Matlab. Figure A.6 shows a diagram of the Test Fixture 5 setup. A balun is necessary to convert the differential transmission of the DUT to a single-ended input for the SA. Alternatively a DSO may be used for measuring PSD, such a setup is demonstrated in Test Fixture 1 (A.3). Details regarding DSO settings and configurations for measuring PSD can be found in Appendix B.

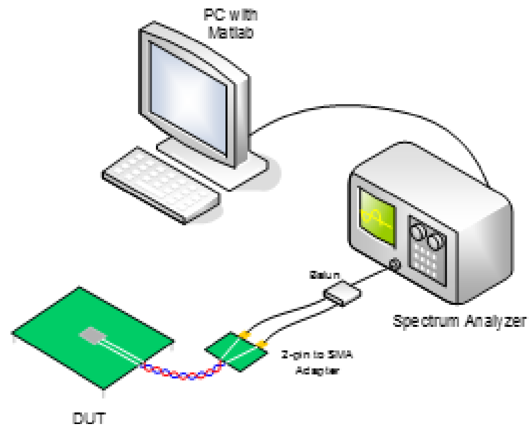

Figure A.7: PSD Test Setup (Test Fixture 5)

A.7 – MDI Return Loss and MDI Mode Conversion Loss Setup

The MDI return loss and mode conversion loss measurements are typically performed with a VNA. Mode conversion loss must be performed on a multi-port network analyzer (Figure A.9). Return loss can be performed on multi-port or single-port VNA (Figure A.8 and A.9) In the case of a single port VNA, a balun will be used to convert differential transmission of the DUT to the single-ended input of the VNA. See figure A.8. However, if the VNA has two or more input ports a balun is not necessary, see Figure A.9.

When measuring mode conversion loss the impedance balance of the cabling and test fixtures in the test setup is critical. In addition to the test fixtures used it is highly recommended that a reference ground plane is placed under the test setup, and securely connected to the test fixture for sufficient grounding. Any fixtures used to connect the MDI of the DUT to the test equipment should have mode conversion loss as defined in [7], Table 7.2-1.

Alternatively, a DSO may be used for performing the MDI measurements, such a setup is not shown in this document. For accurate results, the DSO should have sufficient dynamic range to verify compliance.

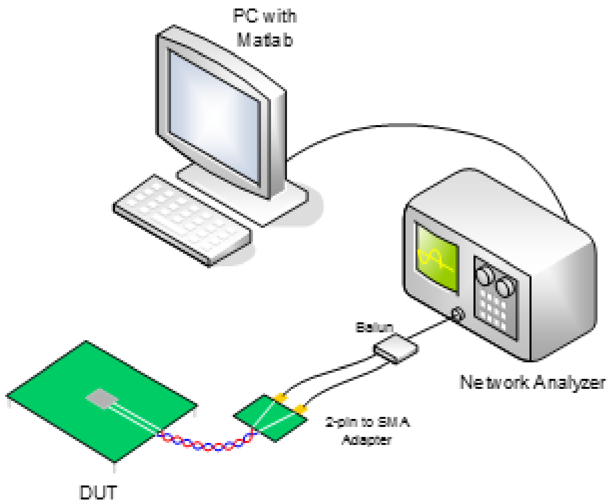

Figure A.8: MDI Return Loss with Single-port VNA

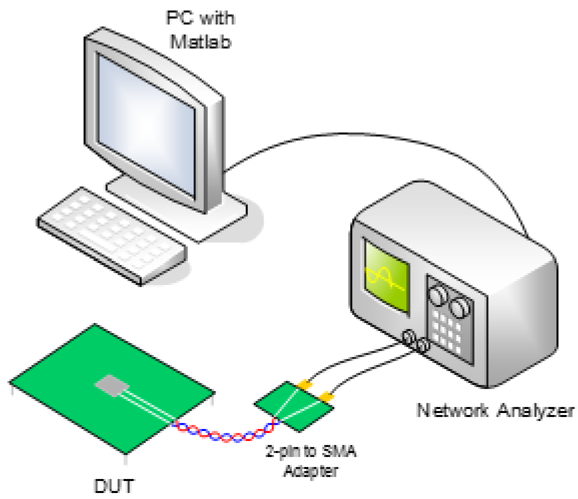

Figure A.9: MDI Return Loss and MDI Mode Conversion Loss with Multi-port VNA

A.8 – PMA Receiver Testing Setup

Figure A.10 describes the setup for Test 5.2.1 and 5.2.3, the only difference between the setups is the frequency of the link partner transmit clock. A packet generation and monitoring station will be used to measure the amount of dropped packets. This test is performed over various channel lengths, representative of the worst case channel defined in [2], to simulate real world environments. Additionally, [6] includes an appendix describing three channels that represent use cases specifically created for PHY conformance and interoperability evaluation.

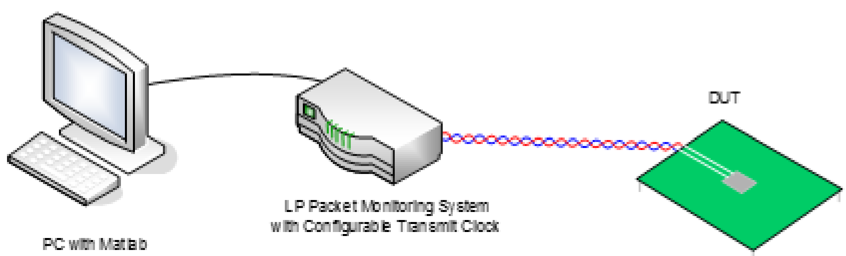

Figure A.10: BER & Receiver Frequency Tolerance Test Setup

A.9 – Alien Crosstalk Noise Rejection Setup

Figure A.11 describes the test cable used to introduce the crosstalk source defined in [4]. A small adapter populated with the necessary resistors is connected to the end of an automotive cable, closest to the receiver under test. The insertion loss of the test cable is conformant to the worst case characteristics described in [2]. Additionally, [6] includes an appendix describing three channels that represent use cases specifically created for PHY conformance and interoperability evaluation.

The Noise source is defined to be of Gaussian distribution, with bandwidth of 550 MHz and magnitude of –100 dBm/Hz. The -100 dBm/Hz is to be verified at the output of the noise source, terminated with 100Ω differential impedance (not connected to the test channel).

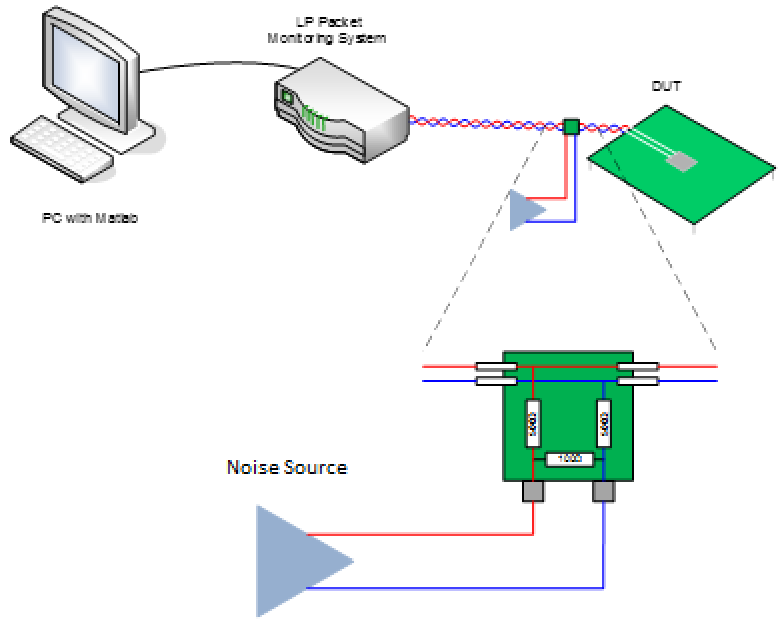

Figure A.11: Alien Crosstalk Noise Rejection Setup

7 Appendix B – Power Spectral Density Measurements on Oscilloscopes vs. Spectrum Analyzers

Purpose: Power spectral density (PSD) measurements are typical measurements for spectrum analyzers. However, an oscilloscope with FFT capabilities can perform such spectral measurements as well. This appendix highlights key aspects that should be taken into account when performing such measurements on an oscilloscope.

References:

[1] Rauscher, C., Janssen, V., Minihold R., „Fundamentals of Spectrum Analysis“, Rohde & Schwarz GmbH & Co. KG

Discussion:

B.1- Introduction

The power spectrum describes how the power of a signal is distributed over the frequency spectrum. For broadband or noise-like signals, it is often measured as the power spectral density, which is the power in a specified bandwidth, often 1 Hz. Hence, it is measured in dBm/Hz.

B.2 – PSD Measurement Parameters

In order to determine the power spectral density, one must measure the frequency spectrum of a signal. The resolution bandwidth of the instrument is the key parameter for determining the frequency spectrum.

B.2.1 - Resolution Bandwidth

In spectrum analysis, it is common practice to specify the 3 dB bandwidth of the resolution bandwidth filter.

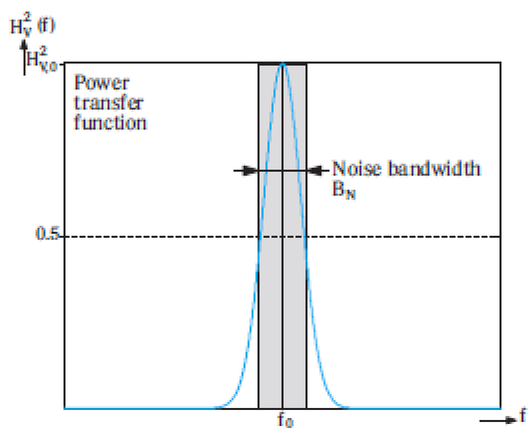

Figure B.1: Power transfer function of a Gaussian filter in linear level scale

Modern spectrum analyzers as well as oscilloscopes use digital filters. These are well defined in shape and can thus can be corrected according to the transfer function. The filter shape is optimized for steep roll-off in conjunction with minimized side-lobes.

When using a certain filter shape, the captured power differs from the ideal rectangular shape. Therefore, the results must be corrected for the filter shape before normalizing the values to 1 Hz.

Initial value is 3 dB bandwidth	4 filter circuits (analog)	5 filter circuits (analog)	Gaussian filter (digital)
6 dB bandwidth (B_{6dB})	$1.480 \cdot B_{3dB}$	$1.464 \cdot B_{3dB}$	$1.415 \cdot B_{3dB}$
Noise bandwidth (B_N)	$1.129 \cdot B_{3dB}$	$1.114 \cdot B_{3dB}$	$1.065 \cdot B_{3dB}$
Pulse bandwidth (B_I)	$1.806 \cdot B_{3dB}$	$1.727 \cdot B_{3dB}$	$1.506 \cdot B_{3dB}$
3 dB bandwidth (B_{3dB})	$0.676 \cdot B_{6dB}$	$0.683 \cdot B_{6dB}$	$0.707 \cdot B_{6dB}$
Noise bandwidth (B_N)	$0.763 \cdot B_{6dB}$	$0.761 \cdot B_{6dB}$	$0.753 \cdot B_{6dB}$
Pulse bandwidth (B_I)	$1.220 \cdot B_{6dB}$	$1.179 \cdot B_{6dB}$	$1.065 \cdot B_{6dB}$

Figure B.2: Typical correction factors for RBW filters

Consequently, the power spectral density is calculated according to the following formula:

$$PSD \left[\frac{dBm}{Hz}\right] = P[dBm] - 10 * \log(\frac{RBW * corr}{1Hz})$$

For RBW = 100 kHz, the formula leads to subtracting approximately 50 dB from the power at the respective frequency.

B.2.2 - Detector

For correct power measurements, the RMS detector shall be used. This type of detector is available both in spectrum analyzers and in some oscilloscopes.

B.2.3 – Windowing in FFT

The window function in the FFT calculation affects the level accuracy of the spectrum. Therefore, a suitable window function must be used. The Blackman Harris window function is a good choice for this purpose. This is available on most spectrum analyzers and oscilloscopes.

B.2.4 – Determining the Noise Bandwidth of the Filter

If the correction factor for the RBW filter is not available, it can be determined by measuring the filter shape in the frequency spectrum. The linear power must be integrated over frequency spectrum, normalized, and corrected to the nominal value of the filter bandwidth.

B.2.5– Sweep Time vs. Video Bandwidth vs. Averaging

Sweep time and video bandwidth both have a smoothing effect on the measured spectrum. The analogous parameter on the oscilloscope is averaging. By setting the average factor to a suitable value, one can achieve similar smoothing of the spectrum as if setting the sweep time on the spectrum analyzer.

B.3– Measurement of Continuous Sine Wave Signal

Measuring a continuous sine wave with additive noise demonstrates the analogy of the measurements on oscilloscopes vs. spectrum analyzers.

B.3.1 – Spectrum Analyzer

The spectrum analyzer display such a measurement.

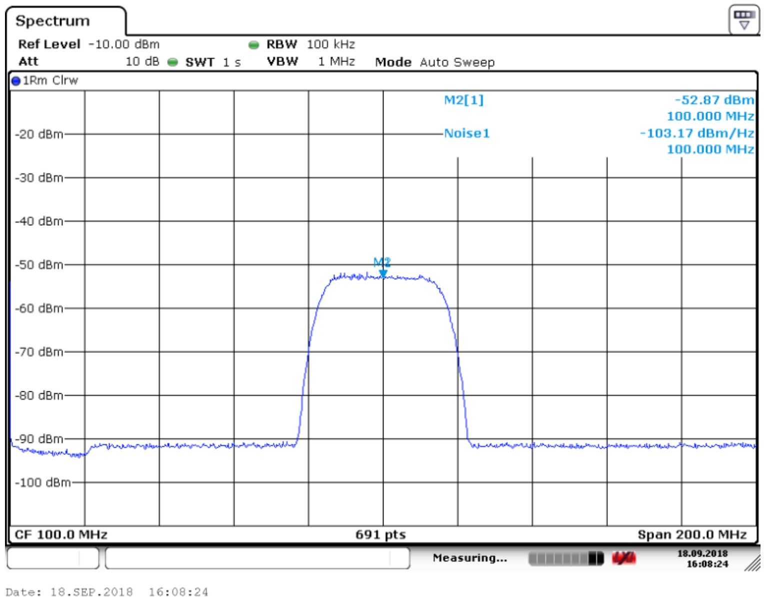

Figure 3: 100 MHz CW signal with additive noise on spectrum analyzer

For simplicity, a normal marker and a noise marker (spectral density) show the corresponding values at 100 MHz.

B.3.2 – Oscilloscope

The same signal on the oscilloscope looks very similar.

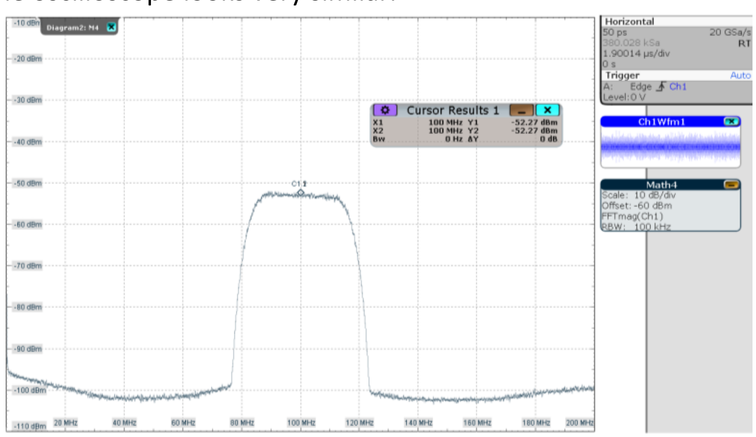

Figure 4: 100 MHz CW signal with additive noise on oscilloscope

B.4 – Measurement of 1000BASE-T1 Test Mode 5 Signal

Now we apply the real 1000BASE-T1 test mode 5 signal for the PSD measurements on the instruments. The screenshots below display the raw spectrum as it comes out of the test fixture. Input coupling is set to DC coupling; the test fixture uses a balun to convert the differential signal into a single ended one.

B.4.1 – Spectrum Analyzer

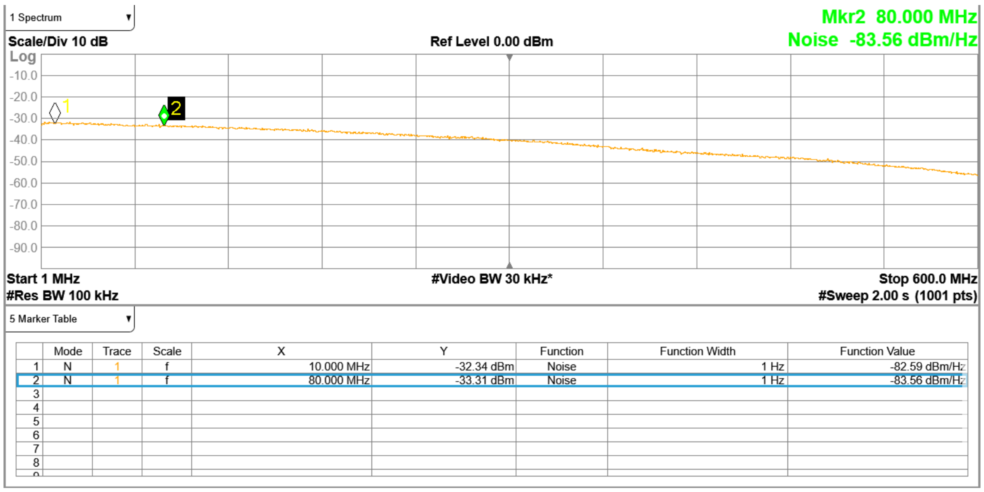

Figure 5: Spectrum with the marker at 10 MHz and 80 MHz

As expected, the PSD value is very close to 50 dB below the normal marker value. This corresponds to the RBW of 100 kHz normalized to 1 Hz.

Here as well, the PSD value is very close to 50 dB below the normal marker value. This corresponds to the RBW of 100 kHz normalized to 1 Hz.

B.4.2 – Oscilloscope

The same signal on the oscilloscope:

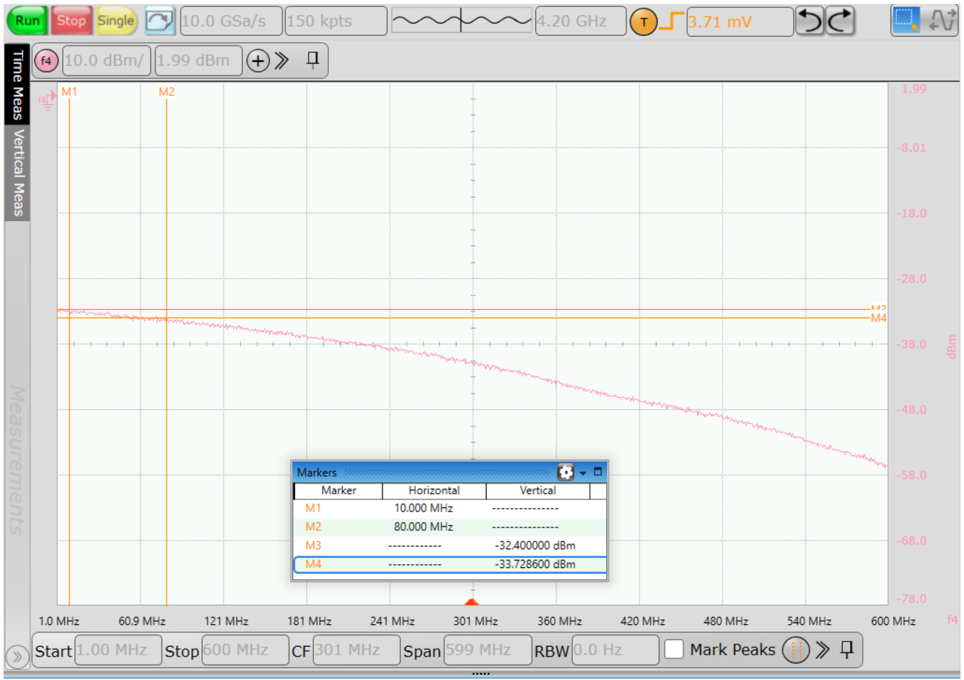

Figure 7: Spectrum of test mode 5 signal on the oscilloscope

As you can see, the two discrete values match very closely.

- 10 MHz: delta 0.06 dB
- 80 MHz: delta 0.41 dB

These values are within the instrument’s specifications for level measurements.

B.5 – Summary

Given that modern oscilloscopes allow spectrum measurements to be configured in a similar way like on spectrum analyzers (setting start & stop frequency and RBW), the potential of misconfiguration is rather limited. As demonstrated above, the measurement results match very well on both CW signals with additive noise as well as 1000BASE-T1 test mode 5 signals.