Advanced diagnostic features for 1000BASE-T1 automotive Ethernet PHYs

TC12 - advanced PHY features

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Contents

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2 Introduction

This specification describes advanced features of a 1000BASE-T1 automotive Ethernet PHY (often also called transceiver), e.g. for diagnostic purposes for automotive Ethernet PHYs.

3 Normative references

[1] IEEE P802.3bp™ Amendment 4: Physical Layer Specifications and Management Parameters for 1 Gb/s Operation over a Single Twisted-Pair Copper Cable - Clause 97

4 Abbreviation/Symbols

*****	AND
!	NOT
+	OR
COM	Communication ready (status bit)
COR	Polarity correct
DCQ	Dynamic Channel Quality
DD	Defect distance
DET	Polarity detect
ECU	Electronic Control Unit
ESD	End of Stream Delimiter
FAV	FEC Counter Average
FEC	Forward Error Correction
FLB	FEC Counter Last Block
HDD	Harness defect detection
LFL	Link Failures and Losses
LP	Link Partner
LQ	Link Quality
LRT	Local Receiver Time
LTT	Link-Training Time
MSE	Mean Square Error
MSE_WC	Mean Square Error Worst Case
OS	OPEN/SHORT detection
PEC	Pulse Error Correction
PHY	PHY is a Physical layer interface device, often called transceiver
pMSE	Peak MSE

POL	Polarity
RRT	Remote Receiver Time
RS-FEC	Reed Solomon Forward Error Correction
SDD	Start of stream Delimiter
SQI	Signal Quality Index
TDR	Time Delay Reflection

5 Overview

1000BASE-T1 automotive Ethernet transceivers (PHY or every PHY port of a switch) shall offer the information specified below for diagnostic purposes.

group	group name	parameter	parameter name	Description	mandatory /optional	remarks
DCQ	dynamic channel	MSE	Mean Square Error	The MSE (Mean Square Error) value of the symbol detection shall be determined in a standardized way	o	1)
		SQI	Signal Quality Index	A classification of the signal quality in 8 stages (3 bit) shall be carried out	m	1), 2)
		pMSE	peak MSE	to identify short time noise (pulses) a peak MSE value shall be provided (for 1000BASE-T1)	o	1)
HDD	Harness defect detection	OS	OPEN/SHORT detection	Cable-Harness errors (short circuit or open line) shall be detected	m	
	TDR based Cable	TDR	SHORT/OPEN/NNOISE / DISTANCE	Cable Harness errors detected by TDR-like test approach	m	
LQ	LinkQuality	LTT	Link-training time	The time of the last link training shall be stored	m	
		LRT	Local Receiver Time	The timing of the local receiver shall be stored	o	
		RRT	Remote Receiver Time	The timing of the remote receiver shall be stored	o	
		LFL	Link Failures and Losses	number of link losses since the last power cycle shall be stored	m	
		COM	communication ready	Optimized Link Status information. Signals when communication is possible.	m	
POL	Polarity detection & correction	DET	Polarity detect	according to the IEEE specifications of 1000BASE-T1	m	
		COR	Polarity correct	according to the IEEE specifications of 1000BASE-T1	m	
FEC	Forward Error Correction	FLB	Counter Last Block	FEC counter	m	
		FAV	Counter Average	Average value of the last 128 single values of FEC block	m	

Table 1: Overview of required PHY parameters to be stored and provided via registers.

Remarks to Table 1:

1) The dynamic channel quality shall be determined with a reasonable refresh rate and be stored in the corresponding defined registers. For the evaluation of all registers that represent a dynamic signal quality, there shall be a second register providing the worst value since the last register reading process.

2) The 8 stages should correlate to according SNR values at the MDI and may represent corresponding bit error rates (in the case of an interference model with white noise).

All optional topics ‘o’ are initial proposals and are only seen as a rough framework. Optional features are not yet fully checked in terms or implementation, feasibility and thus could be changed or even dropped in a next version of this document.

3) All of the above registers can be reset to a value of ‘0’ by writing ‘0’ to the register value at any point through software tools.

6 Advanced PHY features

6.1 Dynamic Channel Quality (DCQ)

Dynamic channel quality includes MSE values, SQI values, and peak MSE values.

6.1.1 Mean Square Error (MSE)

Optional or mandatory feature: Optional
Providing Mean Square Error information is optional, if provided it is recommended that the calculation is defined and controlled by the implementer. The MSE information shall not be used for further qualification (e.g. for Interop Testing). For qualification purposes the mandatory SQI information is defined.

The PHY can provide detailed information of the dynamic signal quality by means of a MSE value or comparable information. The MSE value can e.g. be determined from the MeanSquareError of the slicer. The following recommendations can be used as guidance for calculating and presenting the MSE value:

The MSE value for 1000BASE-T1 should be determined across 2^16 (65,536) symbols (summing up and normalization), with a refresh rate in the tolerance range of 80us – 200us. The resulting MSE value shall be linearly scaled to a value in the range of [0…511] and this value shall be placed in the register, DCQ.MSE.

In addition to the current MSE value the worst case MSE value since the last read should be stored in a second register.

Register	DCQ.MSE
Name	Mean Square Error
size[bits]	9+1

Bit	Description
[8:0]	MSE value
[9]	MSE value valid [1=invalid;0=valid]

register value	Explanation
0x0000	MSE = 0
…	…
0x01FE	MSE = 510
0x01FF	MSE = 511

Table 2 Definition of DCQ.MSE

Register	DCQ.MSE_WC
Name	Worst Case Mean Square Error
size[bits]	9+1

Bit	description
[8:0]	MSE value
[9]	MSE value valid [1=invalid;0=valid]

register value	explanation
0x0000	MSE = 0
…	…
0x01FE	MSE = 510
0x01FF	MSE = 511

Table 3 Definition of DCQ.MSE_WC

6.1.2 Signal Quality Index (SQI)

Optional or mandatory feature: mandatory

The signal quality value (SQI) shall be determined from the determined MSE value or comparable information. The SQI value shall be stored in a register in 8 levels (between “000” = worst value and “111” = 7 = best value).

In addition to the current SQI value, the lowest SQI value calculated since the last register read access shall be stored in the DCQ.SQI register as shown below.

Register	DCQ.SQI
Name	Signal Quality Index
size[bits]	8

bit	Description
[0]	Reserved
[3:1]	current SQI value
[4]	Reserved
[7:5]	worst case SQI value since last read

register value	Explanation
0x0	SQI=0 (worst value)
0x1	SQI=1
0x2	SQI=2
0x3	SQI=3
0x4	SQI=4
0x5	SQI=5
0x6	SQI=6
0x7	SQI=7 (best value)

Table 4 Definition of DCQ.SQI

The following features of the SQI value are mandatory:

- When the register value outputs a value of 0 a link loss shall be recorded through the LQ.LFL register.
- The indicated signal quality shall monotonically increase /decrease with noise level.
- It shall be indicated in the datasheet at which level a BER<10^-10 (better than 10^-10) is achieved (e.g. "from SQI=3 to SQI=7 the link has a BER<10^-10 (better than 10^-10)")

During interoperability testing the indicated signal quality shall be monitored and documented for information only.

The recommended correlation between the SQI values stored in the register and an accompanying signal to noise ratio (SNR) based on AWG noise (bandwidth of 550MHz) is shown in Table 5. The bit error rates to be expected in the case of white noise as interference signal are shown in the table as well for information purposes.

SQI value	SNR value @MDI - AWG noise, 80MHz (informative)	recommended BER for AWG noise model (informative)
SQI=0	<18dB	BER>10^-10
SQI=1	18dB=<SNR<19dB	
SQI=2	19dB=<SNR<20dB	
SQI=3	20dB=<SNR<21dB	BER<10^-10
SQI=4	21dB=<SNR<22dB	
SQI=5	22dB=<SNR<23dB	
SQI=6	23dB=<SNR<24dB	
SQI=7	24dB=<SNR	

Table 5 Recommended correlation from SQI to SNR under AWG assumption.

6.1.3 Peak MSE value (pMSE)

Optional or mandatory feature: optional

Providing peakMSE information is optional. Goal of the peakMSE value is to identify transient disturbances which are typically in the µs-range. If this information is provided, it is recommended to provide according to the described algorithm. The peakMSE information shall not be used for further qualification (e.g. for Interop Testing). For qualification purposes the mandatory SQI information is defined.

For 1000BASE-T1 a peakMSE value can be stored (identification of transient disturbances). The peakMSE value shall be determined from the MeanSquareError of the slicer. The peakMSE value can be determined by a sliding window over 128 symbols. Each 2^16 (65,536) symbols the maximum value of this sliding window shall be stored in an 8bit register (range is 0…63).

The value can be determined with a refresh rate in the tolerance range of 80us to 200us.

Register	DCQ.peakMSE (only 1000BASE-T1)
Name	peak MSE
size[bits]	8 + 8

bit	Description
[7:0]	current peak MSE value
[15:8]	Worst case peak MSE value since last read

register value	explanation (1000BASE-T1) for peakMSE (lower 8 bit) and worst case peakMSE (higher8 bit)
0x00	peakMSE = 0
0x01	peakMSE = 1
…	…
0x3E	peakMSE = 62
0x3F	peakMSE = 63
0x40 … 0xFE	value invalid
0xFF	measurement not possible

Table 6 Definition of DCQ.peakMSE

6.2 Harness Defect Detection (HDD)

6.2.1 OPEN and SHORT detection (OS)

Optional or mandatory feature: Optional

There shall be a possibility to detect harness defects. This can either be done during normal operation (as long as possible) or in a specific host-triggered diagnostic mode. With this functionality a PHY shall reliably detect the following error situations as long as the channel is properly terminated (link partner termination is connected to the channel):

- OPEN of one bus wire
- OPEN of both bus wires
- SHORT of both conductors (to ground or supply line)
- SHORT between both bus wires
- (OPTIONAL) SHORT of one conductor (to ground or supply line)*

(OPEN = open circuit, SHORT = short circuit)

It is not needed to distinguish all of the above error situations individually.

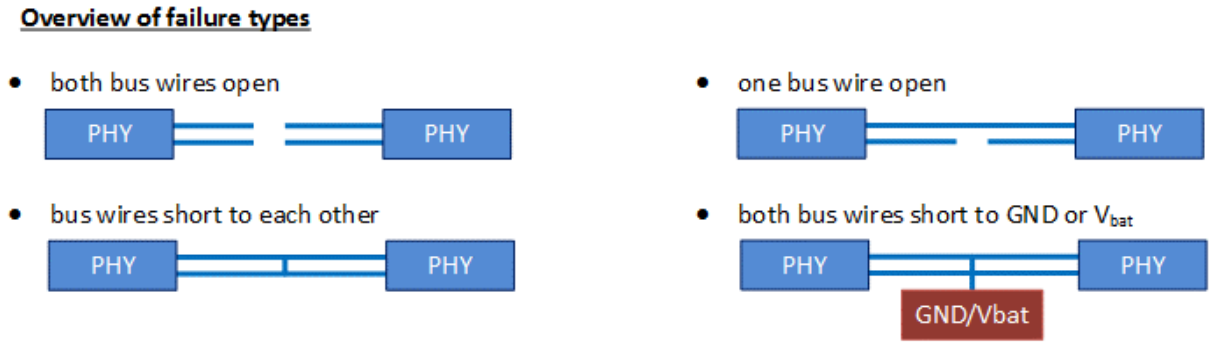

Figure 1 Overview of error situations to be detected.

It is mandatory to detect all these failures when the LP is not transmitting any signal (typically “SEND_Z” for 1000BASE-T1 or as SLAVE). Optionally these failures are also detected when the LP is MASTER and transmitting e.g. TRAINING pattern.*) REMARK: The condition of short circuit of one bus wire to GND or VBAT is not reliably detectable with today’s technology. The detection of short circuit of one wire to GND or VBAT is therefore an optional feature. If no link loss is occurring, this only may be identified by higher layers due to significantly decreased signal quality. An indication for such a failure may be a significantly reduced SQI or sporadic link losses, which can be detected by higher layers (e.g. by SQI register or LinkLoss register).

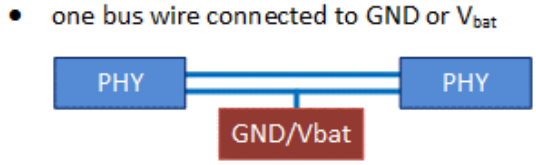

Figure 2 Overview of error situation optionally to be detected.

Table 7 is showing the Bus Failure Matrix, indicating which combinations of failures and environmental conditions are mandatory to detect and which combinations are optional.

Bus Failure Matrix	LP is SLAVE	LP is MASTER
cable OK	mandatory	optional
Both bus wires OPEN	mandatory	optional
Bus wires SHORT	mandatory	optional
One bus wire OPEN	mandatory	optional
both bus wires SHORT to GND/VBAT	mandatory	optional
one bus wires SHORT to GND/VBAT	optional	optional

Table 7 bus failure matrix.

6.2.2 Time Delay Reflection (TDR)

Optional or mandatory feature: mandatory

There shall be the possibility to use a TDR based diagnostic feature for cable diagnostic. This feature is applicable only in diagnostic mode of the PHY device and shall not be activated during normal operation. The TDR diagnostic feature shall be available in both PHY modes: Master or Slave. This diagnostic mode shall be available on a 1000BASE-T1 device independent if operating in 100BASE-T1 or 1000BASE-T1 mode.

Activating the TDR feature shall deliver the following information:

Register	HDD.TDR (only 1000BASE-T1 devices)
Name	TDR
size[bits]	8 + 8

bit	Description
[1:0]	TDR activation 01 = TDR OFF; 10 TDR = ON; 00 , 11= TDR not available
[3:2]	Reserved
[7:4]	0011 = Short 0110 = Open 0101 = Noise 0111 = Cable O.K. 1000 = Test in progress; initial value with TDR ON 1101 = Test not possible (e.g. noise; active link/communication) 0000, 0001, 0010, 0100, 1001, 1010, 1011, 1100, 1110, 1111 value invalid
[13:8]	1Bit = Distance to 1st / main fault 1Bit approx. 1m approx.. 1… 31m 000000 = no error 000001 = error about 0-1m away 000002 = error between 1-2m away … 011111= error about 30-31m away 111111 = resolution not possible / out of distance
[15:14]	Reserved

Table 8 Definition of **HDD.TDR**

In order to enhance the resolution, in addition to a single pulse, multiple pulses can be used. Also, settings from the PHY internal equalizer, the echo compensation and other signal processing units can be used.

6.3 Link quality – start-up time and link losses (LQ)

6.3.1 Link training time (LTT)

Optional or mandatory feature: mandatory

The transceiver shall provide the time required to establish a link, in this context, the following time definitions apply:

- 1000BASE-T1

  Linkup Time (LU) = t_{Stop} - t_{Start}

  t_{Start} *= time (link_control=ENABLE) OR*

  $_{Tstop}$*=> the timing entering SEND_Data state*

  The timer for the time measurement shall be started when entering SLAVE_SILENT, either from DISABLE_TRANSMITTER or from a stable link (SEND_IDLE_OR_DATA). The timer shall stop when entering SEND_IDLE_OR_DATA (link has established).

The respective value for the start-up [in ms] shall be stored in a 16 bit register. Here the value ranges from [0x00 = 0ms] to [0xFA = 250ms], all higher values shall be stored with [0xFB].

97.4.5 State diagrams

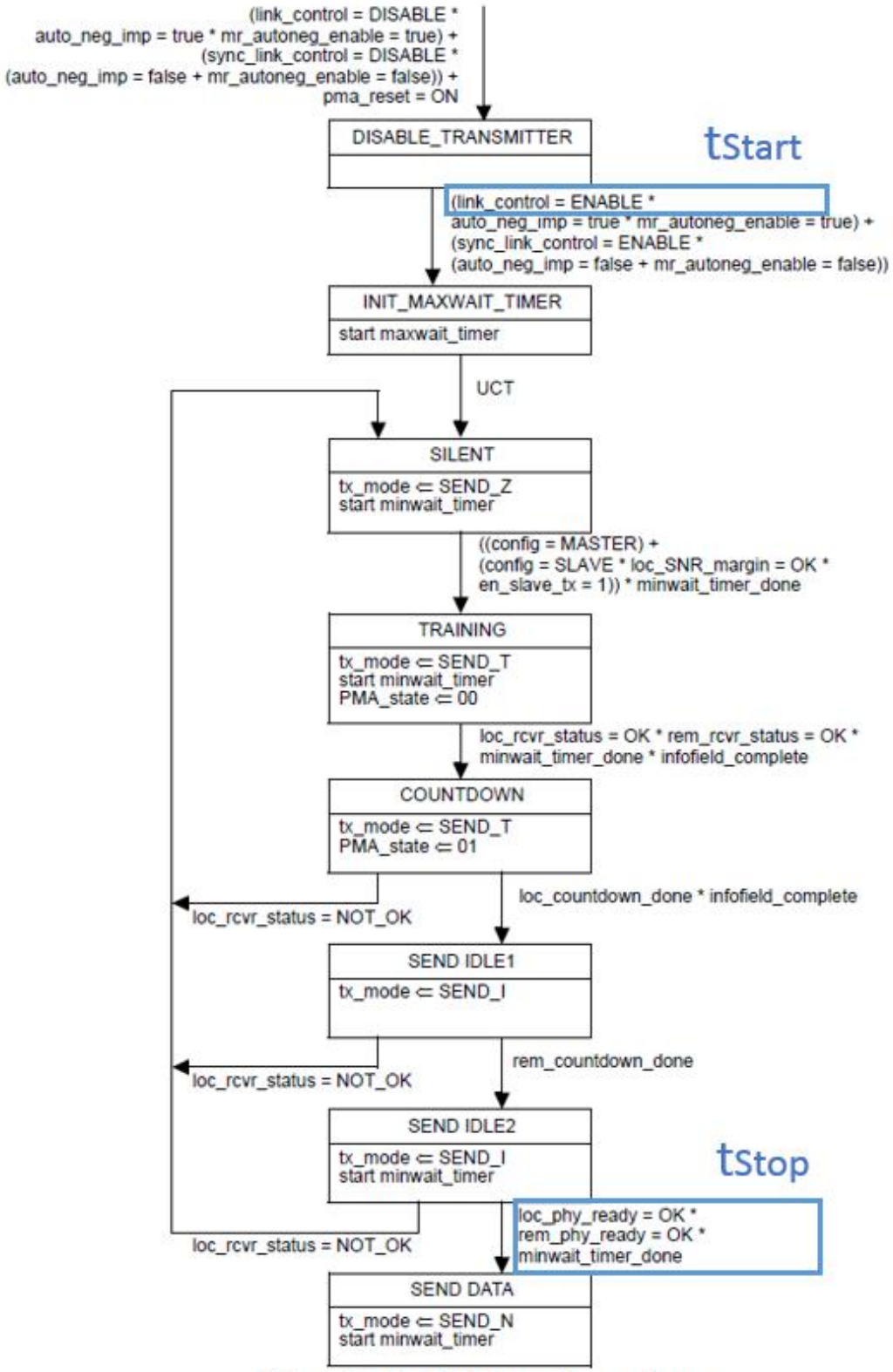

Figure 97–26—PHY Control state diagram

Figure 3 Definition of the start and end times for a determination of the start-up times of a 1000BASE-T1 link.

Register	LQ.LTT
Name	Link-training time
size[bits]	8

Bit	description
[7:0]	Information about the link training time of the last link training (lcl_rcv AND rem_rcv)

register value	explanation
0x00	0ms
0x01	1ms
…	
0x64	100ms
…	
0xFA	250ms
0xFB	more than 250ms
…	n/a
0xFF	measurement not possible

Table 9 Definition of LQ.LTT

6.3.2 Local receiver time (LRT)

Optional or mandatory feature: optional

The transceiver shall provide the time required until the local receiver is locked, in this context, the following time definitions apply (t_{Start} as in subclause 6.3.1):

- 1000BASE-T1
  Local Receiver Time (LRT)
  t_{stop}=>loc_phy_ready=OK

Register	LQ.LRT
Name	Local Receiver Time
size[bits]	8

Bit	description
[7:0]	Time until local_receiver = OK

register value	explanation
0x00	0ms
0x01	1ms
…	
0x64	100ms
…	
0xFA	250ms
0xFB	more than 250ms
…	n/a
0xFF	measurement not possible

Table 10 Definition of LQ.LRT register

6.3.3 Remote receiver time (RRT)

Optional or mandatory feature: optional

The transceiver shall provide the time required until the remote receiver is signalling that it is locked, in this context, the following time definitions apply (t_{Start} as in subclause 6.3.1):

- 1000BASE-T1
  Remote Receiver Time (RRT)
  $_{Tstop}$=> rem_phy_ready=OK

Register	LQ.RRT
Name	Remote Receiver Time
size[bits]	8

Bit	Description
[7:0]	Time until remote_receiver = OK

register value	Explanation
0x00	0ms
0x01	1ms
…	
0x64	100ms
…	
0xFA	250ms
0xFB	more than 250ms
…	n/a
0xFF	measurement not possible

Table 11 Definition of LQ.RRT register

6.3.4 Link Failures and Losses (LFL)

Optional or mandatory feature: mandatory

The PHY shall store the number of failures which occurred since the last power cycle but did not cause a link loss in a 10bit register.

The PHY shall store the number of link failures which occurred since the last power cycle in a 6bit register.

Register	LQ.LFL
Name	Link Failures and Losses
size[bits]	16

Bit	description
[9:0]	Number of Link Failures causing NOT a link loss (SSD failure, ESD failure, etc.) since last power cycle (0…1023)
[15:10]	number of Link Losses occurred since last power cycle (0…63)

register [9:0]	explanation
0x000	0 failure
0x001	1 failure
…	
0x3FE	1022 failures
0x3FF	1023 or more failures occurred

register [15:10]	explanation
0x00	0 link losses occurred
0x01	1 link loss occurred
…	
0x3E	62 link losses occurred
0x3F	63 or more link losses occurred

Table 12 Definition of LQ.LFL register

6.3.5 Communication ready status (COM)

Optional or mandatory feature: mandatory

The Communication_ready (Comm_ready) status is an optimized Link_Status information which shall be provided via the extended status register as information for higher layers to signal that from now on communication via the link is possible.

The optimized link status shall be defined by the comm ready status, when this meets the (comm_ready = link_status) the system will be confirmed as capable of communicating.

- 1000BASE-T1
  Comm_ready = link status

Register	LQ.COM
Name	Communication Ready Status
size[bits]	1

bit	Description
[0]	information on communication_ready

register [0]	Explanation
0	!(loc_phy_ready = OK * rem_phy_ready = OK)
1	loc_phy_ready = OK * rem_phy_ready = OK

Table 13 Definition of LQ.COM

6.4 Polarity Detection and Correction (POL)

6.4.1 Polarity Detection (DET)

Optional or mandatory feature: mandatory

Polarity detection, as well as their diagnostic accessibility (registers) shall be implemented in accordance with the specifications (1000BASE-T1).

6.4.2 Polarity Correction (COR)

Optional or mandatory feature: mandatory

Polarity correction, as well as their diagnostic accessibility (registers) shall be implemented in accordance with the specifications (1000BASE-T1).

(Feature must have option to enable and disable but needs to be supported)

6.5 Forward Error Correction Counter

6.5.1 FEC Counter Last Block (FLB)

Optional or mandatory feature: mandatory

The transceiver shall store the number of errors which occurred in a 10bit register, since the last power cycle.

Register	FEC.FLB
Name	Forward Error Correction Counter
size[bits]	10

Bit	description
[9:0]	Number of Frames captured (0…1023) Symbols to be counted up to 22 before error is captured.

register [9:0]	explanation
0x000	0 failure
0x001	1 failure
…	
0x3FE	1022 failures
0x3FF	1023 or more failures occurred

Table 14 Definition of FEC.FLB

6.5.2 FEC Counter Average 128 TX (FAV)

Optional or mandatory feature: mandatory

The transceiver shall store the average number of errors which occurred within 128 single values in a 10bit register.

Register	FEC.FAV
Name	Forward Error Correction Average
size[bits]	10

Bit	description
[9:0]	Number of frames captured (0…1023) Symbols to be counted up to 22 before error is captured.

register [9:0]	explanation
0x000	0 failure
0x001	1 failure
…	
0x3FE	1022 failures
0x3FF	1023 or more failures occurred

Table 15 Definition of FEC.FAV

6.5.3 FEC Counter Block Error (BLK)

Optional or mandatory feature: mandatory

The transceiver shall store the number of forward block errors which occurred within 128 single values in a 10bit register.

Register	FEC.BLK
Name	Forward Block Error Counter
size[bits]	10

Bit	description
[9:0]	Number of frames captured (0…1023) Symbols to be counted up to 22 before error is captured.

register [9:0]	explanation
0x000	0 failure
0x001	1 failure
…	
0x3FE	1022 failures
0x3FF	1023 or more failures occurred

Table 15 Definition of FEC.BLK