1000BASE-T1 Physical Coding Sublayer Test Suite

Version 1.0

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This suite of tests has been developed to help implementers identify problems that 1000BASE-T1 devices may have with the PCS functions.

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Restriction level history of Document

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Contents

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2 Introduction

2.1 Overview

This particular suite of tests has been developed to help implementers evaluate the functionality of the PCS sublayer of their 1000BASE-T1 device.

These tests are designed to determine if a product conforms to specifications defined in IEEE802.3 Clause 97. Successful completion of all tests contained in this suite does not guarantee that the tested device will operate with other devices. However, combined with satisfactory operation when tested in accordance with the OPEN Alliance 1000BASE-T1 Interoperability Test Suite, these tests provide a reasonable level of confidence that the Device Under Test (DUT) will function properly in many 1000BASE-T1 automotive environments.

The tests contained in this document are organized in such a manner as to simplify the identification of information related to a test, and to facilitate in the actual testing process. Tests are organized into groups, primarily in order to reduce setup time in the lab environment, however the different groups typically also tend to focus on specific aspects of device functionality. A three-part numbering system is used to organize the tests, where the first number indicates the section of the IEEE 802.3 Standard on which the test suite is based. The second and third numbers indicate the test’s group number and test number within that group, respectively. This format allows for the addition of future tests to the appropriate groups without requiring the renumbering of the subsequent tests.

2.2 Normative References

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEEE 802.3-2022

2.3 Terms and definitions

DUT	Device Under Test

3 Organization of Tests

The test definitions themselves are intended to provide a high-level description of the motivation, resources, procedures, and methodologies pertinent to each test.

3.1 Elementary Test Structure

Specifically, each test description consists of the following fields as shown in Table 3.1. A brief description of each field is provided.

Table 3.1 – Elementary Test Structure

Purpose	The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.
References	This section specifies source material *external* to the test suite, including specific subsections pertinent to the test definition, or any other references that might be helpful in understanding the test methodology and/or test results. External sources are always referenced by number when mentioned in the test description. Any other references not specified by number are stated with respect to the test suite document itself.
Resource Requirements	The requirements section specifies the test hardware and/or software needed to perform the test. This is generally expressed in terms of minimum requirements; however, in some cases specific equipment manufacturer/model information may be provided.
Discussion	The discussion covers the assumptions made in the design or implementation of the test, as well as known limitations. Other items specific to the test are covered here.
Test Setup	The setup section describes the initial configuration of the test environment. Small changes in the configuration should not be included here, and are generally covered in the test procedure section, below.
Test Procedure	The procedure section of the test description contains the systematic instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.
Observable Results	This section lists the specific observables that can be examined by the tester in order to verify that the DUT is operating properly. When multiple values for an observable are possible, this section provides a short discussion on how to interpret them. The determination of a pass or fail outcome for a particular test is generally based on the successful (or unsuccessful) detection of a specific observable.
Potential Issues	This section contains a description of known issues with the test procedure, which may affect test results in certain situations. It may also refer the reader to test suite appendices and/or whitepapers that may provide more detail regarding these issues.

3.2 DUT Requirements

For the purposes of this test suite, the DUT is one port of a 1000BASE-T1 capable device that includes a 1000BASE-T1 PHY mounted on a PCB with an MDI connector and any necessary circuitry such as a low pass filter or common mode choke. All tests will be performed at the MDI connector of the DUT.

Please see the additional requirements listed in table 3.2:

Table 3.2 –DUT Requirements

	Required Capabilities			
Test Number and Name	PCS Reset	GMII/LP(*1)	MDIO	Comment
Test PCS.97.1.1 – PCS Reset	✓	✓ (Observables a,c, e,g)		+ Config as Master & Slave + link_status indication
Test PCS.97.2.1 – Transmit Encoding				
Test PCS.97.2.2 – Side Stream Scrambling				+ Config as Master & Slave
Test PCS.97.2.3 – Control Codes		✓ (Part b, c)		Part c requires (R)GMII
Test PCS.97.3.1 – DISABLE_TRANSMITTER	✓			
Test PCS.97.3.2 – SEND_IDLES				
Test PCS.97.3.3 – SEND_DATA		✓		
Test PCS.97.4.1 – Receive Bit Order			✓	+ 3.2306 access (*2)
Test PCS.97.4.2 – Side Stream Descrambling				+ Config as Master & Slave
Test PCS.97.4.3 – Decoding		✓		
Test PCS.97.5.1 – RECEIVE_INIT		✓		Part a requires (R)GMII
Test PCS.97.5.2 – RECEIVE_DATA		✓	✓	+ 3.2306.6 access (*2)
Test PCS.97.6.1 – Verify Operation without high BER			✓	+ link_status indication + 3.2306 access (*3)
Test PCS.97.6.2 – Verify Operation in presence of low forced BER			✓	+ link_status indication + 3.2306 access (*3,4)
Test PCS.97.6.3 – HI_RFER not set when below limits			✓	+ link_status indication + 3.2306 access (*3,4)
Test PCS.97.6.4 – HI_RFER set when too many errors in window			✓	+ link_status indication + 3.2306 access (*3,4)
Test PCS.97.6.5 – HI_RFER set with consecutive errors			✓	+ link_status indication + 3.2306 access (*3)

(*1) GMII access equivalent or line-side loopback above the PCS but below any MAC if present
(*2) **Optional** MDIO register access or equivalent to read 3.2306.6 and 3.2306.7
(*3) **Optional** MDIO register access or equivalent to latching-high hi_rfer register bit (3.2306.7)
(*4) **Optional** MDIO register access or equivalent to RFER_count (3.2306.5:0)

4 Test Cases

The following test cases shall be performed on all 1000BASE-T1 PHYs.

4.1 GROUP 1: PCS Functions

This section verifies the integrity of the 1000BASE-T1 PCS Functions.

4.1.1 Test PCS.97.1.1 – PCS Reset

Purpose	To verify that the PCS properly initializes upon receipt of a reset request from the management entity, and links and passes frames as expected.
References	[1] IEEE 802.3 – 2022 Subclause 97.3.2.1 – PCS Reset function
Resource Requirements	1000BASE-T1 Test Station (refer to Appendix B) 1000BASE-T1 Monitor Station (refer to Appendix B) (R)GMII Test Station (refer to Appendix B) Management access to *link_status* and/or led indication of *link_status*
Discussion	Reference [1] states that the PCS is reset when power for the device containing the PMA has not yet reached the operating state, or upon the receipt of a reset request from management entity. The PCS Reset function should cause all state diagrams to take the open-ended pcs_reset branch upon execution of PCS Reset. PCS Reset is distinct from pma_reset, thus the behavior on the wire is undefined by the standard. This test will simply verify that if a pcs_reset can be performed; normal link operation resumes as expected. NOTE: A link interruption is allowed following a PCS reset. Any test frames sent while the link is down are not expected to be received or looped back.
Test Setup	Connect the DUT to the 1000BASE-T1 Test Station, the 1000BASE-T1 Monitor station and, if a suitable interface is exposed, the (R)GMII Test Station.
Test Procedure Part A	**Part A:** *DUT as MASTER properly reacts to a PCS Reset.* 1. Configure the DUT as MASTER. 2. Establish a link with the DUT. a. Send from the Transmit station valid link signaling such that *link_status* = OK is indicated by the DUT. 3. Monitor and decode transmissions from the DUT. a. If available, monitor and decode transmissions on the DUT’s GMII (or equivalent) receive path; otherwise, use the loopback described in (b) below. b. Enable a loopback which must loop received code groups from the line back to the transmitter. The loopback must include the PCS, but not include the MAC. 4. Send at least one frame from the Transmit station to the DUT to verify the DUT is operational. a. If possible, continue to send frames through the rest of this test. 5. Perform a PCS reset. If necessary, re-establish a link with the DUT. 6. Send at least one frame from the Transmit station to the DUT to verify the DUT is operational following the reset (or continue sending per step 4 above). 7. Monitor and decode transmissions from the DUT.

Observable Results for Part A	In step 2, a link should be established. In step 4, after a frame is sent the Monitoring station should receive a frame as observed either on the GMII equivalent interface, or via the loopback. In step 5, a link should be established (or remain established). In step 7, after a frame is sent the Monitoring station should receive a frame as observed either on the GMII equivalent interface, or via the loopback. When a frame is not being sent, the DUT should send IBLOCK_R up the GMII (or equivalent interface), if accessible.
Test Procedure Part B	**Part B:** *DUT as SLAVE properly reacts to a PCS Reset. {Note: this part is effectively identical to the MASTER case}* 8. Configure the DUT as SLAVE. 9. Establish a link with the DUT. a. Send from the Transmit station valid link signaling such that *link_status* = OK is indicated by the DUT 10. Monitor and decode transmissions from the DUT. a. If available, monitor and decode transmissions on the DUT's GMII (or equivalent) receive path; otherwise, use the loopback described in (b) below. b. Enable a loopback which must loop received code groups from the line back to the transmitter. The loopback must include the PCS, but not include the MAC. 11. Send at least one frame from the Transmit station to the DUT to verify the DUT is operational. a. If possible, continue to send frames through the rest of this test. 12. Perform a PCS reset. If necessary, re-establish a link with the DUT. 13. Send at least one frame from the Transmit station to the DUT to verify the DUT is operational following the reset (or continue sending per step 4 above). 14. Monitor and decode transmissions from the DUT. Configure the DUT as slave and repeat steps 2 through 7.
Observable Results for Part B	In step 9, a link should be established. In step 11, after a frame is sent the Monitoring station should receive a frame as observed either on the GMII equivalent interface, or via the loopback. In step 12, a link should be established (or remain established). In step 14, after a frame is sent the Monitoring station should receive a frame as observed either on the GMII equivalent interface, or via the loopback. When a frame is not being sent, the DUT should send IBLOCK_R up the GMII (or equivalent interface), if accessible.
Potential Issues	If the ability to control the PCS Reset request is not available, this test cannot be performed. Some devices may not allow configuration as master or slave, in which case only the supported configuration will be tested.

4.2 GROUP 2: PCS Transmit

This section verifies the integrity of the 1000BASE-T1 PCS Transmit function.

4.2.1 Test PCS.97.2.1 – Transmit Encoding

Purpose	To verify that the DUT correctly encodes RGMII transfers into 80B/81B blocks, performs RS-FEC encoding, and 3B2T to PAM3 mapping.
References	[1] IEEE 802.3 – 2022 Subclause 97.3.2.2.4 – Transmission order [2] IEEE 802.3 – 2022 Figure 97 – 5 – PCS Transmit bit ordering [3] IEEE 802.3 – 2022 Figure 97 – 7 – PCS detailed transmit bit ordering [4] IEEE 802.3 – 2022 Subclause 97.3.2.2.5 – Block structure [5] IEEE 802.3 – 2022 Subclause 97.3.2.2.11 – RS-FEC encoder [6] IEEE 802.3 – 2022 Equation 97 – 1 FEC encoder [7] IEEE 802.3 – 2022 Subclause 97.3.2.2.13 – 3B2T to PAM3 [8] IEEE 802.3 – 2022 Table 97 – 1 GMII control code mapping [9] IEEE 802.3 – 2022 Table 97 – 2 – 3B2T Mapping to PAM3
Resource Requirements	1000BASE-T1 Test Station (refer to Appendix B) 1000BASE-T1 Monitor Station (refer to Appendix B)
Discussion	The DUT should conform to the transmission order defined in [1], the transmit bit ordering defined in [2] and [3], the 81-bit block structure defined in [4], the RS-FEC encoding rules defined in [5], and the 3B2T to PAM3 mapping defined in [7] and [9].
Test Setup	Connect the DUT to the 1000BASE-T1 Test Station and the 1000BASE-T1 Monitor Station.
Test Procedure for Part A	***Part A:*** *DUT transmits Idle* 1. Establish a link with the DUT. 2. Cause the DUT to transmit an Idle stream to the test station. 3. Monitor and decode transmissions from the DUT.
Observable Results for Part A	a) In step 3, the DUT should be observed to transmit the Idle stream with the appropriate bit ordering, block structure, RS-FEC encoding, and 3B2T to PAM3 mapping.
Test Procedure for Part B	***Part B:*** *DUT encodes data with no errors* 4. Establish a link with the DUT. 5. Cause the DUT to transmit valid frames. 6. Monitor and decode transmissions from the DUT.
Observable Results for Part B	b) In step 6, the DUT should be observed to transmit the valid frames with the appropriate bit ordering, block structure, RS-FEC encoding, and 3B2T to PAM3 mapping.
Potential Issues	None.

4.2.2 Test PCS.97.2.2 – Side Stream Scrambling

Purpose	To verify that the DUT employs the scrambler polynomial defined in equation 97 – 3 when configured as MASTER and equation 97 – 4 when configured as SLAVE.
References	[1] IEEE 802.3 – 2022 Subclause 97.3.2.2.12 – PCS scrambler [2] IEEE 802.3 – 2022 Equation 97 – 3 – MASTER scrambler polynomial [3] IEEE 802.3 – 2022 Equation 97 – 4 – SLAVE scrambler polynomial [4] IEEE 802.3 – 2022 Figure 97 – 9 MASTER and SLAVE PCS scramblers
Resource Requirements	1000BASE-T1 Test Station (refer to Appendix B) 1000BASE-T1 Monitor Station (refer to Appendix B)
Discussion	The 1000BASE-T1 PCS uses a side stream scrambler to reduce correlation in transmitted data. The initial seed value for the MASTER and SLAVE scramblers are left up to the implementer with the exception that they shall be non-zero. The seed value is then transmitted to the link partner during the InfoField exchange. The scrambler is then run continuously on all PHY frame output bits.
Test Setup	Connect the DUT to the 1000BASE-T1 Test Station and the 1000BASE-T1 Monitor Station.
Test Procedure for Part A	***Part A:*** *Side stream scrambler polynomial* 1. Configure the DUT as MASTER. 2. Establish a link with the DUT. Causing the DUT to transmit an Idle stream to the testing station. 3. Monitor the transmissions from the DUT. 4. Configure the DUT as SLAVE and repeat steps 2 and 3.
Observable Results for Part A	a) The DUT should use the scrambler polynomial defined in 97 – 3 when configured as MASTER. The DUT should use the scrambler polynomial defined in 97 – 4 when configured as SLAVE.
Potential Issues	Some devices may not allow configuration as master or slave, in which case only the supported configuration will be tested.

4.2.3 Test PCS.97.2.3 – Control Codes

Purpose	To verify that the DUT properly encodes 81-bit blocks based on the control codes defined in [2].
References	[1] IEEE 802.3 – 2022 Table 35 – 1 – Permissible encoding of TXD<7:0>, TX_ER, and TX_EN [2] IEEE 802.3 – 2022 Subclause 97.3.2.2.5 – Block structure [3] IEEE 802.3 – 2022 Subclause 97.3.2.2.6 – Control codes [4] IEEE802.3 – 2018 Table 97 – 1 GMII control code mapping
Resource Requirements	1000BASE-T1 Test Station (refer to Appendix B) 1000BASE-T1 Monitor Station (refer to Appendix B) (R)GMII Test Station (refer to Appendix B)
Discussion	The 1000BASE-T1 PCS supports a subset of RGMII Control codes. Supported codes and their meanings are defined in [1], and [3]. The PCS conveys a Normal Inter-Frame control code (either 000 or 010 based on the loc_phy_ready variable) in the 80B/81B block code when the RGMII indicates TX_EN=0 and TXERR=0 or if the GMII is present, when TX_EN=0 and TX_ER=0. The PCS conveys a Transmit Error when the RGMII indicates TX_EN=1 and TXERR=1 or if the GMII is present, when TX_EN=1 and TX_ER=1. Per [3], any GMII encoding of Carrier Extend, Carrier Extend Error, or any Reserved encoding should be encoded as Normal Inter-Frame, which is examined in case 3. Note this test references TX_CTL, the RGMII signal formed from the multiplexing of TX_EN during the rising edge of the transmitter clock (TXC) and the TXERR signal sent during the falling edge of the TXC. If TX_EN=0 and TXERR=1 for one TXC cycle, TX_CTL is denoted "0,1". Patterns used in Part B are shown below for clarity: Initial pattern (Single error in all 10 81B positions):

	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9
1	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0
2	TX_ER=1	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0
3	TX_ER=0	TX_ER=1	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0
4	TX_ER=0	TX_ER=0	TX_ER=1	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0
5	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=1	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0
6	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=1	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0
7	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=1	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0
8	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=1	TX_ER=0	TX_ER=0	TX_ER=0
9	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=1	TX_ER=0	TX_ER=0
10	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=1	TX_ER=0
11	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=1

Second patter (single non-error in all 10 81B positions):

	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9
1	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0
2	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1
3	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1
4	TX_ER=0	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1
5	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1
6	TX_ER=1	TX_ER=0	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1
7	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1
8	TX_ER=1	TX_ER=1	TX_ER=0	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1
9	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1

10	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=0	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1
11	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1
12	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=0	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1
13	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1
14	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=0	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1
15	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1
16	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=0	TX_ER=1	TX_ER=1	TX_ER=1
17	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1
18	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=0	TX_ER=1	TX_ER=1
19	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1
20	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=0	TX_ER=1
21	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1
22	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=1	TX_ER=0
23	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0	TX_ER=0

Test Setup	Connect the DUT to the 1000BASE-T1 Test Station, the 1000BASE-T1 Monitor station and, if a suitable interface is exposed, the (R)GMII Test Station.
Test Procedure for Part A	**Part A:** *DUT transmits Normal Inter-Frame control code between frames* 1. Establish a link with the DUT. 2. Cause the DUT to transmit an Idle stream to the testing station, with at least 2 frames sent spaced at a minimum interframe gap (eg: 12 bytes). 3. Monitor and decode transmissions from the DUT.
Observable Results for Part A	a) The DUT should transmit the Normal Inter-Frame control code when not sending frame data.
Test Procedure for Part B	**Part B:** *DUT transmits the Transmit Error control code* 4. Establish a link with the DUT. 5. Cause the DUT to transmit frames with transmit errors; eg: TX_EN=TX_ER=1. a. The pattern stimulated should be at least a 110 byte frame consisting of 10 non-error bytes followed by 10 transmit errors, each spaced 11 bytes apart, such that all control code encodings of the 81B vector are stimulated. b. The pattern stimulated may be through direct GMII (or equivalent) access, or via loopback. The loopback must loop received code groups from the line back to the transmitter. The loopback must include the PCS, but not include the MAC. 6. Monitor and decode transmissions from the DUT. 7. Repeat steps 4 through 6 replacing the pattern with a 230 byte frame, consisting of 10 non-error bytes as the first and last 10 bytes of the frame, and a pattern, repeated 10 times, of 20 consecutive error bytes followed by 1 non-errored data byte. Thus stimulating the 81B vector's encoding of control and data words throughout all possible positions of single data byte encodings, and validating encoding of 81B vectors of all non-idle control words.
Observable Results for Part B	b) The DUT should transmit the appropriate Error symbol in place of a transmit error. Examining decoded 80B/81B blocks should show single transmit error locations in all positions (0 through 9) in the first iteration, and single data byte encodings in all positions (0 through 0) in the second iteration, along with entire 81B block encodings of control words (with RGMII control code 0b001).

Test Procedure for Part C	**Part C:** *DUT does not transmit reserved control codes* 8. Establish a link with the DUT. 9. If possible, cause the DUT to transmit an Idle stream with TXD<7:0> = 0F and: if RGMII: TX_CTL=0,1; and if GMII: TX_EN=0, TX_ER=1. 10. Monitor and decode transmissions from the DUT. 11. Repeat steps 8 and 9 but cause the DUT to transmit an Idle stream with TXD<7:0> = 1F and: if RGMII: TX_CTL=0,1; and if GMII: TX_EN=0, TX_ER=1. 12. Repeat steps 8 and 9 but cause the DUT to transmit an Idle stream with TXD<7:0> = 20 and: if RGMII: TX_CTL=0,1; and if GMII: TX_EN=0, TX_ER=1.
Observable Results for Part C	c) The DUT should encode the Carrier Extend, Carrier Extend Error, and Reserved control codes as Normal Inter-Frame.
Potential Issues	Test part B cannot be performed if access to a GMII equivalent interface is not provided, or an appropriate loopback is not available. Test part C cannot be performed if access to a GMII equivalent interface is not provided.

4.3 GROUP 3: PCS Transmit State Diagram

This section verifies the integrity of the 1000BASE-T1 PCS Transmit state diagram.

4.3.1 Test PCS.97.3.1 – DISABLE_TRANSMITTER

Purpose	To verify that the DUT properly behaves in the DISABLE_TRANSMITTER state.
References	[1] IEEE 802.3 – 2022 Figure 97 – 14 – PCS Transmit state diagram [2] IEEE 802.3 – 2022 Subclause 97.3.6.2.2 – Variables [3] IEEE 802.3 – 2022 Subclause 97.3.6.3 - Messages
Resource Requirements	1000BASE-T1 Test Station (refer to Appendix B) 1000BASE-T1 Monitor Station (refer to Appendix B)
Discussion	A 1000BASE-T1 device will enter the DISABLE_TRANSMITTER state upon a PCS Reset. PCS Reset is distinct from pma_reset, thus the behavior on the wire is undefined by the standard. This test will simply verify that if a pcs_reset can be performed, normal link operation resumes as expected, once the DUT has aggregated 10 RGMII transfers into tx_raw<99:0> the DUT will transition to the SEND_IDLES state.
Test Setup	Connect the DUT to the 1000BASE-T1 Test Station and the 1000BASE-T1 Monitor Station.
Test Procedure Part A	**Part A:** DUT transitions to SEND_IDLES 1. Establish a link with the DUT. a. Send from the Transmit station valid link signaling such that *link_status* = OK is indicated by the DUT. 2. Perform a PCS Reset on the DUT. If necessary, re-establish a link with the DUT. 3. Monitor transmissions from the DUT.
Observable Results for Part A	a) The DUT should begin transmitting IBLOCK_T following the PCS Reset. The DUT may also be observed to break and re-establish link.
Potential Issues	If the ability to control the PCS Reset request is not available, this test cannot be performed.

4.3.2 Test PCS.97.3.2 – SEND_IDLES

Purpose	To verify that the DUT properly behaves in the SEND_IDLES state.
References	[1] IEEE 802.3 – 2022 Figure 97 – 14 – PCS Transmit state diagram [2] IEEE 802.3 – 2022 Subclause 97.3.6.2.2 – Variables [3] IEEE 802.3 – 2022 Subclause 97.3.6.3 - Messages
Resource Requirements	1000BASE-T1 Test Station (refer to Appendix B) 1000BASE-T1 Monitor Station (refer to Appendix B) (R)GMII Test Station (refer to Appendix B)
Discussion	A 1000BASE-T1 device will enter the SEND_IDLES state when 10 successive RGMII transfers have been aggregated into tx_raw<99:0>. The DUT will remain in this state as long as tx_data_mode = FALSE. When tx_data_mode = TRUE and 10 successive RGMII transfers have been aggregated, the DUT will transition to the SEND_DATA state.
Test Setup	Connect the DUT to the 1000BASE-T1 Test Station, the 1000BASE-T1 Monitor station and, if a suitable interface is exposed, the (R)GMII Test Station.
Test Procedure Part A	***Part A:*** *DUT sends IBLOCK_T when in SEND_IDLES* 1. Establish a link with the DUT. a. Send from the Transmit station signaling indicating *rem_phy_ready* = NOT_OK. 2. Monitor transmissions from the DUT.
Observable Results for Part A	a) In step 2, after training, the DUT should transmit IBLOCK_T while in the SEND_IDLES state, observed by receive of Idle signaling at the Monitor station.
Test Procedure Part B	***Part B:*** *DUT transitions to SEND_DATA* 3. Establish a link with the DUT. a. Send from the Transmit station valid link signaling such that *link_status* = OK is indicated by the DUT. 4. Through any means (loopback, GMII stimulation, etc) stimulate frame transmission from the DUT. 5. Monitor transmissions from the DUT.
Observable Results for Part B	b) The DUT should begin transmitting the encoded version of tx_raw<99:0> as stimulated in step 4. As block alignment is unknown, the tx_raw vector should correspond to the expected frame data received by the DUT (either via GMII or via loopback).
Potential Issues	None.

4.3.3 Test PCS.97.3.3 – SEND_DATA

Purpose	To verify that the DUT properly behaves in the SEND_DATA state.
References	[1] IEEE 802.3 – 2022 Figure 97 – 14 – PCS Transmit state diagram [2] IEEE 802.3 – 2022 Subclause 97.3.6.2.2 – Variables [3] IEEE 802.3 – 2022 Subclause 97.3.6.3 - Messages
Resource Requirements	1000BASE-T1 Test Station (refer to Appendix B) 1000BASE-T1 Monitor Station (refer to Appendix B) (R)GMII Test Station (refer to Appendix B)
Discussion	A 1000BASE-T1 device will enter the SEND_DATA state when 10 successive RGMII transfers have been aggregated into tx_raw<99:0> and tx_data_mode = TRUE. The DUT will remain in this state as long as tx_data_mode = TRUE. When tx_data_mode = FALSE and 10 successive RGMII transfers have been aggregated, the DUT will transition to the SEND_IDLES state. Note that, once a 1000BASE-T1 device enters the SEND_N state (tx_data_mode=true) it cannot leave this state without going through SEND_Z and re-training, thus a “SEND_DATA” to “SEND_IDLES” state transition must also have a training sequence before observing the IBLOCK_T transmission while in the SEND_IDLES state.
Test Setup	Connect the DUT to the 1000BASE-T1 Test Station, the 1000BASE-T1 Monitor station and, if a suitable interface is exposed, the (R)GMII Test Station.
Test Procedure Part A	***Part A:*** *DUT Encodes tx_raw<99:0> and transmits properly* 1. Establish a link with the DUT. a. Send from the Transmit station valid link signaling such that *link_status* = OK is indicated by the DUT 2. Through any means (loopback, GMII stimulation, etc) stimulate frame transmission from the DUT. 3. Monitor transmissions from the DUT.
Observable Results for Part A	a) The DUT should transmit the encoded version of tx_raw<99:0>.
Test Procedure Part B	***Part B:*** *DUT transitions back to SEND_IDLES* 4. While in the link up state established in the first part of this test, cease transmitting from the Transmit station for at least one second. a. This may be achieved by breaking the link to the DUT, or stopping all transmissions from the Transmit station. 5. Establish a link with the DUT. a. Send from the Transmit station signaling indicating *rem_phy_ready* = NOT_OK. 6. Monitor transmissions from the DUT.
Observable Results for Part B	b) After training, the DUT should transmit IBLOCK_T while in the SEND_IDLES state.
Potential Issues	Cannot be performed if access to a GMII equivalent interface is not provided, or an appropriate loopback is not available.

4.4 GROUP 4: PCS Receive

This section verifies the integrity of the 1000BASE-T1 PCS Transmit state diagram.

4.4.1 Test PCS.97.4.1 – Receive Bit Order

Purpose	To verify that the DUT properly conforms to the receive bit order defined in [1]
References	[1] IEEE 802.3 – 2022 Figure 97 – 6 – PCS Receive bit ordering [2] IEEE 802.3 – 2022 Subclause 97.3.7.1 – Status
Resource Requirements	1000BASE-T1 Test Station (refer to Appendix B) 1000BASE-T1 Monitor Station (refer to Appendix B) Optional access to LL block_lock (3.2306.6) & LH hi_rfer bit (3.2306.7)
Discussion	Following training, the DUT should receive PAM3 symbols, demap and descramble them into RS-FEC frames, perform RS-FEC Decoding on these frames and group them into 81B blocks. When 45 81B blocks are aggregated, they are passed to the decoder function which decodes them into successive RGMII transfers. Block lock is indicated in MDIO register bit 3.2306.6, and high PHY frame error ratio (hi_rfer) is indicated in MDIO register bit 3.2306.7.
Test Setup	Connect the DUT to the 1000BASE-T1 Test Station and the 1000BASE-T1 Monitor Station.
Test Procedure Part A	***Part A:*** *Correct Bit Ordering* 1. Establish a link with the DUT. a. Send from the Transmit station valid link signaling such that *link_status* = OK is indicated by the DUT. b. When in SEND_N, send an Idle stream to the DUT with the correct bit ordering 2. If possible, read bit 3.2306.6 and 3.2306.7 at least twice. 3. By any method, observe if *link_status* = OK is indicated by the DUT.
Observable Results for Part A	a) The DUT should implement the received bit order as stated in [1] and establish synchronization and block lock. Report if the MDIO registers were read and properly indicate block lock and no hi_rfer. Note, reads of the Latching Low (LL) and Latching High (LH) MDIO registers may indicate no block_lock and hi_rfer initially, but subsequent reads should indicate block_lock and no hi_rfer.
Test Procedure Part B	***Part B:*** *Incorrect Bit Ordering* 4. Attempt to establish a link with the DUT. a. Send from the Transmit station link signaling such training is completed and SEND_I is reached by the DUT. b. When the 1000BASE-T1 Test Station is in SEND_N, send an Idle stream to the DUT with the incorrect bit ordering. 5. If possible, after step 4(b) above, read bit 3.2306.6 & 3.2306.7 at least twice. 6. By any method, observe if *link_status* = OK is indicated by the DUT.
Observable Results for Part B	b) The DUT should not indicate *link_status* = OK. Report if the MDIO registers were read and properly indicate no block_lock and hi_rfer.
Potential Issues	None.

4.4.2 Test PCS.97.4.2 – Side Stream Descrambling

Purpose	To verify that the DUT employs the descrambler polynomial defined in equation 97 – 4 when configured as MASTER and equation 97 – 3 when configured as SLAVE.
References	[1] IEEE 802.3 – 2022 Subclause 97.3.2.2.12 – PCS scrambler [2] IEEE 802.3 – 2022 Equation 97 – 3 – MASTER scrambler polynomial [3] IEEE 802.3 – 2022 Equation 97 – 4 – SLAVE scrambler polynomial [4] IEEE 802.3 – 2022 Figure 97 – 9 MASTER and SLAVE PCS scramblers
Resource Requirements	1000BASE-T1 Test Station (refer to Appendix B) 1000BASE-T1 Monitor Station (refer to Appendix B)
Discussion	The 1000BASE-T1 PCS uses a side stream scrambler to eliminate the correlation transmit data. The descrambler function uses the same polynomials used in the scrambling function. The PCS descrambles the data stream to generate the correct sequence of symbols for decoding and generation of RXD<7:0> to the RGMII. The initial seed value for the MASTER and SLAVE scramblers are left up to the implementer with the exception that they shall be non-zero.
Test Setup	Connect the DUT to the 1000BASE-T1 Test Station and the 1000BASE-T1 Monitor Station.
Test Procedure Part A	***Part A:*** *Side stream descrambler polynomial - MASTER* 1. Configure the DUT as MASTER. 2. Establish a link with the DUT. a. Send from the Transmit station valid link signaling such that *link_status* = OK is indicated by the DUT. 3. Monitor the transmissions from the DUT.
Observable Results for Part A	a) The DUT should use the descrambler polynomial defined in 97 – 4 when configured as MASTER.
Test Procedure Part B	***Part B:*** *Side stream descrambler polynomial - SLAVE* 4. Configure the DUT as SLAVE. 5. Establish a link with the DUT. a. Send from the Transmit station valid link signaling such that *link_status* = OK is indicated by the DUT. 6. Monitor the transmissions from the DUT.
Observable Results for Part B	b) The DUT should use the descrambler polynomial defined in 97 – 3 when configured as SLAVE.
Potential Issues	Some devices may not allow configuration as MASTER or SLAVE, in which case only the supported configuration will be tested.

4.4.3 Test PCS.97.4.3 – Decoding

Purpose	To verify that the DUT correctly performs PAM3 to 3B2T mapping, RS-FEC decoding, and decodes 80B/81B blocks into successive RGMII transfers.
References	[1] IEEE 802.3 – 2022 Subclause 97.3.2.2.4 – Transmission order [2] IEEE 802.3 – 2022 Figure 97 – 5 – PCS Transmit bit ordering [3] IEEE 802.3 – 2022 Figure 97 – 7 – PCS detailed transmit bit ordering [4] IEEE 802.3 – 2022 Subclause 97.3.2.2.5 – Block structure [5] IEEE 802.3 – 2022 Subclause 97.3.2.2.11 – RS-FEC encoder [6] IEEE 802.3 – 2022 Equation 97 – 1 [7] IEEE 802.3 – 2022 Subclause 97.3.2.2.13 – 3B2T to PAM3 [8] IEEE 802.3 – 2022 Table 97 – 1 GMII control code mapping [9] IEEE 802.3 – 2022 Table 97 – 2 – 3B2T Mapping to PAM3
Resource Requirements	1000BASE-T1 Test Station (refer to Appendix B) 1000BASE-T1 Monitor Station (refer to Appendix B) (R)GMII Test Station (refer to Appendix B)
Discussion	The DUT should conform to the transmission order defined in [1], the transmit bit ordering defined in [2] and [3], the 81-bit block structure defined in [4], the RS-FEC encoding rules defined in [5], and the 3B2T to PAM3 mapping defined in [7] and [9].
Test Setup	Connect the DUT to the 1000BASE-T1 Test Station, the 1000BASE-T1 Monitor station and, if a suitable interface is exposed, the (R)GMII Test Station.
Test Procedure Part A	***Part A:*** *DUT decodes valid 81B data blocks* 1. Establish a link with the DUT. 2. Transmit 81B blocks containing all data symbols to the DUT. 3. Monitor and decode transmissions from the DUT. a. If available, monitor and decode transmissions on the DUT's RGMII receive path; otherwise, use the loopback described in (b) below. b. Enable a loopback which must loop received code groups from the line back to the transmitter. The loopback must include the PCS, but not include the MAC.
Observable Results for Part A	a) The DUT should receive and decode all valid 81B data blocks.
Test Procedure Part B	***Part B:*** *DUT decodes valid 81B control blocks* 4. Establish a link with the DUT. a. Send from the Transmit station signaling indicating *rem_phy_ready* = NOT_OK. This is accomplished by transmitting 81B control blocks containing only the control code 000 to the DUT. 5. Monitor and decode transmissions on the DUT's receive path. a. If available, monitor and decode transmissions on the DUT's RGMII receive path; otherwise, use the loopback described in (b) below. b. Enable a loopback which must loop received code groups from the line back to the transmitter. The loopback must include the PCS, but not include the MAC. 6. Repeat steps 4 – 5 replacing the control code 000 with all other supported control codes defined in [8], as noted below: a. For control code 010, a valid link_status = OK is expected from the DUT.

	b. For control code 001, first establish a valid link (link_status = OK) then send error codes (control code 001). c. Control code 101 will not be sent in this version of the test suite. A future update may include support for Low Power Idle (LPI) modes.
Observable Results for Part B	b) The DUT should receive and decode all valid 81B control blocks.
Test Procedure Part C	***Part C:*** *DUT decodes 81B blocks with invalid pointer values* 7. Establish a link with the DUT. 8. Transmit 81B control blocks with an incorrect pointer value in the first 4 bits of the block. 9. Monitor and decode transmissions on the DUT's receive path. a. If available, monitor and decode transmissions on the DUT's RGMII receive path; otherwise, use the loopback described in (b) below. b. Enable a loopback which must loop received code groups from the line back to the transmitter. The loopback must include the PCS, but not include the MAC
Observable Results for Part C	c) The DUT should receive and decode the invalid control blocks and transmit error symbols on the RGMII receive path. If a loopback is enabled, the DUT should be observed to send one or more /E/ codes.
Test Procedure Part D	***Part D:*** *DUT decodes 81B blocks with invalid control codes* 10. Establish a link with the DUT. 11. Transmit 81B control blocks with a control code value that is not defined in [8]. 12. Monitor and decode transmissions on the DUT's receive path. a. If available, monitor and decode transmissions on the DUT's RGMII receive path; otherwise, use the loopback described in (b) below. b. Enable a loopback which must loop received code groups from the line back to the transmitter. The loopback must include the PCS, but not include the MAC 13. Repeat steps 14 – 16 with all other undefined control code values.
Observable Results for Part D	d) The DUT should receive and decode the invalid control blocks and transmit error symbols on the RGMII receive path. If a loopback is enabled, the DUT should be observed to send one or more /E/ codes.
Potential Issues	Test cannot be performed if access to a GMII equivalent interface is not provided, or an appropriate loopback is not available.

4.5 GROUP 5: PCS Receive State Diagram

This section verifies the integrity of the 1000BASE-T1 PCS Receive state diagram.

4.5.1 Test PCS.97.5.1 – RECEIVE_INIT

Purpose	To verify that the DUT properly behaves in the RECEIVE_INIT state.
References	[1] IEEE 802.3 – 2022 Figure 97 – 12 – PCS Receive state diagram [2] IEEE 802.3 – 2022 Subclause 97.3.6.2.2 – Variables [3] IEEE 802.3 – 2022 Subclause 97.3.6.3 - Messages
Resource Requirements	1000BASE-T1 Test Station (refer to Appendix B) 1000BASE-T1 Monitor Station (refer to Appendix B) (R)GMII Test Station (refer to Appendix B)
Discussion	A 1000BASE-T1 device will enter the RECEIVE_INIT state upon a PCS Reset. At which time it will begin sending control blocks containing all Idle symbols up the RGMII receive path. Once the DUT has aggregated 9 aligned Reed-Solomon symbols into rx_coded, the DUT will transition to the RECEIVE_DATA state. As training must be completed and the SEND_N state reached before frame (non-Idle) data can be received, this test will simply validate that the Test Station can link with the DUT and reception verified.
Test Setup	Connect the DUT to the 1000BASE-T1 Test Station, the 1000BASE-T1 Monitor station and, if a suitable interface is exposed, the (R)GMII Test Station.
Test Procedure Part A	***Part A:*** *DUT enters the RECEIVE INIT state* 1. Send no signaling to the DUT's 1000Base-T1 receiver (causing !block_lock) 2. Monitor the RGMII receive path on the DUT.
Observable Results for Part A	a) The DUT should begin sending control blocks up the GMII-equivalent receive path containing all Idle symbols in the RECEIVE_INIT state.
Test Procedure Part B	***Part B:*** *DUT transitions to the RECEIVE_DATA state* 3. Send no signaling to the DUT's 1000Base-T1 receiver (causing !block_lock) 4. Establish a link with the DUT. a. Send from the Transmit station valid link signaling such that *link_status* = OK is indicated by the DUT. b. As part of substep (a) above, the Transmit station will send a stream of valid Idle containing 9 aligned Reed-Solomon symbols to the DUT 5. Once link_status = OK, send a valid frame to the DUT. 6. Monitor the receive path on the DUT. a. If available, monitor and decode transmissions on the DUT's RGMII receive path; otherwise, use the loopback described in (b) below. b. Enable a loopback which must loop received code groups from the line back to the transmitter. The loopback must include the PCS, but not the MAC.
Observable Results for Part B	b) The DUT should enter the RECEIVE_DATA state and transmit the frame on the GMII-equivalent receive path to the MII test station, or if a loopback is in use, the frame should be observed on the transmit path from the DUT.
Potential Issues	In Part A, if access to a GMII equivalent interface is not provided, this test part cannot be performed. In Part B, this test cannot be performed if access to a GMII equivalent interface is not provided, or an appropriate loopback is not available.

4.5.2 Test PCS.97.5.2 – RECEIVE_DATA

Purpose	To verify that the DUT properly behaves in the RECEIVE_DATA state.
References	[1] IEEE 802.3 – 2022 Figure 97 – 12 – PCS Receive state diagram [2] IEEE 802.3 – 2022 Subclause 97.3.2.3 – PCS Receive function [3] IEEE 802.3 – 2022 Subclause 97.3.6.2.2 – Variables [4] IEEE 802.3 – 2022 Subclause 97.3.6.3 – Messages [5] IEEE 802.3 – 2022 Subclause 97.3.7.1 – Status
Resource Requirements	1000BASE-T1 Test Station (refer to Appendix B) 1000BASE-T1 Monitor Station (refer to Appendix B) (R)GMII Test Station (refer to Appendix B) Optional access to latching low block_lock (3.2306.6)
Discussion	A 1000BASE-T1 device will enter the RECEIVE_DATA state once the DUT has aggregated 9 aligned Reed-Solomon symbols into rx_coded. The DUT will then remain in the RECEIVE_DATA state until a PCS reset has occurred, the DUT will also return to the RECEIVE_INIT state if block_lock = FALSE or hi_rfer = TRUE.
Test Setup	Connect the DUT to the 1000BASE-T1 Test Station, the 1000BASE-T1 Monitor station and, if a suitable interface is exposed, the (R)GMII Test Station.
Test Procedure Part A	***Part A:*** *DUT remains in the RECEIVE_DATA state* 1. Perform a PCS Reset on the DUT, or break link with the DUT for ~1 s. 2. Establish a link with the DUT. a. Send from the Transmit station valid link signaling such that *link_status* = OK is indicated by the DUT. 3. Continue to send frames interspersed with valid Idle to the DUT. 4. Monitor the RGMII receive path on the DUT.
Observable Results Part A	a) The DUT should receive and decode received blocks containing decoded symbols based on the received 81B vector while in the RECEIVE_DATA state, observed either at the GMII equivalent, or by observing the same frame data emitted on the loopback transmit path.
Test Procedure Part B	***Part B:*** *DUT returns to the RECEIVE_INIT state via hi_rfer = TRUE* 5. Perform a PCS Reset on the DUT, or break link with the DUT for ~1 s. 6. Establish a link with the DUT. a. Send from the Transmit station valid link signaling such that *link_status* = OK is indicated by the DUT. 7. Begin sending enough invalid Reed-Solomon frames such that the DUT sets hi_rfer = TRUE. a. Send a repeating pattern of 16 consecutive invalid PHY frames followed by 72 valid PHY frames {to avoid setting block_lock=FALSE}. 8. Monitor the receive path on the DUT and, if accessible, the latching-high hi_rfer register bit (3.2306.7). a. If available, monitor and decode transmissions on the DUT's RGMII receive path; otherwise, use the loopback described in (b) below. b. Enable a loopback which must loop received code groups from the line back to the transmitter. The loopback must include the PCS, but not include the MAC.
Observable Results Part B	b) The DUT should emit at least one /E/ and up to 7200 /E/ bytes before entering the RECEIVE_INIT state when hi_rfer = TRUE and transmit control

	blocks containing all Idle symbols up the GMII-equivalent receive path. If observed via loopback, at least one /E/ should be observed transmitted from the DUT.
Test Procedure Part C	***Part C: DUT returns to the RECEIVE_INIT state via block_lock = FALSE*** 9. Perform a PCS Reset on the DUT, or break link with the DUT for ~1 s. 10. Establish a link with the DUT. a. Send from the Transmit station valid link signaling such that *link_status* = OK is indicated by the DUT. 11. Begin sending enough invalid Reed-Solomon frames such that the DUT sets block_lock = FALSE. a. 40 consecutive invalid PHY frames should be sufficient.[2] 12. Monitor the receive path on the DUT and, if accessible, the latching-low block_lock register bit (3.2306.6). a. If available, monitor and decode transmissions on the DUT's RGMII receive path; otherwise, use the loopback described in (b) below. b. Enable a loopback which must loop received code groups from the line back to the transmitter. The loopback must include the PCS, but not include the MAC.
Observable Results Part C	c) The DUT should enter the RECEIVE_INIT state when block_lock = FALSE and transmit control blocks containing all Idle symbols up the RGMII receive path.
Potential Issues	Test cannot be performed if access to a GMII equivalent interface is not provided, or an appropriate loopback is not available.

4.6 GROUP 6: RFER Monitor State Diagram

This section verifies the integrity of the 1000BASE-T1 RFER monitor state diagram.

4.6.1 Test PCS.97.6.1 – Verify Operation without high BER

Purpose	To verify that the DUT properly follows the RDER monitor state diagram when connected to the Transmit station with no intentional errors created.
References	[1] IEEE 802.3 – 2022 Figure 97 – 13 – RFER monitor state diagram [2] IEEE 802.3 – 2022 Subclause 97.3.6.2.2 – Variables [3] IEEE 802.3 – 2022 Subclause 97.3.6.2.4 – Counters [4] IEEE 802.3 – 2022 Subclause 97.3.6.3 – Messages [5] IEEE 802.3 – 2022 Subclause 97.3.7.1 – Status
Resource Requirements	1000BASE-T1 Test Station (refer to Appendix B) 1000BASE-T1 Monitor Station (refer to Appendix B) Management access to *link_status* and/or led indication of *link_status* Optional access to latching-high hi_rfer bit (3.2306.7)
Discussion	A 1000BASE-T1 device will enter the RFER_MT_INIT state upon a PCS Reset. At which time it will set hi_rfer = FALSE. The DUT will also enter the RFER_MT_INIT state when block_lock = FALSE. The DUT will then transition immediately to the INIT_CNT state. From there, the DUT will continue to examine received PHY Frames (RX_FRAME) and if no more than 15 out of 88 PHY Frames have errors, then hi_rfer will not be set TRUE and the link will remain up.
Test Setup	Connect the DUT to the 1000BASE-T1 Test Station and the 1000BASE-T1 Monitor Station.
Test Procedure Part A	***Part A:*** *DUT operates with Transmit station below the hi_rfer threshold.* 1. Perform a PCS Reset on the DUT, or break link with the DUT for ~1 s. 2. Establish a link with the DUT. a. Send from the Transmit station valid link signaling such that *link_status* = OK is indicated by the DUT. 3. If available, read bit 3.2306.7. 4. Continue to send valid link signaling for 10 seconds, or as along as tooling allows, if less than 10 seconds. 5. If available, read bit 3.2306.7.
Observable Results for Part A	a) If the DUT allows access to MDIO registers, the DUT should have 3.2306.7 = 0. And should remain at 0 throughout normal link from the Transmit station. The DUT should maintain link_status=OK after step 2 through the end of this test.
Potential Issues	If the DUT and the Transmit station cannot maintain a low BER connection, the validity of any test results from this test suite should be questioned until any underlying PMA issues are resolved and a low BER is observed in this test.

4.6.2 Test PCS.97.6.2 – Verify Operation in presence of low forced BER

Purpose	To verify that the DUT properly follows the RFER monitor state diagram when receiving a low rate of invalid PHY frames.
References	[1] IEEE 802.3 – 2022 Figure 97 – 13 – RFER monitor state diagram [2] IEEE 802.3 – 2022 Subclause 97.3.6.2.2 – Variables [3] IEEE 802.3 – 2022 Subclause 97.3.6.2.4 – Counters [4] IEEE 802.3 – 2022 Subclause 97.3.6.3 – Messages [5] IEEE 802.3 – 2022 Subclause 97.3.7.1 – Status
Resource Requirements	1000BASE-T1 Test Station (refer to Appendix B) 1000BASE-T1 Monitor Station (refer to Appendix B) (R)GMII Test Station (refer to Appendix B) Management access to *link_status* and/or led indication of *link_status* Optional access to latching-high hi_rfer bit (3.2306.7) & RFER_count (3.2306.5:0)
Discussion	A 1000BASE-T1 device will monitor its link BER via the RFER monitor state diagram. If more than 15 errored PHY frames are received within an 88 PHY frame window, then hi_rfer will be asserted and the link will drop. This test validates that the Transmit station can provide a low rate (<<15 for every 88) of errored PHY frames without causing the link to be dropped
Test Setup	Connect the DUT to the 1000BASE-T1 Test Station, the 1000BASE-T1 Monitor station and, if a suitable interface is exposed, the (R)GMII Test Station.
Test Procedure Part A	***Part A:*** *DUT maintains link when BER is below the error threshold.* 1. Perform a PCS Reset on the DUT, or break link with the DUT for ~1 s. 2. Establish a link with the DUT. a. Send from the Transmit station valid link signaling such that *link_status* = OK is indicated by the DUT. 3. If available, read bit 3.2306.7. 4. Continue to send link signaling for 10 seconds, or as along as tooling allows, if less than 10 seconds. Modify the link signaling as noted below: a. Send at least one invalid PHY frame, and if possible, send one invalid PHY frame every 88 PHY frames. 5. Monitor the receive path on the DUT and, if accessible, the latching-high hi_rfer register bit (3.2306.7) and 3.2306.5:0. a. If available, monitor and decode transmissions on the DUT's RGMII receive path; otherwise, use the loopback described in (b) below. b. Enable a loopback which must loop received code groups from the line back to the transmitter. The loopback must include the PCS, but not include the MAC.
Observable Results for Part A	a) In step 3, the DUT should indicate link_status = OK, and 3.2306.7 = 0 if accessible. In step 5, if accessible, 3.2306.7 should still be 0 and the link_status should still be OK on the DUT. If accessible, in step 5, the RFER_count (3.2306.5:0) should be non-zero, and if >63 invalid PHY frames have been sent, the value returned should be 0b111111. On the GMII equivalent, if available, /E/ codes should be seen, for each error'ed PHY frame sent (450 /E/ codes per errored PHY frame), or equivalent in encoded transmissions from the DUT if a loopback is used.
Potential Issues	None. {If no MDIO, GMII or loopback is available, then link_status will be monitored in this test}

4.6.3 Test PCS.97.6.3 – HI_RFER not set when below limits

Purpose	To verify that the DUT properly implements RFER_CNT_LIMIT and RFRX_CNT_LIMIT values.
References	[1] IEEE 802.3 – 2022 Figure 97 – 13 – RFER monitor state diagram [2] IEEE 802.3 – 2022 Subclause 97.3.6.2.2 – Variables [3] IEEE 802.3 – 2022 Subclause 97.3.6.2.4 – Counters [4] IEEE 802.3 – 2022 Subclause 97.3.6.3 – Messages [5] IEEE 802.3 – 2022 Subclause 97.3.7.1 – Status
Resource Requirements	1000BASE-T1 Test Station (refer to Appendix B) 1000BASE-T1 Monitor Station (refer to Appendix B) (R)GMII Test Station (refer to Appendix B) Management access to *link_status* and/or led indication of *link_status* Optional access to latching-high hi_rfer bit (3.2306.7) & RFER_count (3.2306.5:0)
Discussion	A 1000BASE-T1 device will monitor its received BER and set hi_rfer if more than 15 PHY frames are received in error within a window of 88 PHY frames. This test will validate that when only 15 errored PHY frames are received in a window of 88 PHY frames, the DUT will not set hi_rfer. Other tests (eg: 97.6.4 and 97.6.5) will verify that hi_rfer is set TRUE when 16 errored PHY frames are received within a window of 88 PHY frames.
Test Setup	Connect the DUT to the 1000BASE-T1 Test Station, the 1000BASE-T1 Monitor station and, if a suitable interface is exposed, the (R)GMII Test Station.
Test Procedure Part A	***Part A:*** *DUT maintains link when BER is just below the error threshold.* 1. Perform a PCS Reset on the DUT, or break link with the DUT for ~1 s. 2. Establish a link with the DUT. a. Send from the Transmit station valid link signaling such that *link_status* = OK is indicated by the DUT. 3. If available, read bit 3.2306.7. 4. Begin sending a sequence of invalid Reed-Solomon frames such that the DUT keeps hi_rfer = FALSE. a. Send a repeating pattern of 15 consecutive invalid PHY frames followed by 73 valid PHY frames. 5. Monitor the receive path on the DUT and, if accessible, the latching-high hi_rfer register bit (3.2306.7) and 3.2306.5:0. a. If available, monitor and decode transmissions on the DUT's RGMII receive path; otherwise, use the loopback described in (b) below. b. Enable a loopback which must loop received code groups from the line back to the transmitter. The loopback must include the PCS, but not include the MAC.
Observable Results for Part A	a) In step 3, the DUT should indicate link_status = OK, and 3.2306.7 = 0, if accessible. In step 5, if accessible, 3.2306.7 should still be 0 and the link_status should still be OK on the DUT. If accessible, in step 5, the RFER_count (3.2306.5:0) should be non-zero, and if >63 invalid PHY frames have been sent, the value returned should be 0b111111. On the GMII equivalent, if available, /E/ codes should be seen, for each error'ed PHY frame sent (450 /E/ codes per errored PHY frame), or equivalent in encoded transmissions from the DUT if a loopback is used.

Potential Issues	None. {If no MDIO, GMII or loopback is available, then link_status will be monitored in this test}

4.6.4 Test PCS.97.6.4 – HI_RFER set when too many errors in window

Purpose	To verify that the DUT properly implements RFRX_CNT_LIMIT as 88, as observed by seeing hi_rfer be set when 15 consecutive errors are sent in a repeating patten, spaced by only 72 valid PHY frames.
References	[1] IEEE 802.3 – 2022 Figure 97 – 13 – RFER monitor state diagram [2] IEEE 802.3 – 2022 Subclause 97.3.6.2.2 – Variables [3] IEEE 802.3 – 2022 Subclause 97.3.6.2.4 – Counters [4] IEEE 802.3 – 2022 Subclause 97.3.6.3 – Messages [5] IEEE 802.3 – 2022 Subclause 97.3.7.1 – Status
Resource Requirements	1000BASE-T1 Test Station (refer to Appendix B) 1000BASE-T1 Monitor Station (refer to Appendix B) (R)GMII Test Station (refer to Appendix B) Management access to *link_status* and/or led indication of *link_status* Optional access to latching-high hi_rfer bit (3.2306.7) & RFER_count (3.2306.5:0)
Discussion	A 1000BASE-T1 device will monitor its received BER and set hi_rfer if more than 15 PHY frames are received in error within a window of 88 PHY frames. The previous test (97.6.3) verifies that a pattern of 15 invalid PHY frames followed by 73 PHY frames does not cause hi_rfer to be set. This test will validate that the RFRX_CNT_LIMIT is not improperly set at 87, by sending one less valid PHY frame in the pattern sent by the previous test, and expecting hi_rfer to be set.
Test Setup	Connect the DUT to the 1000BASE-T1 Test Station, the 1000BASE-T1 Monitor station and, if a suitable interface is exposed, the (R)GMII Test Station.
Test Procedure Part A	***Part A:*** *DUT breaks link when BER is just above the error threshold.* 1. Perform a PCS Reset on the DUT, or break link with the DUT for ~1 s. 2. Establish a link with the DUT. a. Send from the Transmit station valid link signaling such that *link_status* = OK is indicated by the DUT. 3. If available, read bit 3.2306.7. 4. Begin sending a sequence of invalid Reed-Solomon frames such that the DUT keeps hi_rfer = TRUE. a. Send a repeating pattern of 15 consecutive invalid PHY frames followed by 72 valid PHY frames {violating the RFRX_CNT_LIMIT but avoids setting block_lock=FALSE}. 5. Monitor the receive path on the DUT and, if accessible, the latching-high hi_rfer register bit (3.2306.7) and 3.2306.5:0. a. If available, monitor and decode transmissions on the DUT's RGMII receive path; otherwise, use the loopback described in (b) below. b. Enable a loopback which must loop received code groups from the line back to the transmitter. The loopback must include the PCS, but not include the MAC.
Observable Results for Part A	a) The DUT should be observed to either SEND_Z or SEND_S following receipt of the pattern sent in step 4. The DUT should have bit 3.2306.7 set to 1. Note: The detection of hi_rfer=TRUE will cause the DUT to set pcs_status=NOT_OK, which will cause loc_phy_ready=NOT_OK which will cause the Link Monitor SM to transition to LINK_DOWN and set link_status=FAIL, which will then cause the PHY Link Synchronization SM to enter TRANSMIT_DISABLE and the DUT is then expected to emit either SEND_Z (if Slave) or SEND_S (if Master).

Potential Issues	None. {If no MDIO, GMII or loopback is available, then link_status will be monitored in this test}

4.6.5 Test PCS.97.6.5 – HI_RFER set with consecutive errors

Purpose	To verify that the DUT properly enters the HI_RFER state after receiving 16 consecutive errors.
References	[1] IEEE 802.3 – 2022 Figure 97 – 13 – RFER monitor state diagram [2] IEEE 802.3 – 2022 Subclause 97.3.6.2.2 – Variables [3] IEEE 802.3 – 2022 Subclause 97.3.6.2.4 – Counters [4] IEEE 802.3 – 2022 Subclause 97.3.6.3 – Messages [5] IEEE 802.3 – 2022 Subclause 97.3.7.1 – Status [6] IEEE 802.3 – 2022 Subclause 45.2.3.71 – 1000BASE-T1 PCS status 2 register
Resource Requirements	1000BASE-T1 Test Station (refer to Appendix B) 1000BASE-T1 Monitor Station (refer to Appendix B) (R)GMII Test Station (refer to Appendix B) Management access to *link_status* and/or led indication of *link_status* Optional access to latching-high hi_rfer bit (3.2306.7)
Discussion	A 1000BASE-T1 device will enter the HI_RFER state from the RFER_BAD_RF state when the rfer_cnt counter reaches a value of 16. The DUT will then set hi_rfer = TRUE. The DUT will then transition to the INC_CNT2 state if it receives a Reed-Solomon frame while rfrx_cnt < 88. If the rfrx_cnt counter = 88, the DUT will transition to the INIT_CNT state where both the rfrx_cnt and rfer_cnt counters are initialized to 0.
Test Setup	Connect the DUT to the 1000BASE-T1 Test Station, the 1000BASE-T1 Monitor station and, if a suitable interface is exposed, the (R)GMII Test Station.
Test Procedure Part A	***Part A:*** *DUT enters the HI_RFER state* 1. Perform a PCS Reset on the DUT, or break link with the DUT for ~1 s. 2. Establish a link with the DUT. a. Send from the Transmit station valid link signaling such that *link_status* = OK is indicated by the DUT. 3. Begin sending enough invalid Reed-Solomon frames such that the DUT sets hi_rfer = TRUE. a. Send a repeating pattern of 16 consecutive invalid PHY frames followed by 72 valid PHY frames {to avoid setting block_lock=FALSE}. 4. Monitor the receive path on the DUT and, if accessible, the latching-high hi_rfer register bit (3.2306.7). a. If available, monitor and decode transmissions on the DUT's RGMII receive path; otherwise, use the loopback described in (b) below. b. Enable a loopback which must loop received code groups from the line back to the transmitter. The loopback must include the PCS, but not include the MAC.
Observable Results for Part A	a) The DUT should be observed to either SEND_Z or SEND_S following receipt of the pattern sent in step 4. The DUT should have bit 3.2306.7 set to 1. Note: The detection of hi_rfer=TRUE will cause the DUT to set pcs_status=NOT_OK, which will cause loc_phy_ready=NOT_OK which will cause the Link Monitor SM to transition to LINK_DOWN and set link_status=FAIL, which will then cause the PHY Link Synchronization SM to enter TRANSMIT_DISABLE and the DUT is then expected to emit either SEND_Z (if Slave) or SEND_S (if Master).
Potential Issues	None. {If no MDIO, GMII or loopback is available, then link_status will be monitored in this test}

5 Appendices

5.1 Appendix A –Testing Devices Without RGMII Access

Purpose: To detail the tests that can be performed on a device without RGMII (or any equivalent GMII), access and to detail the modifications to the Procedures and Observable Results.

Discussion: The amount of tests that can be performed on a device without RGMII access is reduced. Typically, the only observation points that will be available packet counters or packets that are forwarded through another port on the DUT. Also, the only transmissions available from the DUT will be Training, Idle, and packets. The following table lists all tests and if they are possible with or without modification. The necessary modifications are detailed in the following sections.

Test Name	Test Number	No Modification Required	Requires Modification	Cannot be Tested
Group 1: PCS Functions				
PCS Reset	Test 97.1.1	All Parts		
Group 2: PCS Transmit				
Transmit Encoding	Tests 97.2.1	All Parts		
Side Stream Scrambling	Tests 97.2.2	All Parts		
Control Codes	Tests 97.2.3	a,b		c
Group 3: PCS Transmit State Diagram				
DISABLE_TRANSMITTER	Test 97.3.1	All Parts		
SEND_IDLES	Test 97.3.2	All Parts		
SEND_DATA	Test 97.3.3	All Parts		
Group 4: PCS Receive				
Receive Bit Order	Test 97.4.1	All Parts		
Side Stream Descrambling	Test 97.4.2	All Parts		
Decoding	Test 97.4.3	All Parts		
Group 5: PCS Receive State Diagram				
RECEIVE_INIT	Test 97.5.1	b		a
RECEIVE_DATA	Test 97.5.2	All Parts		
Group 6: RFER Monitor State Diagram`				
RFER_MT_INIT	Test 97.6.1	All Parts		
INIT_CNT	Test 97.6.2	All Parts		
INC_CNT	Test 97.6.3	All Parts		
RFER_BAD_RF	Test 97.6.4	All Parts		
HI_RFER	Test 97.6.5	All Parts		
GOOD_RFER	Test 97.6.6	All Parts		

Table A. 1 - Tests that are possible without RGMII access

At this time, all proposed test procedures incorporate GMII (or equivalent) procedures, and if not available, may require a line-side loopback (one that would copy data received from the line through the PCS Receiver back to the PCS Transmitter). Such a loopback must be between the PCS and any MAC present in the DUT. A loopback at the GMII is acceptable but may have timing implications.

5.2 Appendix B – Test Stations

Purpose: To provide the requirements of the test stations used during 1000BASE-T1 PHY Control testing.

Discussion:

Two to Three test stations will be required to perform all tests that are specified in this document, depending on DUT capabilities.

The **1000BASE-T1 Test Station** emulates a compliant 1000BASE-T1 PHY, with testability features to perform controlled negative test cases (eg: cease transmission, keep loc_rcvr_status indications as NOT_OK, etc) as required by the tests in this test plan. The 1000BASE-T1 Test Station also has external triggering capability to align events observed by the 1000BASE-T1 Test Station with those observed by the 1000BASE-T1 Monitor Station.

The **1000BASE-T1 Monitor Station** would typically consist of an oscilloscope and software to capture and decode the transmissions from the DUT. The DUT will connect through the Line Tap as specified in appendix 5.2 B. The software will download the capture from the oscilloscope and decode the symbols, using knowledge of the 1000BASE-T1 encoding.

The **(R)GMII Test Station** is required for some tests, if the DUT exposes a supported interface (typically RGMII, following the Samtec connector and pinout employed by the 1000BASE-T1 Interoperability Test Plan). While some tests can be performed with either loopback enabled, or the (R)GMII Test Station, use of the (R)GMII Test Station is generally preferred unless indicated otherwise in the specific test.

Figures A - 1 and A - 2 below show the typical test setups with a DUT with an exposed (R)GMII interface in Figure A – 1, or configured with a line-side loopback, as shown in Figure A – 2.

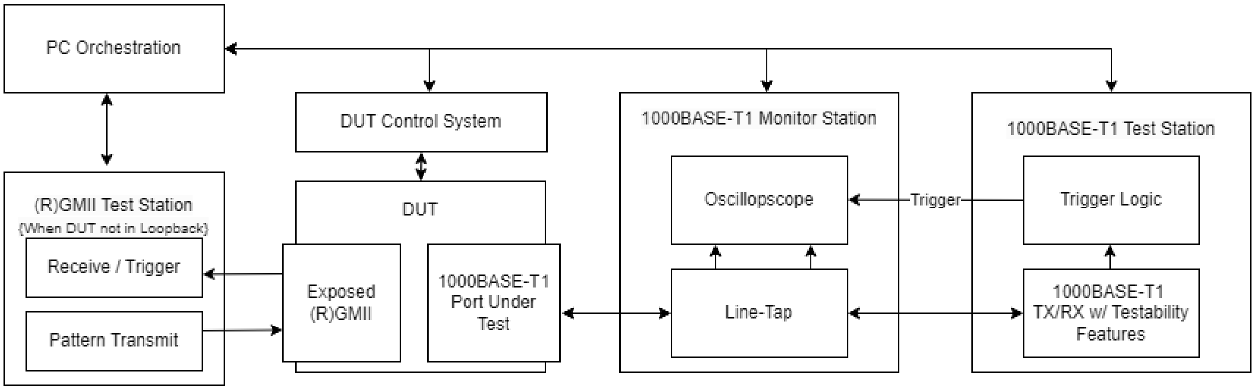

Figure A - 1: 1000BASE-T1 Test Setup with RGMII Test Station

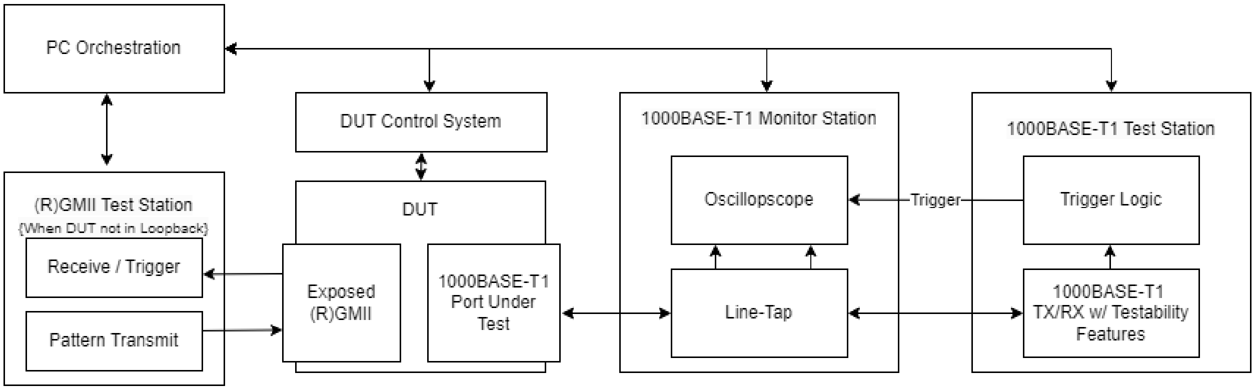

Figure A - 2: 1000BASE-T1 Test Setup with Loopback

Figure A – 3 shows the potential to test a multi-port DUT that has no exposed RGMII interface. Any equivalent setup is acceptable (eg: two 1000BASE-T1 Test Stations, substituted for the compliant 1000BASE-T PHY and (R)GMII Test Station). The test plan does not explicitly refer to this test setup but multi-port DUTs (with 2 or more ports operating at 1000 Mbps) can be tested by such as setup where the test plan's (R)GMII Test Station is driving traffic into (or monitoring traffic from) the 1000Mbps port not under test.

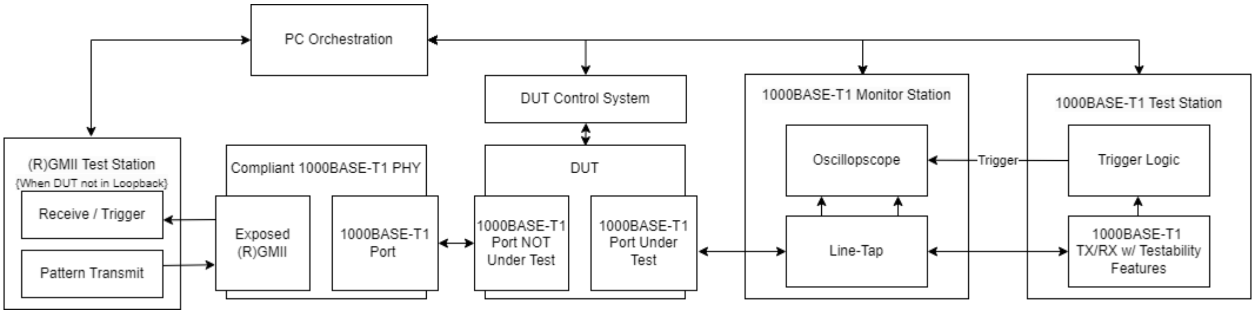

Figure A - 3: 1000BASE-T1 Test Setup with multi-port 1000BASE-T1 (eg: no exposed RGMII)

5.3 Appendix C – Line Tap

Purpose: To provide the requirements of a line tap that will be used, in conjunction with an oscilloscope, to capture the transmissions from the DUT.

Discussion:

Any directional line tap capable of providing a low insertional loss impedance matched channel connection with at least 500MHz bandwidth has been shown to be functional for short reach (~2 meter) connections between the Test Station and DUT. Additional bandwidth is recommended. A minimum of 8GSps sampling with a 10bit oscilloscope is recommended. Care should be taken to ensure cabled connections to the oscilloscope are on equal-length cables and that the directional taps do not provide substantial asymmetry in monitored paths.

Delays from the Line-Tap to the DUT should be considered in those tests that may be impacted by such propagation delays.