Advanced diagnostic features for 10BASE-T1S automotive Ethernet PHYs Specification

TC14 – advanced PHY features

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4 INTRODUCTION

This specification describes advanced features of a 10BASE-T1S automotive Ethernet PHY (often also called transceiver), e.g. for diagnostic purposes for automotive Ethernet Phis

5 ABBREVIATION/SYMBOLS

AWG noise	Added White Gaussian noise
BER	Bit Error Rate
CRC	Cyclic Redundancy Check
DCQ	Dynamic Channel Quality
DigPHY	PHY without analog PMA portion which is left into a separate chip (i.e., the PMD transceiver)
ED	Energy Detect
HDD	Harness defect detection
MDI	Medium Dependent Interface
OSD	OPEN/SHORT detection
PHY	PHY is a Physical layer interface device, often called transceiver
SNR	Signal Noise Ratio
SQI	Signal Quality Index (8 levels)
SQI+	Signal Quality Index (8 up to 256 levels)
TOID	Transmit Opportunity ID

6 SCOPE

The objective of this document is to provide a standard set of Advanced PHY features for 10BASE-T1S implementations.

7 NORMATIVE REFERENCES

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

[1] IEEE Std 802.3™ - 2022, IEEE Standard for Ethernet

[2] OPEN Alliance : 10BASE-T1S PMD Transceiver Interface

[3] OPEN Alliance : 10BASE-T1S Physical Media Attachment Test Suite

[4] OPEN Alliance : 10BASE-T1S Half-Duplex Interoperability Test Suite

[5] OPEN Alliance : 10BASE-T1S System implementation specification

8 TERMS AND DEFINITIONS

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- ISO Online browsing platform: available at https://www.iso.org/obp
- IEC Electropedia: available at http://www.electropedia.org/

Node term definition:

End Node	A node that is at either end of a mixing segment. There are no other nodes between the End Node and the 100Ω edge termination. The End Node may contain the 100Ω edge termination.
Drop Node	Any node that is located between the two end nodes
Coordinator	This is the node configured as aPLCALocalNodeID=0 that is responsible for the periodic transmission of the BEACON and configuring the number of transmit opportunities between each BEACON.
Follower	Followers are any nodes configured as aPLCALocalNodeID=1..254. They synchronize their transmit opportunity counter with the reception of the periodic BEACON transmitted by the coordinator
Head Node	This is the highest-level application node on the mixing segment. It typically implements a switch or gateway access to the core network beyond the bus segment.

Note:
It is expected that each segment includes two end nodes, one coordinator and one head node.

9 OVERVIEW

10BASE-T1S automotive Ethernet transceivers (PHY or every PHY port of a switch) shall offer the information specified below for diagnostic purposes.

group	group name	parameter	parameter name	Description	remarks
ADFCAP	Advanced diagnostic features capability	HDD	HDD capability	Indication of HDD capability and of supported HDD class (HDDx; x= 1;2..)	3)
		SQI+	SQI+ capability	Indication of SQI+ capability and of used bits for the SQI+ value.	
		SQI	SQI capability	Indication of SQI capability.	
HDD	Harness defect detection	HDD_CTRL	HDD control	Ctrl. Bit for enabling request of HDD function.	2) 3)
		HDD_READY	HDD Ready	Status feedback	2) 3)
		START_CTRL	Start measurement	Ctrl. Bit for starting Measurement and indication bit for Measurement in progress.	2) 3)
		VALID	Measurement results ready and valid	Indication bit for measurement results ready and valid.	2) 3)
		SHORT_ OPEN_ST	Bus short/open status	Indication bit for bus short/open condition detected	2) 3)
DCQ	Dynamic channel quality is applicable for PHY.	TOID	SQI/SQI+ Transmit Opportunity ID	The SQI/SQI+ value is determined for only a specific transmitting node as identified by the PLCA transmit opportunity as configured in TOID	
		SQI.UPDATE	SQI Update Indication	SQI was updated since last read.	
		SQI	Signal Quality Index	Current SQI value. A classification of the signal quality with 8 levels	1)
		SQI+.UPDATE	SQI+ Update Indication	SQI was updated since last read.	
		SQI+	Signal Quality Index Plus	Current SQI+ value. A classification of the signal quality with 8 up to 256 levels.	

Table 1: Overview of required PHY parameters to be stored and provided via Register fields

Remarks to Table 1:

1) "The SQI levels, at least 8 (3 bits), have a recommended correlation to BER as shown in Table 19 and for jitter ≤ 15ns @MDI (see [5]) the SQI value shall be ≥ 3."

2) Diagnostic function is only available in special “diagnostic” mode, not on the fly.

3) For PMD Transceiver, HDD function may be located in PMD Transceiver. In this case, the HDD capability and control registers should be at location x04 and x05 of PMD Transceiver. If HDD function is located in digPHY, the HDD capability and control registers are at location xCC00 and xCC01.

9.1 Advanced Diagnostic features capability (ADFCAP)

Before defining the different diagnostic features like HDD (Harness defect detection) and SQI (Signal Quality Index), it makes sense to define the capability a PHY can support and where this information is available."

For supporting most of system implementation requirements, HDD and SQI diagnostic features were split into diagnostic subclasses.

In this document four diagnostic classes for HDD are defined: HDD1, HDD2, HDD3, HDD4; and two diagnostic classes for SQI are defined: SQI and SQI+."

Due to various diagnostic functions and their subclasses, in Table 2 the capability register is shown in which the PHY information of supported diagnostic classes are accessible.

Register Name	ADFCAP
Description	Advanced diagnostic features capability
size[bits]	16
MMD	31
Addr/Offset	0xCC00/0 *

*In case PMD Transceiver is used for diagnostics in this specification the capability register shall be at location x04 of PMD Transceiver.

15	14	13	12	11	10	9	8
Reserved					**HDD**		
RO					RO		
7	6	5	4	3	2	1	0
Reserved			**SQI+**				**SQI**
RO			RO				RO

Bit(s)	Name	Description	Access
15:11	Reserved	Reserved (Default = 0)	RO

10:8	HDD	**Harness Defect Detection capability** 0 – HDD is not supported X – HDD class X is supported	RO
7:5	Reserved	Reserved (Default = 0)	RO
4:1	SQI+	**SQI+ capability** 0 – SQI+ is not supported X – SQI+ is supported using X bits	RO
0	SQI	**SQI capability** 0 – SQI is not supported 1 – SQI is supported	RO
RO = read-only, RW = read-write, SC = self-clearing			

Table 2: Definition of ADFCAP register

9.1.1 HDD class capability

Harness Defect Detection capability information for supported HDD class.

Field Name	ADFCAP.HDD
Description	Harness Defect Detection capability
size[bits]	3
MMD	31
Addr/Offset	0xCC00 / 8 *

*In case PMD Transceiver is used for diagnostics in this specification the capability register shall be at location x04 of PMD Transceiver.

Field value	Explanation (ADFCAP.HDD)
0x0	0 - HDD is not supported
0x1	1 – HDD1 (HDD class 1 is supported)
0x2	2 – HDD2 (HDD class 2 is supported)
0x3	3 – HDD3 (HDD class 3 is supported)
0x4	4 – HDD4 (HDD class 4 is supported)
0x5	Reserved
0x6	Reserved
0x7	Reserved

Table 3: Definition of HDD field in the ADFCAP register

9.1.2 SQI+ class capability

SQI+ capability information for supported SQI+ class and used numbers of bits.

Field Name	ADFCAP.SQI+
Description	SQI+ capability
size[bits]	4
MMD	31
Addr/Offset	0xCC00 / 1

Field value	Explanation (ADFCAP.SQI+)
0x0	0 – SQI+ is not supported
0x1	Reserved
0x2	Reserved
0x3	3 – SQI+ is supported, using 3 bits (8 levels)
0x4	4 – SQI+ is supported, using 4 bits (16 levels)
0x5	5 – SQI+ is supported, using 5 bits (32 levels)
0x6	6 – SQI+ is supported, using 6 bits (64 levels)
0x7	7 – SQI+ is supported, using 7 bits (128 levels)
0x8	8 – SQI+ is supported, using 8 bits (256 levels)
0x9	Reserved
0xA	Reserved
0xB	Reserved
0xC	Reserved
0xD	Reserved
0xE	Reserved
0xF	Reserved

Table 4: Definition of SQI+ field in the ADFCAP register

9.1.3 SQI class capability

SQI+ capability information for supported SQI class of the used PHY

Field Name	ADFCAP.SQI
Description	SQI capability
size[bits]	1
MMD	31

Addr/Offset	0xCC00 / 0

Field value	Explanation (ADFCAP.SQI)
0x0	0 – SQI is not supported
0x1	1 – SQI is supported, using 3 bits (8 levels)

Table 5: Definition of SQI field in the ADFCAP register

9.2 Harness Defect Detection (HDD)

There shall be a possibility to detect harness defects. This can either be done during normal operation (as long as possible) or in a specific host-triggered diagnostic mode.

This procedure should be controlled via defined registers. Before the procedure is started, all other nodes connected to the same line should be prevented from any transmission.

Figure 1 shows an overview of all possible short circuits and open wire states including differential end termination mismatch. The physical positions are to be understood as examples. Based on this image, the following Table 6 shows which errors can be generated:

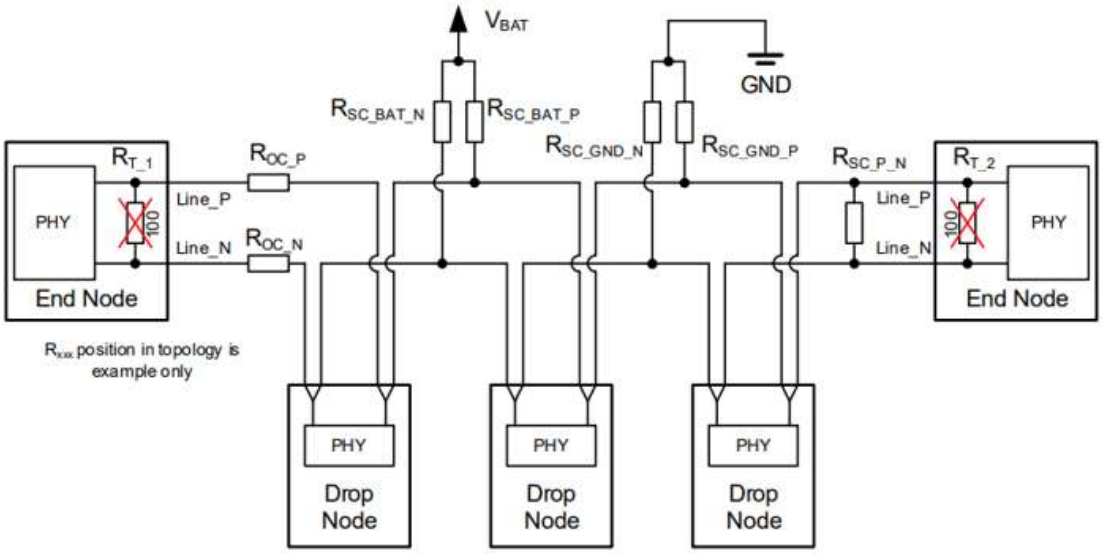

Figure 1: Overview of possible harness defects.

Table 6 is showing the Bus Failure Matrix, indicating which combinations of failures and environmental conditions belongs to which HDD diagnostic.

	R_{OC_P}	R_{OC_N}	$R_{SC\_BAT\_P}$	$R_{SC\_BAT\_N}$	$R_{SC\_GND\_P}$	$R_{SC\_GND\_N}$	$R_{SC\_P\_N}$	R_{T_1}	R_{T_2}
Fault 1: Single Wire Open P	R	0						100	100
Fault 2: Single Wire Open N	0	R						100	100
Fault 3: Double Wire Open	R	R						100	100
Fault 4: Single Wire Short BAT P	0	0	R					100	100
Fault 5: Single Wire Short BAT N	0	0		R				100	100
Fault 6: Single Wire Short GND P	0	0			R			100	100
Fault 7: Single Wire Short GND N	0	0				R		100	100
Fault 8: Short P to N	0	0					R	100	100
Fault 9: Double Wire Short to BAT	0	0	R				0	100	100
Fault 10: Double Wire Short to GND	0	0			R		0	100	100
Fault 11: Single Termination Missing	0	0						100	
	0	0							100
Fault 12: Double Termination Missing	0	0							

Table 6: Bus Failure Matrix

9.2.1 HDD classes with their resistive thresholds

The supported failure cases of each HDD class with its resistive thresholds are given in Table 7.

The defined resistive thresholds are relating only to the physical channel, consisting of PCB plugs, contacts, wire, and inline connectors.

From a PHY perspective, the impact of series coupling capacitors and of further components for example CMC, ESD, 1.5 kΩ CMT (common mode termination) have to be considered at the PHY HDD implementation in addition to that given resistive threshold limits.

	HDD Class 1 Open / Short		**HDD Class 2** SW Open / Short		**HDD Class 3** SW Open / SW Short		**HDD Class 4** SW Open / SW Short	
Failure Case	**HARD**				**WEAK**			
Reporting:	**OK**	**FAIL**	**OK**	**FAIL**	**OK**	**FAIL**	**OK**	**FAIL**
Open of both wires	$R_{OC} \le 2.5\ \Omega$	$R_{OC} \ge 100\ k\Omega$	$R_{OC} \le 2.5\ \Omega$	$R_{OC} \ge 100\ k\Omega$	$R_{OC} \le 20\ \Omega$	$R_{OC} \ge 100\ \Omega$	$R_{OC} \le 20\ \Omega$	$R_{OC} \ge 100\ \Omega$
Short of both wires to GND or VBAT	$R_{SC} \ge 100\ k\Omega$	$R_{SC} \le 10\ \Omega$ *	$R_{SC} \ge 100\ k\Omega$	$R_{SC} \le 10\ \Omega$ *	$R_{SC} \ge 10\ k\Omega$	$R_{SC} \le 1\ k\Omega$ *	$R_{SC} \ge 10\ k\Omega$	$R_{SC} \le 1\ k\Omega$ *
Short of both wires	$R_{SC} \ge 100\ k\Omega$	$R_{SC} \le 10\ \Omega$	$R_{SC} \ge 100\ k\Omega$	$R_{SC} \le 10\ \Omega$	$R_{SC} \ge 1\ k\Omega$	$R_{SC} \le 100\ \Omega$	$R_{SC} \ge 1\ k\Omega$	$R_{SC} \le 100\ \Omega$
Open of single wire or Single Termination lost	Not req.	Not req.	$R_{OC} \le 2.5\ \Omega$	$R_{OC} \ge 100\ k\Omega$	$R_{OC} \le 20\ \Omega$	$R_{OC} \ge 100\ \Omega$	$R_{OC} \le 20\ \Omega$	$R_{OC} \ge 100\ \Omega$
Third Termination	Not req.	Not req.	Not req.	Not req.	$R_{SC} \ge 1\ k\Omega$	$R_{SC} \le 100\ \Omega$	$R_{SC} \ge 1\ k\Omega$	$R_{SC} \le 100\ \Omega$
No Termination	Not req.	Not req.	Not req.	Not req.	Not req.	Not req.	$R_{OC} \le 20\ \Omega$	$R_{OC} \ge 100\ \Omega$
Short of single wire to GND or VBAT	Not req.	Not req.	Not req.	Not req.	Not req.	Not req.	$R_{SC} \ge 10\ k\Omega$	$R_{SC} \le 1\ k\Omega$

*($R_{SC\_PN} < 10\ \Omega$)
Short circuit voltage range is implementation specific and shall at least support 2V GND shift and up to 18V Battery supply

Table 7: HDD classes with their supported failure cases included.

Figure 2 shows a simple summary of Table 7 with comparison of “hard / weak” failure with its resistive thresholds.

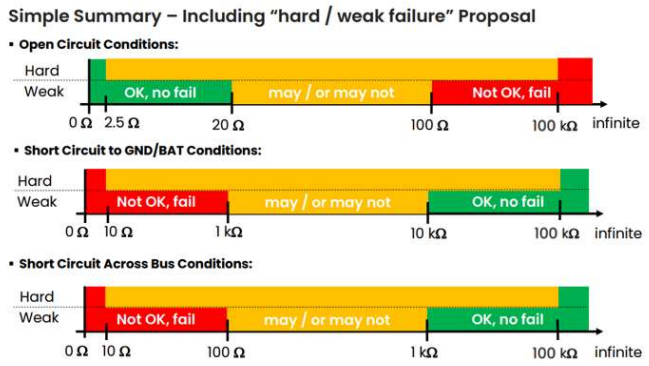

Figure 2: Summary HDD condition for "hard / weak failure"

During HDD measurement all other nodes shall be silent/transmitter high impedance.

It could be easier to apply this harness failures detection in a kind of diagnostic mode. The system implementer should design the system to ensure that the other nodes on the segment also enter a kind of passive mode to avoid disturbing the testing signals to be transmitted by the node performing the diagnostic.

9.2.2 HDD (HDD_CTRL; HDD_READY; START_CTRL; VALID; SHORT_OPEN_ST) register

HDD is a summary of four HDD-subclasses (HDD1; HDD2; HDD3; HDD4) which are defined together with some status and control bits in the HDD register shown in Table 8.

Register Name	HDD
Description	Harness defect detection
size[bits]	16
MMD	31
Addr/Offset	0xCC01/0 *

*In case PMD Transceiver is used for diagnostics in this specification the control register shall be at location x05 of PMD Transceiver.

15	14	13	12	11	10	9	8
HDD_CTRL	**HDD_READY**	**START_CTRL**	**Reserved**				
RW	RO	RW/SC	RO				
7	6	5	4	3	2	1	0
Reserved					**VALID**	**SHORT_OPEN_ST**	
RO					RO	RO	

Bit(s)	Name	Description	Access
15	HDD_CTRL	0 - HDD not requested (Default) 1 - HDD enable requested	RW
14	HDD_ READY	0 – status feedback (HDD is not ready) (Default) 1 – status feedback (HDD is ready)	RO
13	START_CTRL	**Write access:** 0 - Start measurement not requested 1 - Start measurement enabled **Read access:** 0 - Measurement completed or aborted or not started (Default) 1 – Measurement in progress	RW/SC
12:3	Reserved	Reserved (Default = 0)	RO
2	VALID	0 – Measurement not valid. (Default) 1 - Measurement results are ready and valid.	RO
1:0	SHORT_OPEN_ST	**Bus Short/Open Status:** 0 0 - no fault; everything is ok. (Default) 0 1 - detected as an open or missing termination(s) 1 0 - detected as a short or extra termination(s) 1 1 - fault but fault type not detectable More details can be available by vender specific register if supported.	RO
RO = read-only, RW = read-write, SC = self-clearing			

Table 8: Definition of HDD register.

9.2.3 HDD_CTRL field

Field Name	HDD_CTRL
Description	HDD enable requested
size[bits]	1
MMD	31
Addr/Offset	0xCC01/15 *

*In case PMD Transceiver is used for diagnostics in this specification the control register shall be at location x05 of PMD Transceiver.

Field value	Explanation (HDD_CTRL)
0x0	0 – HDD not requested (Default)
0x1	1 – HDD enable requested

Table 9: Definition of HDD_CTRL field in HDD register

9.2.4 HDD_READY field

Field Name	HDD_READY
Description	Status feedback (HDD ready/nor ready)
size[bits]	1
MMD	31
Addr/Offset	0xCC01/14 *

*In case PMD Transceiver is used for diagnostics in this specification the control register shall be at location x05 of PMD Transceiver.

Field value	Explanation (START)
0x0	0 – Status feedback (HDD is not ready)
0x1	1 – Status feedback (HDD is ready)

Table 10: Definition of HDD_READY field in the HDD register

9.2.5 START_CTRL field

Field Name	START_CTRL
Description	Start measurement
size[bits]	1
MMD	31
Addr/Offset	0xCC01/13 *

*In case PMD Transceiver is used for diagnostics in this specification the control register shall be at location x05 of PMD Transceiver.

Field value	Explanation (START)	
0x0	**Write access:** 0 – Start measurement not requested	**Read access:** Measurement completed or aborted or not started
0x1	**Write access:** 1 – Start measurement enabled	**Read access:** Measurement in progress

Table 11: Definition of START_CTRL field in the HDD register

9.2.6 VALID

Field Name	VALID
Description	Measurement results are ready and valid
size[bits]	1
MMD	31
Addr/Offset	0xCC01/2 *

*In case PMD Transceiver is used for diagnostics in this specification the control register shall be at location x05 of PMD Transceiver.

Field value	Explanation (VALID)
0x0	0 – Measurement not valid.
0x1	1 – Measurement results are ready and valid.

Table 12: Definition of VALID field in the HDD register

9.2.7 SHORT_OPEN_ST

Field Name	SHORT_OPEN_ST
Description	Bus Short/Open Status
size[bits]	2
MMD	31
Addr/Offset	0xCC01/1 *

*In case PMD Transceiver is used for diagnostics in this specification the control register shall be at location x05 of PMD Transceiver.

Field value	Explanation (SHORT_OPEN_ST)
0x0	0 – no fault; everything is ok
0x1	1 – detected as an open or missing termination(s)
0x2	2 – detected as a short or extra termination(s)
0x3	3 – fault but fault type not detectable

Table 13: Definition of SHORT_ST field in the HDD register

9.3 Dynamic Channel Quality

Dynamic channel quality includes the SQI diagnostic features with the two subclasses SQI, SQI+ and value.

9.3.1 SQI Transmit Opportunity ID (DCQ.TOID) register

The SQI value (8 levels), specified in 9.3.2 and the SQI+ value (8 to max. 256 levels), specified in 9.3.3, are determined for only a specific PLCA transmit opportunity or all as configured in DCQ.TOID. Multidrop mixing segments operating with PLCA enabled allow for the determination of a SQI or SQI+ value for each PHY transmit opportunity.

When this register is written (regardless of the previous value), the computation of DCQ.SQI and DCQ.SQI+ shall restart. Additionally, the DCQ.SQI.UPDATE field shall be reset.

Register Name	DCQ.TOID
Description	DCQ Signal Quality Index Transmit Opportunity ID
size[bits]	16
MMD	31
Addr/Offset	0xCC02/0

15	14	13	12	11	10	9	8
Reserved							
RO							
7	6	5	4	3	2	1	0
DCQ.TOID							
RW							

Bit(s)	Name	Description	Access
15:8	Reserved	Reserved (Default = 0)	RO
7:0	DCQ.TOID	Signal Quality Index Transmit Opportunity ID	RW
RO = read-only, RW = read-write, SC = self-clearing			

Table 14: Definition of register DCQ.TOID

9.3.1.1.1 DCQ.TOID field

Field Name	DCQ.DCQ.TOID
Description	Signal Quality Index (Update current SQI value)
size[bits]	8
MMD	31
Addr/Offset	0xCC02 / 0

Field value	Explanation (DCQ.TOID)
0x00	Compute SQI over packets received in PLCA transmit opportunity 0
0x01	Compute SQI over packets received in PLCA transmit opportunity 1
0x02	Compute SQI over packets received in PLCA transmit opportunity 2
…	…
0xFF	Compute SQI over all received packets. (default)

Table 15: Definition of TOID field in the DCQ register

9.3.2 SQI (DCQ.SQI.UPDATE; DCQ.SQI) register

Diagnostic class SQI

The SQI value of eight levels shall be stored in a mandatory register (see section 9.3.2.2 DCQ.SQI).

It is open to the vendors, to implement in addition a second SQI register with min. 3 and max. 8 bits.
For this optional DCQ.SQI+ register, if implemented, it is required to fulfill section 9.3.3.2 DCQ.SQI+.

Register Name	DCQ.SQI
Description	DCQ Signal Quality Index
size[bits]	16
MMD	31
Addr/Offset	0xCC03 / 0

15	14	13	12	11	10	9	8
SQI_UPD	**Reserved**						
RO	RO						
7	6	5	4	3	2	1	0
Reserved						**SQI**	
RO						RO	

Bit(s)	Name	Description	Access
15	SQI_UPD	**SQI Update** 0 – Update=0 (no change since last read) (Default) 1 – Update=1 (changed since last read)	RO
14:3	Reserved	**Reserved** (Default = 0)	RO
2:0	SQI	Signal Quality Index (current SQI value)	RO
RO = read-only, RW = read-write, SC = self-clearing			

Table 16: Definition of SQI field in the DCQ register

9.3.2.1 DCQ.SQI.UPDATE field

Field Name	DCQ.SQI.UPDATE
Description	Signal Quality Index (Update current SQI value)
size[bits]	1
MMD	31
Addr/Offset	0xCC03 / 15

Field value	Explanation (SQI_UPD)
0x0	0 – Update = 0 (no change since last read) (Default)
0x1	1 – Update = 1 (changed since last read)

Table 17: Definition of SQI.UPDATE field in the DCQ register

This bit is automatically cleared once read, or when DCQ.TOID is written.
Note that DCQ.SQI.UPDATE * is mapped at addresses 0xCC03 and 0xCC04. These two aliases are effectively the same bit, meaning that when one is cleared, the other one shall be cleared too. This behaviour allows the host to read either the SQI or the SQI+ register collecting the DCQ.SQI.UPDATE information in a single read operation.

* SQI: SQI or SQI+

9.3.2.2 DCQ.SQI (current SQI value) field

The SQI value of eight levels shall be stored in a 3bit register.

Field Name	DCQ.SQI
Description	Signal Quality Index (current SQI value)
size[bits]	3
MMD	31
Addr/Offset	0xCC03 / 0

Field value	Explanation (SQI)
0x0	0 - SQI=0 (worst value) (Default)
0x1	1 - SQI=1
0x2	2 - SQI=2
0x3	3 - SQI=3
0x4	4- SQI=4
0x5	5 - SQI=5
0x6	6 - SQI=6
0x7	7 - SQI=7 (best value)

Table 18: Definition of register field DCQ.SQI (8 levels)

Correlation SQI to BER.

The recommended correlation between the SQI values stored in the register is based on AWG noise (bandwidth of 40 MHz) as shown in the Table 19 as well for information purposes.

SQI with 3 bits (at least 8 levels)	**Recommended BER for AWG noise model (informative)** BER: Informative with the aim of calibrating SQI value of PHYs (Based on a defined test setup [4])
SQI = 0	BER > 10^-6
SQI = 1	10^-10 ≤ BER ≤ 10^-6
SQI = 2	
SQI = 3	BER < 10^-10
SQI = 4	
SQI = 5	
SQI = 6	
SQI = 7	BER < 10^-12

Table 19: Recommended correlation from SQI (at least 8 levels or 3 bits) to BER under AWG assumption.

The following features of the SQI value are mandatory:

- The indicated signal quality shall monotonically increase /decrease with noise (AWGN).
- The indicated SQI value shall be ≥ 3 for jitter ≤ 15ns @MDI (see [5]).
- SQI calculation shall be available in both PLCA and CSMA/CD mode.
- SQI Transmit Opportunity ID register is ignored in CSMA/CD mode.
  In that case SQI is therefore calculated over all received packets.

A PHY implementation shall update the SQI value no later than when all the following conditions are met:

Condition 1

At least 16 Kbytes of data at the MAC layer has been received since the last SQI update.

Condition 2

At least 32 carrier events (frames or bursts of frames) have been detected at the MAC layer since the last update.

9.3.2.2.1 Example to condition 1

Example for 1 Transmitter and 1 Receiver:

SQI_refresh_time_max(s) = 16kBytes/(Framerate[1)](frame/s)*Framesize[1)]kBytes))
[1)]:of the Transmitter

Calculation example:
One head node and one drop node, both are sending one max. Ethernet frame during one PLCA cycle (2 max. Ethernet Frames during one PLCA cycle).

SQI_(drop node sent to head node) calculated by head node = ?

Framesize(drop node) = Layer 1 Ethernet frame
= 1522Bytes

Framerate = 1 Frame / PLCA-Cycle-Time
= 1 Frame / [2*(preamble & SFD & payload & IPG) Bytes * 8 <bit/Bytes> * 100ns/bit]
= 1 Frame / [2*(1542Bytes+*8 bit/Bytes * 100ns/bit)] = 1/ (2*1,2336ms)
= 405,3 Frames/s

SQI_refresh_time_max(s) = 16kBytes/(Framerate[1)](frame/s)*Framesize[1)]kBytes))
= 16kBytes/(408,5 Frame/s *1,522kBytes/Frame)
= **25,9 ms**

Example for multiple Transmitter and multiple Receiver:

Average_SQI_refresh_time_max(s) = 16kBytes/(Average_Framerate[2)](frame/s)*Average_Framesize[2)](kBytes)

[2)]: Average on the line

Calculation example:
One Head node and 7 drop nodes, all are sending 5 max. Ethernet frames during every 7 PLCA cycle (8*5 max. Ethernet Frames during 7 PLCA cycle, Average: 40/((7 max. Ethernet frames) during 1 PLCA cycle)

SQI_(drop node ID1 sent to head node) calculated by head node = ?

Average_Framesize(drop node ID1) = Average Layer 1 Ethernet frame
= (5/7) * 1522 Bytes
= 1087,1 Bytes

Average_Framerate = 5 Frames / (7*PLCA-Cycle-Time)
= 5 Frames / [7*40*(preamble & SFD & payload & IPG) Bytes * 8 <bit/Bytes> * Time/bit]
= 5 Frames / [7*40*(1542 Bytes*8 <bit/Bytes> * 100ns)) = 5/ (7*40*1,2336ms)
= 14,47 Frames/s

SQI_refresh_time_max(s) = 16kBytes/(Average_Framerate[1)](frame/s)*Average_Framesize[1)]kBytes))
= 16kBytes/(14,46 Frame/s *1,522kBytes/Frame)
= **0,726 s**

9.3.2.2.2 Example to condition 2

Example for 1 Transmitter and 1 Receiver:

SQI_refresh_time_max(s)=32* FpB /Framerate(frame/s)

Calculation example:
Head node and drop node, both are sending one max. Ethernet frame (FpB = 1) during one PLCA cycle (2 max. Ethernet Frames during one PLCA cycle).

SQI_(drop node sent to head node) calculated by head node = ?

Framesize(drop node) = Layer 1 Ethernet frame
= 1522Bytes

Framerate = 1 Frame / PLCA-Cycle-Time
= 1 Frame / [2*(preamble & SFD & payload & IPG) Bytes * 8 <bit/Bytes> * 100ns/bit]
= 1 Frame / [2*(1542Bytes+*8 bit/Bytes * 100ns/bit)] = 1/ (2*1,2336ms)
= 405,3 Frames/s

SQI_refresh_time_max(s) = 32* FpB /Framerate(frame/s)
= 32*1 / (408,5 Frame/s)
= **78,33 ms**

Example for multiple Transmitter and multiple Receiver:

Average_SQI_refresh_time_max(s) = 32 * ∑ FpB(i) / ∑ Framerate(i)_(frame/s)

Calculation example:
Head node and 7 drop nodes, all are sending 5 max. Ethernet frames during every 7 PLCA cycle.
-> 8*5 max. Ethernet Frames during 7 PLCA cycle
-> Average: 40/7 max. Ethernet frames during 1 PLCA cycle

SQI_(drop node ID1 sent to head node) calculated by head node = ?

Average_Framesize(drop node ID1) = Average Layer 1 Ethernet frame
= (5/7) * 1522Bytes
= 1087,1 Bytes

Average_Framerate = 5 Frames / (7*PLCA-Cycle-Time)
= 5 Frames / [7*40*(preamble & SFD & payload & IPG) Bytes * 8 <bit/Bytes> * Time/bit]
= 5 Frames / [7*40*(1542 Bytes*8 <bit/Bytes> * 100ns)) = 5/ (7*40*1,2336ms)
= 14,47 Frames/s

Average_SQI_refresh_time_max(s) = 32 * ∑ FpB(i) / ∑ Framerate(i)_(frame/s)
= 32 * (8*1) / (8*14,47 (frame/s))
= **2,21 s**

FpB = Frame per burst = PLCA_burstcount + 1

Under the assumption that the total bandwidth required by the nodes is less than 10Mbit/s

9.3.2.2.3 Total results fulfilling both conditions 1 and 2

Example for 1 Transmitter and 1 Receiver: SQI_refresh_time_max(s) = **78,33 ms**

Example for multiple Transmitter and multiple Receiver: SQI_refresh_time_max(s) = **2,21 s**

Correlation SQI to BER.

The recommended correlation between the SQI values stored in the register is based on AWG noise (bandwidth of 40 MHz) as shown in the Table 19 as well for information purposes.

SQI with 3 bits (at least 8 levels)	**Recommended BER for AWG noise model (informative)** BER: Informative with the aim of calibrating SQI value of PHYs (Based on a defined test setup [4])
SQI = 0	BER > 10^-6
SQI = 1	10^-10 ≤ BER ≤ 10^-6
SQI = 2	
SQI = 3	BER < 10^-10
SQI = 4	
SQI = 5	
SQI = 6	
SQI = 7	BER < 10^-12

Table 19: Recommended correlation from SQI (at least 8 levels or 3 bits) to BER under AWG assumption.

9.3.3 DCQ.SQI+ (DCQ.SQI+.UPDATE; DCQ.SQI+) register

Diagnostic class SQI+

The SQI+ value from 8 up to 256 levels shall be stored in a register of 3 up to 8 bits shown in Table 20.

Register Name	DCQ.SQI+
Name	Signal Quality Index +
size[bits]	16
MMD	31
Addr/Offset	0xCC04 / 0

15	14	13	12	11	10	9	8
SQI+_UPD	**Reserved**						
RO	RO						
7	6	5	4	3	2	1	0
SQI+							
RW							

Bit(s)	Name	Description	Access
15	SQI+_UPD	**SQI+ Update** 0 – Update = 0 (no change since last read) (Default) 1 – Update = 1 (changed since last read)	RO
14:8	Reserved	Reserved (Default = 0)	RO
7:0	SQI	Signal Quality Index+ (current SQI+ value)	RO
RO = read-only, RW = read-write, SC = self-clearing			

Table 20: Definition of register DCQ.SQI+

9.3.3.1 DCQ.SQI+.UPDATE field

Field Name	DCQ.SQI+.UPD
Description	Signal Quality Index (Update current SQI+ value)
size[bits]	1
MMD	31
Addr/Offset	0xCC04/15

Field value	Explanation (SQI+_UPD)
0x0	0 – Update = 0 (no change since last read) (Default)
0x1	1 – Update = 1 (changed since last read)

Table 21: Definition of register field DCQ.SQI+.UPDATE

9.3.3.2 DCQ.SQI+ (current SQI+ value) field

The SQI+ value of 8 to max. 256 levels shall be stored in an 8-bit register.

Field Name	DCQ.SQI+
Description	Signal Quality Index (current SQI+ value)
size[bits]	8
MMD	31
Addr/Offset	0xCC04/0

Field value	**Explanation (SQI+)**
0x0	R=0 (worst value) (Default)
0x1	R=1
0x2	R=2
0x3	R=3
0x4	R=4
0x5	R=5
…	..
0xFF	R= 255 (best value)

Table 22: Definition of register field DCQ.SQI+ (8 until 256 level)

SQI+ format definition:

- Fixed-point Q0.8 representation of the SQI (0 … 1)
  SQI+ is 100 multiplied by the fixed-point Q0.8 representation of the "bin" column. It just provides a human-friendly way of reading the SQI+ value.
  - PHY implementations using N bits will define only the N most significant bits, padding the remaining with '1's (i.e., left-aligned)
  - The host can translate the Q0.8 representation (R) into the SQI+ value
    SQI+ = 100 * (R + 1) / 256
  - The above formula is independent of the resolution of the specific implementation

- PHYs with different resolutions will exhibit a different granularity, but numbers will be consistent and comparable.

- Quick (trivial) example
  - PHY A uses 3 bits and reports ~ half-scale value: '010'
  - PHY B uses 5 bits and reports ~ half-scale value: '01011'
  - with padding, values become '01011111' and '01011111' → SQI+ = 37.5
  - Although PHY B is more accurate and could report, e.g., '01001111' → SQI+ = 31.25

Correlation SQI+ to BER.

The recommended correlation between the SQI+ values stored in the register is based on AWG noise (bandwidth of 40 MHz) as shown in the following Table 24, 25 and 26 as an example for 3 to 5 bits as well for information purposes.

Example 1: SQI+ with 3 bits				Recommended BER for AWG noise model (informative)
dec	hex	bin	SQI+	BER: Informative with the aim of calibrating SQI+ value of PHYs (Based on a defined test setup [4])
0	1F	00011111	12,50	BER > 10^-6
1	3F	00111111	25,00	10^-10 ≤ BER ≤ 10^-6
2	5F	01011111	37,50	
3	7F	01111111	50,00	BER < 10^-10
4	9F	10011111	62,50	
5	BF	10111111	75,00	
6	DF	11011111	87,50	
7	FF	11111111	100,00	BER < 10^-12

Table 23: Recommended correlation 8 level SQI value to BER

Example 2: SQI+ with 4 bits				Recommended BER for AWG noise model (informative)
dec	hex	bin	SQI+	BER: Informative with the aim of calibrating SQI+ value of PHYs (Based on a defined test setup [4])
0	0F	00001111	6,25	BER > 10^-6
1	1F	00011111	12,50	
2	2F	00101111	18,75	
3	3F	00111111	25,00	10^-10 ≤ BER ≤ 10^-6
4	4F	01001111	31,25	
5	5F	01011111	37,50	
6	6F	01101111	43,75	
7	7F	01111111	50,00	BER < 10^-10
8	8F	10001111	56,25	
9	9F	10011111	62,50	
10	AF	10101111	68,75	
11	BF	10111111	75,00	
12	CF	11001111	81,25	
13	DF	11011111	87,50	

14	EF	11101111	93,75	
15	FF	11111111	100,00	BER < 10^-12

Table 24: Recommended correlation 16 level SQI value to BER

Example 3: SQI+ with 5 bits				Recommended BER for AWG noise model (informative) BER: Informative with the aim of calibrating SQI+ value of PHYs (Based on a defined test setup [4])
dec	hex	bin	SQI+	
0	07	00000111	3,13	BER > 10^-6
1	0F	00001111	6,25	
2	17	00010111	9,38	
3	1F	00011111	12,50	
4	27	00100111	15,63	
5	2F	00101111	18,75	
6	37	00110111	21,88	
7	3F	00111111	25,00	10^-10 ≤ BER ≤ 10^-6
8	47	01000111	28,13	
9	4F	01001111	31,25	
10	57	01010111	34,38	
11	5F	01011111	37,50	
12	67	01100111	40,63	
13	6F	01101111	43,75	
14	77	01110111	46,88	
15	7F	01111111	50,00	BER < 10^-10
16	87	10000111	53,13	
17	8F	10001111	56,25	
18	97	10010111	59,38	
19	9F	10011111	62,50	
20	A7	10100111	65,63	
21	AF	10101111	68,75	
22	B7	10110111	71,88	
23	BF	10111111	75,00	
24	C7	11000111	78,13	
25	CF	11001111	81,25	
26	D7	11010111	84,38	
27	DF	11011111	87,50	
28	E7	11100111	90,63	
29	EF	11101111	93,75	
30	F7	11110111	96,88	
31	FF	11111111	100,00	BER < 10^-12

Table 25: Recommended correlation 32 level SQI value to BER

The following features of the SQI+ value is mandatory:

- The indicated signal quality shall monotonically increase /decrease with noise (AWGN).
- The indicated SQI+ value shall be ≥ 50 for jitter ≤ 15ns @MDI (see [5])
- SQI+ calculation shall be available in both PLCA and CSMA/CD mode.

A PHY implementation shall update the SQI+ value no later than when all of the following two conditions are met:

Condition 1

At least 16 Kbytes of data at the MAC layer has been received since the last SQI+ update.

Condition 2

At least 32 carrier events (frames or bursts of frames) have been detected at the MAC layer since the last update.

9.3.3.2.1 Example to condition 1:

For 1 Transmitter and 1 Receiver:

SQI+_refresh_time_max(s)= 16kBytes/(Framerate[1)](frame/s)*Framesize[1)]kBytes))

[1)]: of the Transmitter

For multiple Transmitter and multiple Receiver:

Average_SQI+_refresh_time_max(s)= 16kBytes/(Average_Framerate[2)](frame/s)*Average_Framesize[2)](kBytes)

[2)]: Average on the line

9.3.3.2.2 Example to condition 2:

For 1 Transmitter and 1 Receiver:

SQI+_refresh_time_max(s)=32* FpB /Framerate(frame/s)

For multiple Transmitter and multiple Receiver:

Average_SQI+_refresh_time_max(s)=32* ∑ FpB(i) / ∑ Framerate(i)_(frame/s)

FpB = Frame per burst = PLCA_burstcount + 1

Under the Assumption that the total bandwith required by the nodes is less than 10Mbit/s