10BASE-T1S

EMC Test Specification for Transceivers

This EMC measurement specification shall be used as a standardized common scale for EMC evaluation of 10BASE-T1S transceivers.

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INTRODUCTION

The IEEE 802.3cg standard defines a 10 Mbit/s Ethernet communication over an unshielded single pair of conductors and differentiates the two systems 10BASE-T1S and 10BASE-T1L. The 10BASE-T1S implementation covers a half-duplex communication using a CSMA/CD for point to point channel and the optional functionalities full duplex communication for a point to point channel and a half duplex communication for a so called mixing segment (or multidrop mode) with at least 8 nodes and 25 m length of bus lines. In any case, the bus cable is terminated with the line impedance of 100 Ω at both ends of the channel. As an optional feature to enable a deterministic access time for each bus node in a mixing segment the new access method PLCA is overlaid to the CSMA/CD system.

For 10BASE-T1S physical layer implementation there are different commercially solutions available:

- classical PHY with MDI and MAC interface;
- MAC-PHY as a combination of an IEEE Clause 4 MAC and a 10BASE-T1S PHY;
- PMD transceiver with 3-pin interface to the host controller.

This specification is focused on EMC evaluation of 10BASE-T1S transceivers in general and covers all three types.

Due to the high communication rate of 10BASE-T1S and the intended use of unshielded twisted pair cable, a high risk of EMC problems is expected. For this reason, an EMC optimization of all components of the Ethernet physical layer is required. Different aspects influence the EMC behavior of the complete system:

- Ethernet transceiver hardware implementation itself;
- Ethernet transceiver software configuration (register settings);
- MDI test network (BIN);
- layout implementation of transceiver and interface network;
- other active ICs that are necessary for Ethernet communication and for function of application device (e.g. µC);
- EMC concept of application device;
- symmetry of Ethernet wire and connector;
- transfer function from external disturbance sources to the Ethernet communication system.

For EMC tests of a 10BASE-T1S communication system on ECU level BCI and antenna measurement are usually required test methods. But they are affected by all given aspects in parallel. An advantageous strategy for EMC optimization of the application device is to analyze the influence of each aspect separately.

This EMC measurement specification is focused on the physical layer of the Ethernet interface using standard EMC test methods for ICs. The intent of this specification is:

- a common EMC evaluation of 10BASE-T1S transceiver for comparison purpose;
- checking the EMC behavior of the transceiver in combination with different MDI test networks (BINs);
- separation of emitted disturbance into disturbing source:
    - MDI pins;
    - voltage supplies;
    - other digital interfaces (e.g. xMII or SPI);

- clock out signals;

evaluation of EMC behavior for symmetrical and unbalanced disturbances at MDI pins.

ABBREVIATION/SYMBOLS

AM	Amplitude Modulation
BIN	MDI Test Network
BIST	Built In Self Test
CM	Common Mode
CMC	Common Mode Choke
CRC	Cyclic Redundancy Check
COL	Collision, MII signal that indicates collision
CSMA/CD	Carrier-Sense Multiple Access with Collision Detection
DM	Differential Mode
DPI	Direct Power Injection
DSO	Digital Storage Oscilloscope
DTT	Data Transfer Test
DUT	Device Under Test
CW	Continuous Wave
EAS	Ethernet Access Switch
ECU	Electronic Control Unit
LPF	Low Pass Filter
MAC	Medium Access Control
MAC-PHY	Integration of IEEE Clause 4 MAC and 10BASE-T1x PHY in an IC
MDI	Media Dependent Interface
MII	Media Independent Interface
MSE	Mean Squared Error
PM	Pulse Modulation
PMD	Physical Medium Dependent

PLCA	Physical Layer Collision Avoidance
PHY	Interface semiconductor circuit for implementation of the functions of the Ethernet physical layer
PRBS	Pseudo Random Bit Stream
RF	Radio Frequency
SBC	System Basis Chip
SNR	Signal to Noise Ratio
SPI	Serial Peripheral Interface
SQI	Signal Quality Indicator
WUP	Wake Up Pulse

1 SCOPE

This document specifies test and measurement methods for EMC evaluation of Ethernet transceiver ICs under network condition. It defines test configurations, test conditions, test signals, failure criteria, test procedures, test setups and test boards. It is applicable for transceiver of the Ethernet system 10BASE-T1S according to IEEE 802.3cg and covers

- the emission of RF disturbances;
- the immunity against RF disturbances;
- the immunity against impulses;
- the immunity against electrostatic discharges (ESD).

2 NORMATIVE REFERENCES

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

[1] IEEE P802.3cgTM: Physical Layer Specifications and Management Parameters for 10 Mb/s Operation and Associated Power Delivery over a Single Balanced Pair of Conductors

[2] OPEN ALLIANCE Inc.: IEEE 10BASE-T1S EMC Test Specification for Common Mode Chokes, version 1.1

[3] OPEN ALLIANCE Inc.: IEEE 10BASE-T1S EMC Test Specification for ESD suppression devices, version 1.1

[4] OPEN ALLIANCE Inc.: IEEE 10BASE-T1S Channel and Component Requirements for Link Segments, version 1.0

[5] OPEN ALLIANCE Inc.: 10BASE-T1S Sleep/Wake-up Specification, version 1.0

[6] OPEN ALLIANCE Inc.: 10BASE-T1S System Implementation Specification, version 1.0

[7] OPEN ALLIANCE Inc.: 10BASE-T1S PMD Transceiver Interface, version 1.5

[8] IEC 61967-1, Integrated circuits, Measurement of electromagnetic emissions – Part 1: General and definitions

[9] IEC 61967-2, Integrated circuits – Measurement of electromagnetic emissions – Part 2: Measurement of radiated emissions – TEM cell and wideband TEM cell method

[10] IEC 61967-4, Integrated circuits, Measurement of electromagnetic emissions – Part 4: Measurement of conducted emissions – 1 Ω/150 Ω direct coupling method

[11] IEC 61967-8, Integrated circuits – Measurement of electromagnetic emissions – Part 8: Measurement of radiated emissions – IC stripline method

[12] IEC 62132-1, Integrated circuits, Measurement of electromagnetic immunity – Part 1: General and definitions

[13] IEC 62132-2, Integrated circuits – Measurement of electromagnetic immunity – Part 2: Measurement of radiated immunity – TEM cell and wideband TEM cell method

[14] IEC 62132-4, Integrated circuits, Measurement of electromagnetic immunity – Part 4: Direct RF power injection method

[15] IEC 62132-8, Integrated circuits, Measurement of electromagnetic immunity – Part 8: Measurement of radiated immunity – IC stripline method

[16] IEC 62215-3, Integrated circuits – Measurement of impulse immunity – Part 3: Non-synchronous transient injection method

[17] ISO 10605, Road vehicles – Test methods for electrical disturbances from electrostatic discharge

[18] ISO 7637-2, Road vehicles – Electrical disturbances from conduction and coupling – Part 2: Electrical transient conduction along supply lines only

[19] CISPR 16-1-1, Specification for radio disturbance and immunity measuring apparatus and methods – Part 1-1: Radio disturbance and immunity measuring apparatus – Measuring apparatus

3 TERMS AND DEFINITIONS

For the purposes of this document, the terms and definitions given 2 Normative references and following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- ISO Online browsing platform: available at https://www.iso.org/obp;
- IEC Electropedia: available at http://www.electropedia.org.

10BASE-T1S transceiver	transceiver 10 Mbit/s via single balanced twisted pair, with a functionality according to IEEE 802.3cg (10BASE-T1S)
global pin	pin that carries a signal or power, which enters or leaves the application board without any active component in between
local pin	pin that carries a signal or power, which does not leave the application board
mandatory components, pl	components needed for proper function and/or technical requirement of IC as specified by the IC manufacturer
EAS	IC with integrated Ethernet transceivers and switch functionality as defined in IEEE 802.3

4 GENERAL

The intention of this document is to evaluate the EMC performance of Ethernet transceivers under application conditions in a minimal network.

The evaluation of the EMC characteristics of Ethernet transceivers shall be performed for the implemented functional operation modes as defined in Table 4-1 under network conditions for conducted RF emission and RF immunity tests and impulse immunity tests and on a single transceiver IC for electrostatic discharge tests.

The aim of these tests is to determine the EMC performance on dedicated pins of the Ethernet transceiver which are considered as EMC relevant in the application. For an Ethernet transceiver, these pins are the PHY transceiver pins (BI_DA+, BI_DA-), such as any pins that may be global (e.g. V_{BAT} and WAKE) as well as local pins like power supply inputs (V_{DDx}). The WAKE pin is given as an example, representing any global pin other than MDI and voltage supply V_{BAT}.

If the DUT includes additional product specific EMC relevant pins (functions), it shall be tested as well. The test conditions and failure validation criteria shall be adapted to the definitions for the standard functionality of Ethernet transceivers.

The test methods used for the EMC characterization are based on the international standards for IC EMC tests and are described in Table 4-1.

Configuration	Test	Test method	Evaluation	Operation mode
Transceiver network	RF conducted emission (EMI)	150 Ω direct coupling (IEC 61967-4 [10])	Spectrum	Normal
	RF conducted immunity (RF)	DPI (IEC 62132-4 [14])	Function, DPI distortion (Unwanted feedback to other Ethernet communication if connected to the network)	Normal
				Low power
			DPI distortion	Unpowered
	Impulse immunity (IMP)	Non-synchronous transient injection (IEC 62215-3 [16])	Function	Normal
				Low power
	ESD powered	Contact discharge (ISO 10605 [17])	Function	Normal
				Low power
Single transceiver	ESD unpowered	Contact discharge (ISO 10605 [17])	Damage	Unpowered

Table 4-1: Overview of measurements and tests

The 150 Ω direct coupling, DPI and impulse immunity test methods are chosen for the evaluation of the conducted EMC characteristic of transceivers in network condition. These three test methods are based on the same approach using conductive coupling. Therefore, it is possible to use the same test board for all

tests in functional operation mode, which reduces the effort and increases the reproducibility and comparability of test results.

Powered ESD test will be performed using the same approach of testing the Ethernet transceiver under network conditions but a separate, modified version of the test board is used because of RF and ESD tests cannot be combined on one test board if all specific test conditions of each test method should be covered.

The unpowered ESD test is performed on a separate test board with a single transceiver.

All measurements and tests should be done according to the general drawings of schematics given in Annex A with soldered transceivers on different test boards as described in Annex B to ensure application like conditions and avoid setup effects by sockets. Recommended limits for 10BASE-T1S Ethernet transceivers in automotive application are given in Annex C.

In general, the test definition is done for Ethernet single transceiver. PMD transceiver according to [7] and Ethernet transceiver cells embedded in EASs, SBCs or ASICs shall follow the test methods for PHYs, adapting test conditions and targets as necessary. Such adaptations shall be done individually for the dedicated IC but shall follow the general definitions. Specific adaptations for PMD transceivers are included in the document.

In order to verify filter effects on the EMC performance of Ethernet transceivers, configurations with different bus interface networks for MDI are defined in this document. In consequence the frequency characteristic of these filter elements shall be taken into account for the interpretation of the test results.

5 TEST AND OPERATING CONDITIONS

5.1 Supply and ambient conditions

For all tests and measurements under operating conditions, the settings are based on systems with 12 V power supply, which is the main application of Ethernet transceivers. If a transceiver is designed or targeted for other power supply voltages, the test conditions and test targets shall be adapted and documented accordingly. The defined supply and ambient conditions for functional operation are given in Table 5-1.

Parameter	Value
Battery voltage supply	(14.0 ± 0.2) V
Voltage supply, auxiliary supply	(U_{nom} ± 0.1) V
Test ambient temperature	(23 ± 5) C

Table 5-1: Supply and ambient conditions for functional operation

For RF emission measurements, the ambient noise floor shall be at least 6 dB below the applied target limit and documented in the test report.

For ESD tests, the requirements of ISO 10605 [17] climatic environmental conditions shall be applied.

5.2 Test operation modes

5.2.1 General

The Ethernet transceiver shall be tested in operation modes according to Table 4-1. Depending on the transceiver the configuration for functional operation modes is controlled by hardware and/or software settings.

5.2.2 Transceiver configuration for normal operation mode

To test in normal functional operation mode, a transceiver configuration according to Table 5-2 shall be used.

Operation mode	Content
Transceiver configuration for normal mode with PLCA for PHY and MAC-PHY	• half duplex mode • PLCA activated with maximum node ID number of 1 (two nodes in the test network) and transmit opportunity timer = default according to [1] • collision detection mechanism is masked as per the definitions in 10BASE-T1S System Implementation Specification [6] • transceiver configuration as specified by semiconductor manufacturer for reference application in datasheet, application note or comparable documentation (to be documented in the test report)
Transceiver configuration for normal mode for PMD transceiver	• sending TRANSMIT command, data and RESET command via TX signal according to [7] • transceiver configuration as specified by semiconductor manufacturer for reference application in datasheet, application note or comparable documentation (to be documented in the test report) • if needed, software configuration using the CONFIG command according to [7]

Table 5-2: Definition of transceiver configuration for normal operation mode

5.2.3 Transceiver configuration for low power mode

To test in low power mode, a transceiver configuration according to Table 5-3 shall be used.

Operation mode	Content
Transceiver configuration for low power mode for PHY and MAC-PHY	• transceiver configuration as specified by semiconductor manufacturer for reference application in datasheet, application note or comparable documentation (to be documented in the test report)
Transceiver configuration for low power mode for PMD transceiver	• sending LOWPWRRQ command via TX signal according to [7]

Table 5-3: Definition of transceiver configuration for low power mode

5.3 Definition of BIN

For test of 10BASE-T1S transceivers the following MDI test networks (BIN) are defined:

- Minimum MDI test network (Min-BIN):
  DC blocking capacitor C_{ac1} = C_{ac2} = 100 nF as illustrated in Figure 5-1
- Standard MDI test network (Std-BIN):
  DC blocking capacitor C_{ac1} = C_{ac2} = 100 nF and a CMC that meet the recommendations of [2] as illustrated in Figure 5-2
- Optimized MDI test network (Opt-BIN):
  DC blocking capacitor C_{ac1} = C_{ac2} = 100 nF and a CMC that meet the recommendations of [2], a Low pass filter (LPF) and a ESD suppression devices or terminations defined by semiconductor manufacturer as illustrated in Figure 5-3. The position of ESD suppression devices within the interface network can either be between transceiver and CMC and / or between C_{ac1} and C_{ac2} and MDI port.

NOTE Min-BIN and Std-BIN are defined to provide data for comparison of the EMC characteristics of different Ethernet transceivers. Opt-BIN is intended to use for evaluation of EMC characteristics of the tested Ethernet transceivers.

NOTE For DC blocking capacitors C_{ac1} and C_{ac2} the capacitance C = 100 nF is set as default value for tests. Other capacitor values, defined by semiconductor manufacturer, are also possible to use and need to be documented in the test report.

NOTE The characteristics of ESD suppression device can be evaluated according to the definitions of [3].

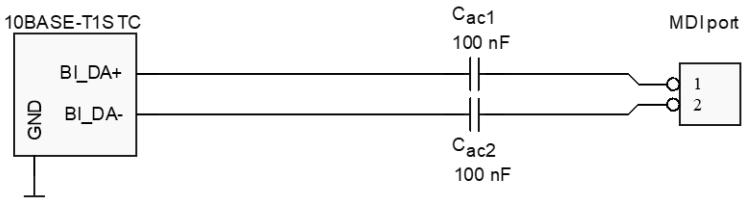


Figure 5-1: Minimum MDI test network (Min-BIN)

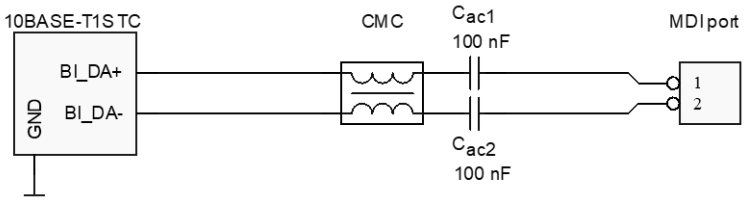


Figure 5-2: Standard MDI test network (Std-BIN)

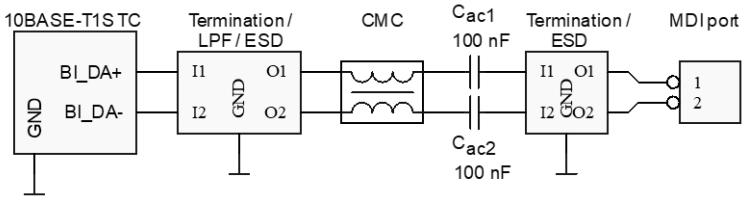


Figure 5-3: Optimized MDI test network (Opt-BIN)

The S-Parameter S_{cc21}, S_{dd21}, S_{sd21} and S_{sd12} of CMC samples used for testing may be measured or prepared by the manufacturer according to [2] and shall be documented in the test report.

5.4 Test configuration

5.4.1 General configuration for transceiver network

A minimal Ethernet test network consisting of two Ethernet transceivers of same type and a distributed MDI differential line termination (without GND path) shall be used to evaluate the conducted RF emission, RF immunity and impulse immunity as well as powered ESD immunity characteristic of an Ethernet transceiver in functional operation mode.

The test configuration in general consists of line termination (Term 1 and Term 2), Ethernet transceivers with external mandatory components and protection and filter components (Ethernet node) in a minimal test network, where filtered power supplies, signals, monitoring probes and coupling networks are connected as shown in Figure 5-4.

The definitions of different BINs are given in 5.3. Both nodes are configured according to data sheet of the semiconductor manufacturer to establish a half-duplex Ethernet link. This connection is carried out as line impedance controlled PCB traces and not a wire connection.

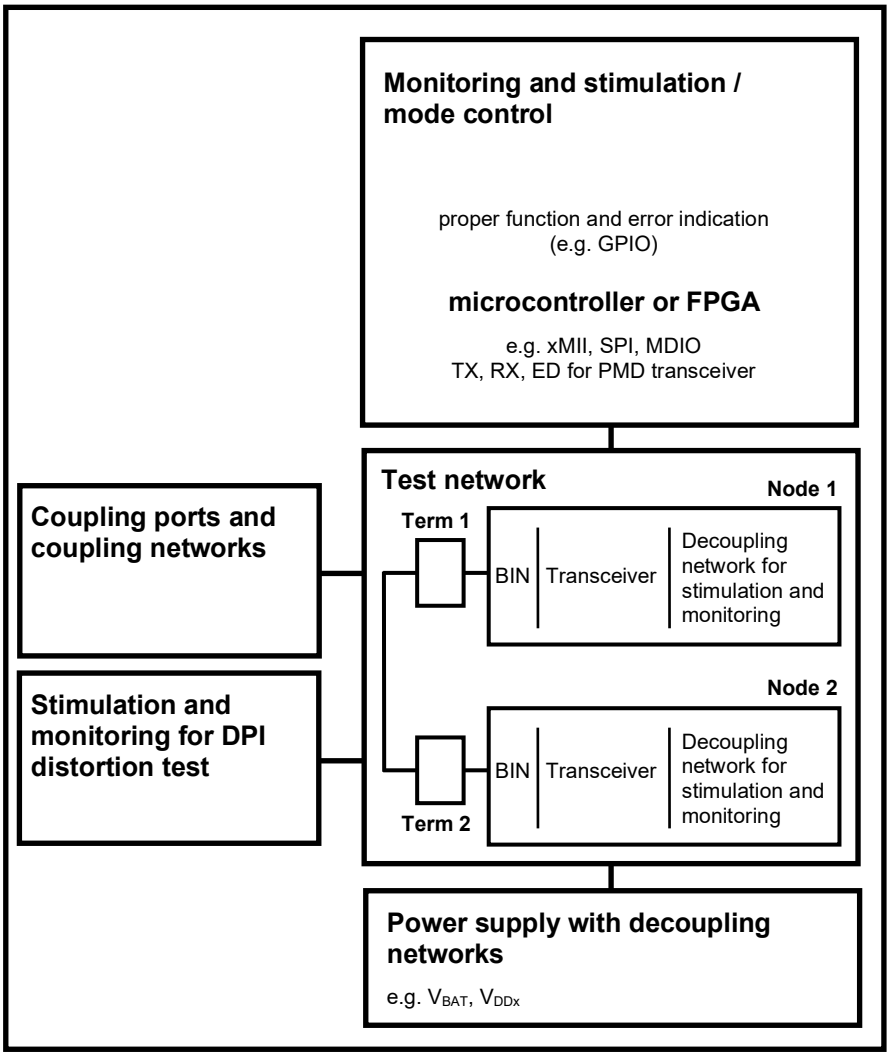


Figure 5-4: General test configuration for conducted tests of the transceiver network

NOTE In specific cases or for analysis a deviation from this setup can be agreed between the users of this document and will be noted in the test report.

The microcontroller or FPGA is used for configuring and monitoring the Ethernet transceiver and for generating a test communication. For this purpose, it should be able to operate with the communication interfaces that are supported by the tested Ethernet transceiver (e.g. xMII, or SPI or TX, RX and ED for PMD transceiver).

If Ethernet transceivers support multiple interfaces to the host microcontroller in minimum two of them should be used for the transceiver network. The default interface is MII for a 10BASE-T1S PHY and SPI for a 10BASE-T1S MAC-PHY. For a 10BASE-T1S PMD transceiver the interface is defined to signals TX, RX and ED.

In most cases it is beneficial to use one microcontroller or FPGA per Ethernet node. The microcontroller or FPGA shall be EMC decoupled from the tested transceiver (and its EMC coupling networks) using filter networks at voltage supplies. Specific layout requirements for effective EMC decoupling shall be considered.

A specific software implementation runs on the microcontroller or FPGA, which should be adapted to the transceiver type, especially for configuration and monitoring.

If an EAS or an IC with more than one integrated Ethernet transceiver (e.g. Dual PHY) shall be evaluated, each port that is intended to be used for wired Ethernet communication must be tested separately. For that purpose, the tested port of node 1 shall be connected with the same port of node 2 (port 1 to port 1, port 2 to port 2, ...).

General drawings of schematics with more details are given in Annex A.

5.4.2 General configuration for single transceiver

The general test configuration for unpowered ESD test of Ethernet transceivers consists of a single Ethernet transceiver with external mandatory components and protection and filter components on a test board with discharge coupling networks as shown in Figure 5-5.

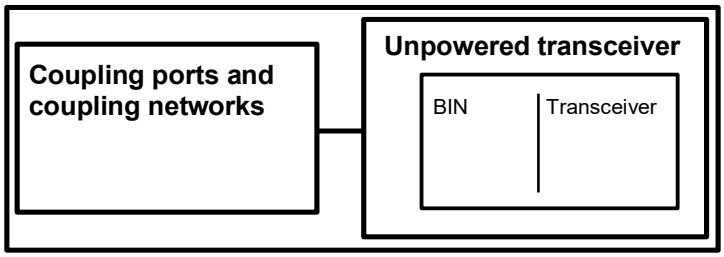
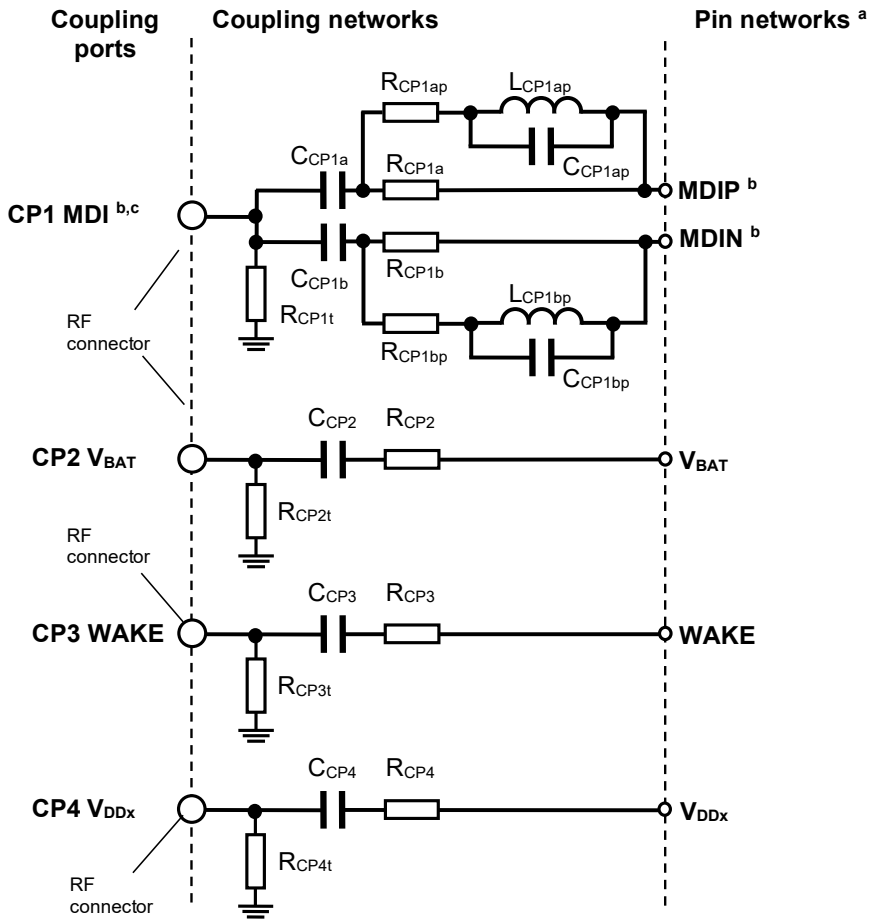


Figure 5-5: General test configuration for unpowered ESD test

5.4.3 Transceiver network tests - coupling ports and networks for conducted tests

The coupling ports and coupling networks are used to transfer disturbances to or from the test network with a defined transfer characteristic. The schematic of the coupling ports, networks and pins are shown in Figure 5-6. The values of the components are dependent on the test method and defined in Table 5-4. The tolerance of the components shall be 1 % or less. For the resistors R_{CP1a} and R_{CP1b} used for symmetrical coupling, a maximum mismatch of 0.1 % is recommended.

NOTE Components can be selected manually out of a larger set of resistors.



[a] The pin networks include all external mandatory components and protection and filter components for the respective pin or pins.

[b] The pins MDIP and MDIN represent all pins of 10BASE-T1S transceiver that are connected to MDI.

[c] The Components C_{CP1ap}, C_{CP1bp}, L_{CP1ap}, L_{CP1bp}, R_{CP1ap} and R_{CP1bp} are only used for RF immunity tests with frequency selective unbalance coupling on MDI. For all other tests, these components are unused.

Figure 5-6: Transceiver network tests - coupling ports and networks

Port	Type	Purpose	Component		
			$R_{CP1..4}$	$C_{CP1..4}$	$R_{CP1..4t}$
CP1	EMI1	RF symmetrical emission measurement on MDI	R_{CP1a} = 120 Ω R_{CP1b} = 120 Ω	C_{CP1a} = 4.7 nF C_{CP1b} = 4.7 nF	R_{CP1t} = 51 Ω
	EMI1a	RF asymmetric emission measurement on MDI (+ 5 %)	R_{CP1a} = 121 Ω R_{CP1b} = 115 Ω	C_{CP1a} = 4.7 nF C_{CP1b} = 4.7 nF	R_{CP1t} = 51 Ω
	EMI1b	RF asymmetric emission measurement on MDI (- 5 %)	R_{CP1a} = 115 Ω R_{CP1b} = 121 Ω	C_{CP1a} = 4.7 nF C_{CP1b} = 4.7 nF	R_{CP1t} = 51 Ω
	EMI1c	RF asymmetric emission measurement on MDI (+ 10 %)	R_{CP1a} = 127 Ω R_{CP1b} = 115 Ω	C_{CP1a} = 4.7 nF C_{CP1b} = 4.7 nF	R_{CP1t} = 51 Ω
	EMI1d	RF asymmetric emission measurement on MDI (- 10 %)	R_{CP1a} = 115 Ω R_{CP1b} = 127 Ω	C_{CP1a} = 4.7 nF C_{CP1b} = 4.7 nF	R_{CP1t} = 51 Ω
	RF1	RF symmetrical coupling for immunity test on MDI	R_{CP1a} = 120 Ω R_{CP1b} = 120 Ω	C_{CP1a} = 4.7 nF C_{CP1b} = 4.7 nF	not used
	RF1c	RF asymmetrical coupling for immunity test on MDI (+ 10 %)	R_{CP1a} = 127 Ω R_{CP1b} = 115 Ω	C_{CP1a} = 4.7 nF C_{CP1b} = 4.7 nF	not used
	RF1d	RF asymmetrical coupling for immunity test on MDI (- 10 %)	R_{CP1a} = 115 Ω R_{CP1b} = 127 Ω	C_{CP1a} = 4.7 nF C_{CP1b} = 4.7 nF	not used
	RF1e	RF asymmetrical frequency selective coupling for immunity test on MDI – A	R_{CP1a} = 120 Ω R_{CP1b} = 150 Ω R_{CP1ap} = 270 Ω R_{CP1bp} = 510 Ω C_{CP1ap} = 6.8 pF C_{CP1bp} = np L_{CP1ap} = np L_{CP1bp} = 560 nH	C_{CP1a} = 4.7 nF C_{CP1b} = 4.7 nF	not used
	RF1f	RF asymmetrical frequency selective coupling for immunity test on MDI – B	R_{CP1a} = 150 Ω R_{CP1b} = 120 Ω R_{CP1ap} = 510 Ω R_{CP1bp} = 270 Ω C_{CP1ap} = np C_{CP1bp} = 6.8 pF L_{CP1ap} = 560 nH L_{CP1bp} = np	C_{CP1a} = 4.7 nF C_{CP1b} = 4.7 nF	not used
	IMP1	Impulse coupling on MDI	R_{CP1a} = 120 Ω R_{CP1b} = 120 Ω	C_{CP1a} = 4.7 nF C_{CP1b} = 4.7 nF	not used

	ESD1 IND	Indirect ESD coupling on MDI [a]	R_{CP1a} = 120 Ω R_{CP1b} = 120 Ω	C_{CP1a} = 33 pF C_{CP1b} = 33 pF	R_{CP1t} = 220 kΩ [b]
CP2	EMI2	RF emission measurement on V_{BAT}	R_{CP2} =120 Ω	C_{CP2} = 6.8 nF	R_{CP2t} = 51 Ω
	RF2	RF coupling for immunity test on V_{BAT}	R_{CP2} = 0 Ω	C_{CP2} = 6.8 nF	not used
	IMP2	Impulse coupling on V_{BAT}	R_{CP2} = 0 Ω	Shorted	not used
CP3	EMI3	RF emission measurement on WAKE	R_{CP3} = 120 Ω	C_{CP3} = 6.8 nF	R_{CP3t} = 51 Ω
	RF3	RF coupling for immunity test on WAKE	R_{CP3} = 0 Ω	C_{CP3} = 6.8 nF	not used
	IMP3	Impulse coupling on WAKE	R_{CP3} = 0 Ω	C_{CP3} = 1 nF	not used
CP4	EMI4	RF emission measurement on V_{DDX}	R_{CP4} = 120 Ω	C_{CP4} = 6.8 nF	R_{CP4t} = 51 Ω

The parasitic inductance value of all resistors and capacitors used for RF emission and immunity coupling networks shall be less than 2 nH.

To ensure reliable performance, the two coupling resistors, RCP1a and RCP1b, can be implemented as parallel combination of two resistors of the same component type.

a All used resistors of the ESD coupling network shall be specified as ESD-robust up to the maximum used discharge voltage level. The specified peak voltage of used capacitors shall be at least 3 kV. The value for the coupling capacitance is estimated related to the test setup for indirect ESD test defined in ISO 10605 [17].

b The resistor R_{CP1t} is used optional to avoid static pre-charge of discharge point caused by the ESD generator. A spark-over at this resistor at high test levels shall be avoided. If a static pre-charge is prevented by the ESD generator construction these resistors are not needed. Alternatively, an external resistor can be used to remove pre-charges of each discharge point before each single test.

Table 5-4: Transceiver network tests – component value definitions of coupling ports and networks

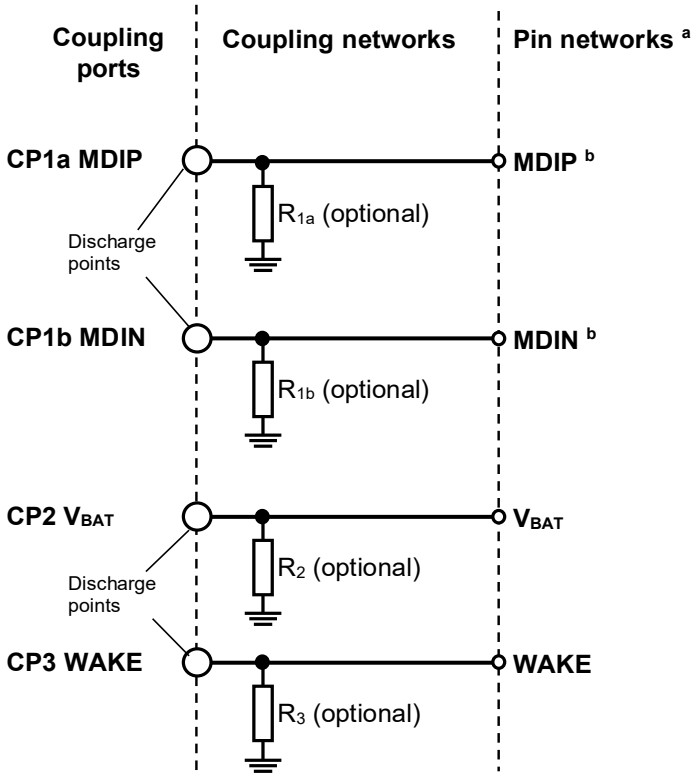
The test configurations with coupling ports and coupling networks connected to the Ethernet test network are given in the general drawing of schematics in Figure A.1.

The characterization of the coupling ports and coupling networks is carried out as follows:

The magnitude of insertion losses (S_{21} measurement) between the ports (CP1 for symmetrically coupling, CP2 to CP4) and the inputs of the respective transceiver pin network on the test board shall be measured and documented in the test report. The connection of signal pads using 50 Ω coaxial probe directly and ground connection shall be as short as possible. For this characterization, the coupling port shall be configured for RF immunity or emission test and the Ethernet transceivers with all components of the MDI test network (BIN) shall be removed. All other components which are directly connected to the coupling port (e.g. filter to power supply or loads) remain on the test board.

5.4.4 Single transceiver tests - coupling ports and networks

The discharge points are connected by the coupling networks to the Ethernet transceiver test circuitry. The schematic and definitions of the coupling ports, networks and pins used for unpowered ESD tests are given in Figure 5-7 and Table 5-5.



[a] The pin networks include all external mandatory components and protection and filter components for the respective pin or pins.
[b] MDIP and MDIN represent all pins of 10BASE-T1S transceiver that are connected to MDI.

Figure 5-7: Coupling ports and networks for unpowered ESD tests

Port	Type	Purpose	Components
CP1a	ESD1a	Direct ESD coupling on MDIP	metal trace for galvanic connection [a]
CP1b	ESD1b	Direct ESD coupling on MDIN	metal trace for galvanic connection [a]
CP2	ESD2	Direct ESD coupling on V_{BAT}	metal trace for galvanic connection [a]
CP3	ESD3	Direct ESD coupling on WAKE	metal trace for galvanic connection [a]

[a] The optional resistors R1a, R1b, R2 and R3 with R ≥ 200 kΩ are used to avoid static pre-charge of discharge point caused by the ESD generator. A spark over at these resistors at high test levels shall be avoided. If a static pre-charge is prevented by the ESD generator construction these resistors are not needed. Alternatively, an external resistor can be used to remove pre-charges of each discharge point before each single test.

Table 5-5: Definitions of coupling ports for unpowered ESD tests

5.5 Test communication and signals

5.5.1 General

Depending on the functionality and type of the Ethernet transceiver, different test signals are defined for communication in normal operation mode and wake-up from low power mode.

5.5.2 Test signals for normal operation mode

The communication test signal shall be used for testing Ethernet transceivers in normal operation mode. The parameters of this periodical signal are defined in Table 5-6, Figure 5-8 and Figure 5-9.

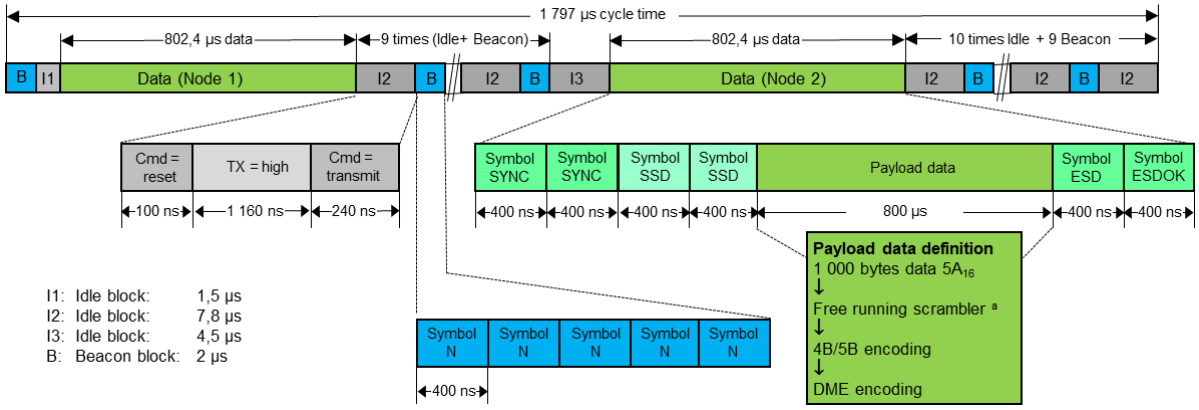
Topic	Content

Test communication for PHYs	• data frame transmission initiated by host controller
	  ○ Ethernet packet (e.g. IEEE 802.3 Ethernet frame, TCP/IP, UDP/IP...) with minimum 1000 bytes data payload
	  ○ minimum 80 % bus load
	  ○ payload data $5A_{16}$
	• data frame transmission initiated by Ethernet transceiver itself (optional, if available)
	• activation of internal BIST or PRBS test with maximum possible performance

Test communication for PMD transceiver	• cyclic TX test signal TX-PMD1 for emission tests according to Figure 5-8
	• cyclic combined test signal TX-PMD2 for immunity tests according to Figure 5-9
	  ○ TX signal
	  ○ additional gating signals, used for proper function evaluation on RX and ED signals

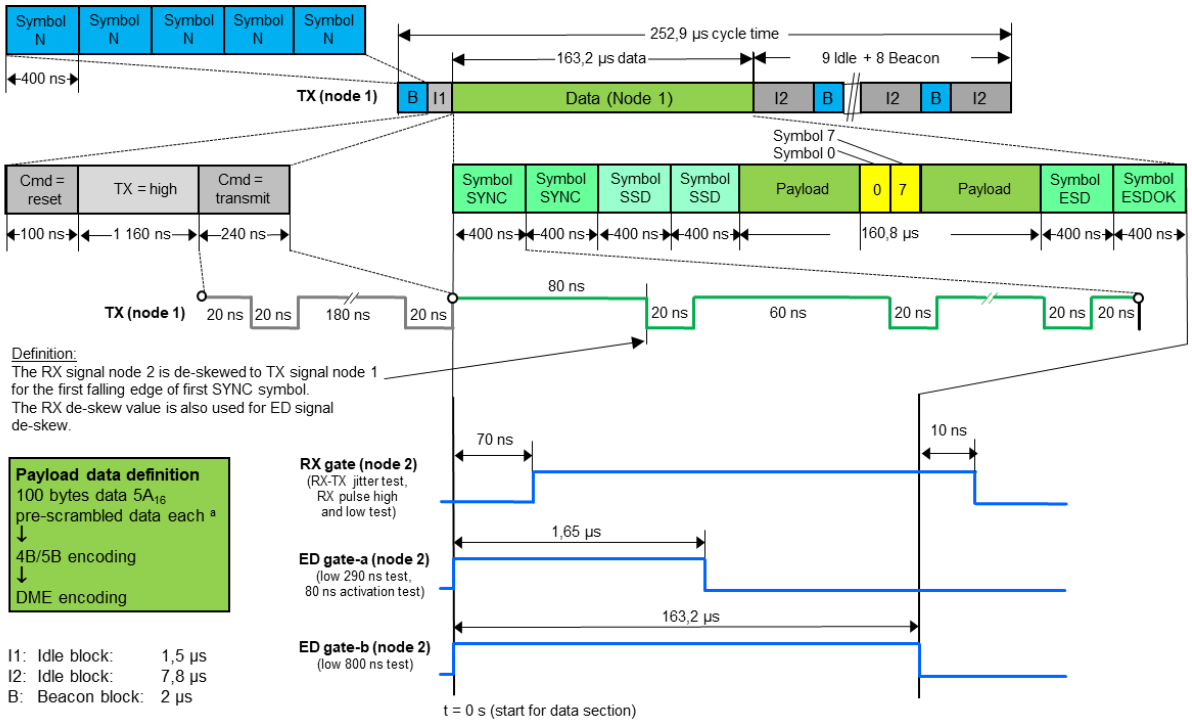
DPI distortion test	Sine wave test signal • combination of two single ended sine wave signals, generated with 50 Ω output impedance, to a differential sine wave signal • f = 12.5 MHz • amplitude 1.2 V_{pp} (± 60 mV) measured at central termination resistor for DPI distortion test • DC offset 0 V

Table 5-6: Transceiver mode configuration definition for normal operation mode



[a] Free running scrambler, 4B/5B encoding and DME encoding implementation according to [1]. Each data segment is new scrambled for the next communication cycle.

Figure 5-8: Test communication signal combination TX-PMD1 for 10BASE-T1S PMD transceiver emission tests



[a] Pre-scrambled data, 4B/5B encoding and DME encoding implementation according to [1]. Usage of same pre-scramble data for each communication cycle.

Figure 5-9: Combined test signal definition TX-PMD2 for 10BASE-T1S PMD transceiver immunity tests

5.5.3 Test signals for low power mode

Tests of unwanted wake-up will be performed without test signal applied to DUT.

To test the wanted wake-up in low power mode, the Wake-Up Pulse (WUP) definitions in 10BASE-T1S Sleep/Wake-up Specification [5] shall be used.

5.6 Evaluation criteria

5.6.1 General

To evaluate the immunity performance of Ethernet transceivers, different evaluation criteria are defined during and after exposure to disturbances.

The resulting functional status of the Ethernet transceiver shall be classified in status classes A_{IC}, C_{IC} or D_{IC} according to IEC 62132-1 [12] following the definitions in 5.6.2.

5.6.2 Evaluation criteria for functional operation modes

The evaluation criteria defined in Table 5-7 shall be used for failure monitoring. The failure validation applies to all transceivers in the test network if not otherwise defined. As soon as a transceiver under test violates the evaluation criteria, an error event for this test case is generated. In case of monitoring analog signals, (e.g. INH output signal) the reference values depend on the transceiver under test and shall be captured in undisturbed conditions before the test. These reference signals combined with the boundary values are used to generate the failure validation masks. Deviations from the defined boundary values can be agreed and shall be noted in the test report. Additional definitions for the evaluation procedure of PMD transceivers are given in Table 5-8.

Transceiver mode	Purpose	Test signal	Function	Activity
Normal for PHY and MAC-PHY	Communi-cation and cross talk	Ethernet test communication	CRC [a]	read out of available register for CRC status
			COL [b]	read out of available register for collision detection
			DTT	error check of all data which are scheduled to be sent by microcontroller or FPGA between the two nodes of the test network or error check for BIST or PRBS test [d] for data frame transmission initiate by Ethernet transceiver itself while read out of available register for status or result
			SQI/SNR [c]	read out and documentation of all available registers for indication of SQI or SNR value
			other pin functions	function validation mask using maximum deviation defined by data sheet (e.g. INH)
Normal for PMD transceiver	Communi-cation and cross talk	PMD-TX2	RX [h]	delay measurement on falling edges between TX reference signal and RX signal applied only for payload data to determine if the maximum pk-pk TIE jitter value of the RX signal meets the requirement of 19ns check for RX signal logic-high and logic-low pulse width with a limit value ≥ 12 ns
			ED [h]	check for ED de-asserted (logic-low) time applied only for data section with a limit value ≤ 290 ns and ≤ 800 ns respectively check for ED being asserted (rising edge) before 80 ns after the start of data section
			other pin functions	function validation mask using maximum deviation defined by data sheet (e.g. INH or V_{DDx} for SBCs)
Low power mode for PHY and MAC-PHY	unwanted wake-up	without	wake-up indication	function validation mask using maximum deviation defined by data sheet (e.g. INH)
	wanted wake-up	WUP	wake-up indication e	function validation mask using maximum deviation defined by data sheet (e.g. INH)
Low power mode for PMD transceiver	unwanted wake-up	without	wake-up indication	function validation mask on RX using maximum deviation defined by data sheet and in [7] / check for RX asserted (logic-high)
	wanted wake-up	WUP	wake-up indication g	function validation mask on RX using maximum deviation defined by data sheet and in [7] / check for RX de-asserted (logic-low) after Remote wake-up detection time t_{wdet} = 35 µs according to [7]

Normal, low power mode and unpowered [f] for PHY, MAC-PHY and PMD transceiver	Unwanted feedback to other communi-cation if DUT is connected to the network	Differential sine wave	DPI distortion	function validation mask for differential sine wave signal forced to MDI with failure criteria: ± 100 mV and ± 2.75 ns to the initial condition before test Trigger condition for DSO: separated Trigger output of function generator used for test signal generation

Different evaluation criteria can be agreed for special cases and shall be noted in the test report.

a If no read out of required error registers at the transceiver is possible, the error validation shall be implemented into the microcontroller software in comparable way.

b not mandatory / only possible optional failure evaluation for analysis purpose for test in normal mode with activated PLCA

c optional function, evaluation only if function is implemented

d optional function. If a BIST or PRBS test is used instead of a data frame transmission, initiate by host controller, this evaluation replaces the CRC and DTT function.

e One transceiver (DUT) of the test network is configured to operate in low power mode. The second transceiver is configured to operate in normal mode for sending out the WUP according to [5] to be detected as wake-up request by the DUT. Only the DUT is monitored and shall wake-up at least after 4 ms (maximum of TWU_Start_quiet time + maximum of TWU_Detection time according to [5].

f Both transceivers of the test network are set to unpowered mode (all power supplies off).

g One transceiver (DUT) of the test network is configured to operate in low power mode. The second transceiver is configured to operate in normal mode for sending out the WUP according to [5] to be detected as remote wake-up request by the DUT. Only the DUT is monitored and shall wake-up at least 35 µs after sending out the first falling edge of WUP (TX signal).

h Additional definitions for PMD transceiver RX signal and ED signal evaluation in normal operation mode are given in Table 5-8.

Table 5-7: Ethernet transceiver evaluation criteria for functional operation mode

Function	Evaluation procedure
RX signal [a]	1) connect the combined test signal definition TX-PMD2 according to Figure 5-9 to TX pin of node 1; 2) connect RX signal of node 2 to the DSO and perform a de-skew of the RX average value to the TX signal node 1, applied at the first falling edge of first SYNC symbol. See Figure 5-9 for more details; 3) apply the gating signal RX gate to the de-skewed RX signal for definition of signal evaluation window; 4) apply the evaluation measurements to the gated RX signal: • delay measurement on each falling edge within the evaluation window between the TX reference signal (node 1) and the gated RX signal (node 2) with a limit of ± 9.5 ns maximum jitter to implement the check for maximum pk-pk TIE jitter value of the RX signal meets the requirement of 19 ns; • measurement of RX high level time starting at 200 ns after beginning of evaluation window up to the end of the evaluation window with a limit of 12 ns; • measurement of RX low level time for whole evaluation window with a limit of 12 ns.
ED signal [a]	1) perform the RX signal de-skew measurement on RX signal; 2) connect ED signal of node 2 to the DSO and apply the measured value of RX signal delay also for ED signal de-skew. See Figure 5-9 for more details; 3) apply the gating signals ED gate-a and ED gate-b to the de-skewed ED signal for definition of the two evaluation windows; 4) apply the evaluation measurements to the gated-a ED signal: • measurement of ED asserted (logic-high) time – time from start of evaluation window to the first rising edged on ED signal with a limit of maximum 70 ns; • measurement of ED bit time de-asserted (logic-low) in the whole evaluation window with a limit of 290 ns for maximal low time 5) apply the evaluation measurements to the gated-b ED signal: • measurement of ED bit time de-asserted (logic-low) in the whole evaluation window with a limit of 800 ns for maximal low time

[a] If no read out of required error registers at the transceiver is possible, the error validation shall be implemented into the microcontroller software in a comparable way.

Table 5-8: Detailed description and application procedure for RX signal and ED signal evaluation of 10BASE-T1S PMD transceiver

5.6.3 Evaluation criteria in unpowered condition after exposure to disturbances

The input I-V characteristic (current versus voltage) of a pin under test to GND including mandatory components and protection and filter components shall be measured using e.g. a semiconductor parameter analyzer. If measurements with mandatory components or protection and filter components are not applicable they shall be removed. The test voltage range should cover or exceed the maximum voltage rating of the pin under test up to the level where e.g. break down, snap back or clamping occurs.

NOTE Commonly used test voltages are ± 50 V to ± 70 V with test current limitations of ± 0.5 mA to ± 5 mA in order to avoid damage of IC during characteristic curve measurement.

Any significant change of I-V characteristic (e.g. more than ± 5 % of maximum applied test voltage or current) measured before and after the immunity test is considered as a failure. Figure 5-10 shows a principal drawing of the maximum deviation on an I-V characteristic.

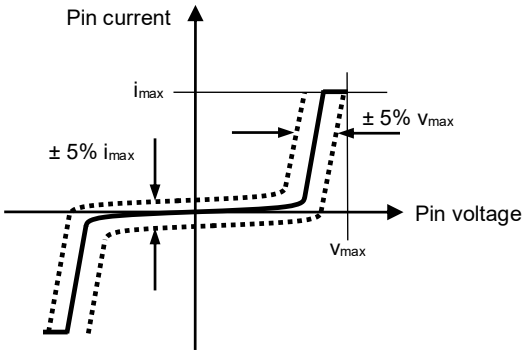


Figure 5-10: Principal drawing of the maximum deviation on an I-V characteristic

Alternatively, to the above described I-V characteristic test a parameter test according to data sheet of the DUT can be used as well to verify damages of the IC.

5.6.4 Status classes

The functional status classes for Ethernet transceivers based on the evaluation criteria are defined in Table 5-9.

Resulting status class	Requirement
A_{IC}	• no error occurred during exposure to disturbance, evaluation criteria 5.6.2 for CRC, DTT (PHY and MAC-PHY) or RX and ED (PMD transceiver) and other pin functions in normal mode, for wake-up indication in low power mode and unwanted feedback to other Ethernet communication in normal, low power and unpowered mode • no damage detected after exposure to disturbance, evaluation criteria 5.6.3, that can be checked at the end of all functional tests
$A2_{IC}$	• no error occurred during exposure to disturbance, evaluation criteria 5.6.2 for CRC and DTT (PHY and MAC-PHY) or RX and ED (PMD transceiver)
$A3_{IC}$	• no wake-up of the Ethernet transceiver operating in low power mode during exposure to disturbance, evaluation criteria 5.6.2 for unwanted wake-up
$A4_{IC}$	• successful wake-up of the Ethernet transceiver operating in low power mode on receiving the WUP or link pulse from the link partner during exposure to disturbance to disturbance, evaluation criteria of 5.6.2 for wanted wake-up
$A5_{IC}$	• no error occurred during exposure to disturbance, evaluation criteria 5.6.2 for unwanted wake-up caused by ESD discharges during exposure, proper wake-up functionality and correct change into normal mode on request during exposure
C_{IC}	• error occurred during exposure to disturbance, evaluation criteria 5.6.2 • no error occurred after exposure to disturbance, evaluation criteria 5.6.2, DUT automatically comes back into proper operation • no damage detected after exposure to disturbance, evaluation criteria 5.6.3
D_{IC}	• error occurred during exposure to disturbance, evaluation criteria 5.6.2 • no error occurred after exposure to disturbance, evaluation criteria 5.6.2, but DUT does not automatically come back into proper operation when disturbance is removed until a simple operator action (e.g. re-initialization by MDIO or SPI ($D1_{IC}$) or power off/on cycle ($D2_{IC}$)) has been done • no damage detected after exposure to disturbance, evaluation criteria 5.6.3

Table 5-9: Definition of functional status classes

5.7 DUT specific information

The following information is required for setting up and conducting the EMC tests of Ethernet transceivers and shall be supported by the semiconductor manufacturer:

- test circuit for typical application of transceiver;
- software configuration data for setting the transceiver in typical application;
- detailed information for data transmission and error register read out activity.

The following additional information should be supported by the semiconductor manufacturer, if available or needed respectively:

- EMC optimized test circuit (optimized MDI test network and optimized filter or supplier specific filter at voltage supply pins);
- information for ESD protection devices;
- layout application hints or equivalent layout requirements;
- software configuration data for setting the transceiver in EMC optimized state.

6 TEST AND MEASUREMENT

6.1 Emission of conducted RF disturbances

6.1.1 Test method

The measurement of the conducted RF emission shall be performed by 150 Ω direct coupling method according to IEC 61967-4 [10].

6.1.2 Test setup

The conducted RF emission measurement of transceiver shall be carried out using a setup according to Figure 6-1 with the coupling network as defined in Table 5-4.

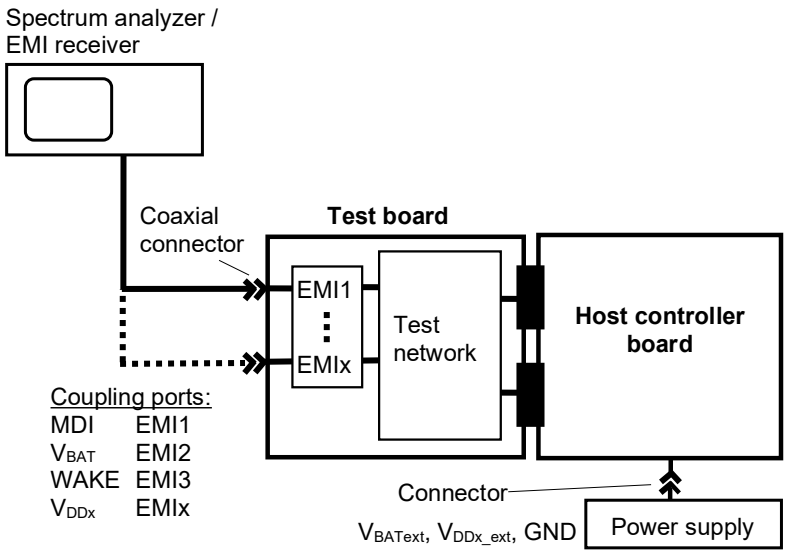


Figure 6-1: Measurement test setup for conducted RF disturbances

The test equipment definitions are the following:

- spectrum analyzer / EMI receiver;
- test board;
- host controller board;
- power supply.

6.1.3 Test procedure and parameters

The settings of the conducted RF measurement equipment are given in Table 6-1.

RF Measurement equipment	Spectrum analyzer	EMI receiver
Detector	Peak	
Frequency range	0.15 MHz to 1000 MHz (2750 MHz optional)	
Resolution bandwidth (RBW)		
150 kHz to 30 MHz:	10 kHz	9 kHz
30 MHz to 2750 MHz:	100 kHz	120 kHz
Video bandwidth (VBW)	≥ 3 times RBW	–
Numbers of sweeps	10 (max hold)	–
Measurement time per step	–	≥ 100 ms
Frequency sweep time	≥ 100 s	–
Frequency step width		
150 kHz to 30 MHz:	–	≤ 5 kHz
30 MHz to 2750 MHz:	–	≤ 50 kHz
FFT based EMI receivers can be used as well if they meet CISPR 16-1-1 [19] definitions.		

Table 6-1: Test equipment settings for conducted RF measurements

The conducted RF emission measurements shall be performed according to Table 6-2. Recommended limits are given in Annex C.1.

Transceiver mode	Coupling port type [a]	Pin	MDI test network (BIN)	Specific mode PLCA [c]
normal mode / with Ethernet test communication	EMI1	MDI	Min-BIN	X
			Std-BIN	X
			Opt-BIN	X
	EMI1a,b		Std-BIN	X
			Opt-BIN	X
	EMI1c,d		Std-BIN	X
			Opt-BIN	X
	EMI2 [b]	V_{BAT}	Opt-BIN	X
	EMI3 [b]	WAKE	Opt-BIN	X
	EMI4 [b]	V_{DDx}	Opt-BIN	X

X A test shall be performed.

a For definition of coupling ports see Table 5-4.

b For transceivers with different interfaces to the host microcontroller emission measurements at both nodes of the transceiver network with those different interface configurations are required. Alternatively, the host interface configuration for one node can be changed between the two available interfaces for emission measurement.

c PLCA mode is only valid for PHY and MAC-PHY.

Table 6-2: Conducted emission measurements

6.2 Immunity to conducted RF disturbances

6.2.1 Test method

The test of the conducted RF immunity shall be performed by using the DPI test method according to IEC 62132-4 [14].

6.2.2 Test setup

In general, the conducted RF immunity tests of transceiver shall be carried out using a setup according to Figure 6-2 with the coupling network as defined in in Table 5-4.

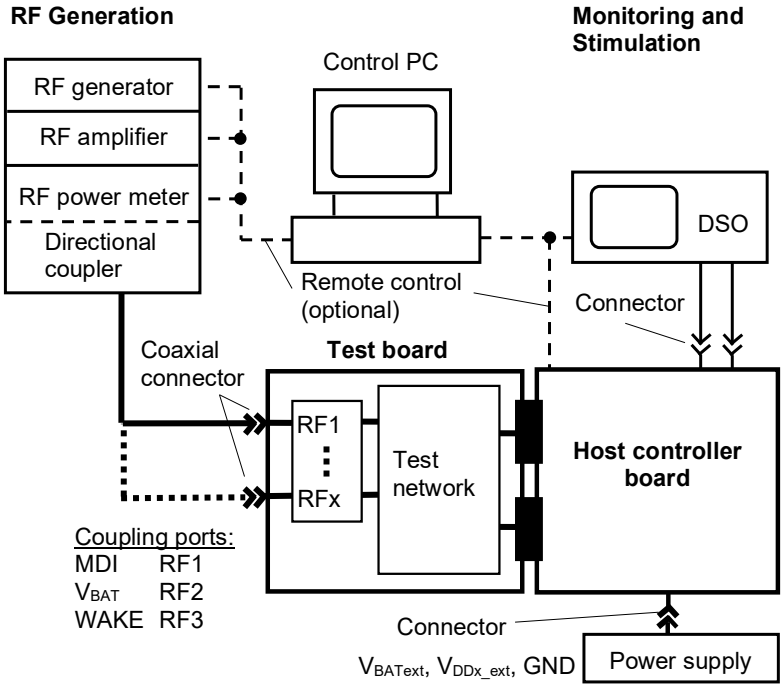


Figure 6-2: DPI general test setup

To test the unwanted feedback to other Ethernet communication (DPI distortion test) of a transceiver in different operation modes, connected to the Ethernet test network, the test setup given in Figure 6-3 is defined.

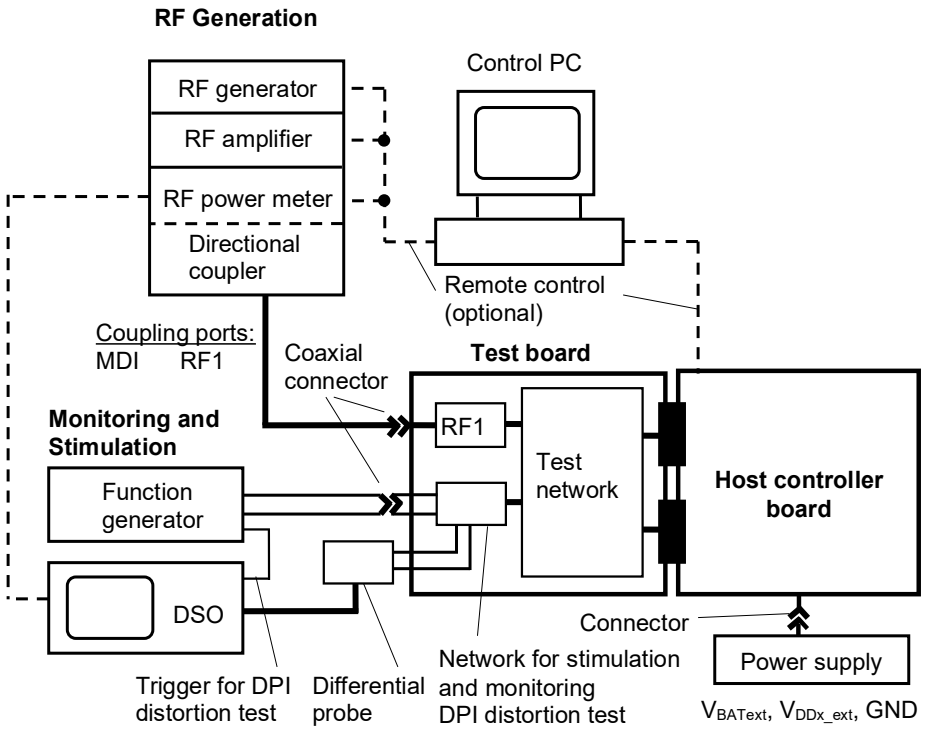


Figure 6-3: Test setup for DPI distortion test

The test equipment definitions are the following:

- RF generator;
- RF amplifier (output power P ≥ 10 W);
- power meter with directional coupler;
- test board;
- host controller board;
- power supply;
- control PC (optional);
- digital storage oscilloscope (DSO, optional);
- function generator, two channels, 50 Ω output impedance (only used for DPI distortion test);
- high impedance, low capacitive (max. 1 pF) DSO differential probe (only used for DPI distortion test).

6.2.3 Test procedure and parameters

To determine the conducted RF immunity of the Ethernet transceiver, tests with the parameters given in Table 6-3 shall be carried out.

Item	Parameter	
Frequency	Range	Step
	1 MHz to 10 MHz	0.25 MHz
	10 MHz to 100 MHz	1 MHz
	100 MHz to 200 MHz	2 MHz
	200 MHz to 400 MHz	4 MHz
	400 MHz to 1000 MHz	10 MHz
Minimum forward power	10 dBm (10 mW)	
Maximum forward power	39 dBm (8 W)	
Power step size	0.5 dB	
Dwell time	1 s	
Modulation	f = 1 MHz to 1000 MHz: CW f = 1 MHz to 380 MHz: AM 80 % 1 kHz ($\hat{P}_{AM} = \hat{P}_{CW}$) f = 380 MHz to 1000 MHz: PM 1 kHz, ton 500 µs ($\hat{P}_{PM} = \hat{P}_{CW}$)	
Test procedure for evaluation of functional status class A_{IC}	Before each single test If shall be ensured that the transceiver is in proper function in relation to function status class A_{IC} for the related test case (e.g. no CRC and DTT error occur, or DUT is set into low power mode for test of unwanted or wanted wake-up). Searching for malfunction in relation to function status classes $A1_{IC}$, $A3_{IC}$ or $A4_{IC}$ during the complete dwell time while power is stepwise increased. An optimized control procedure can be used to reduce the test time but ensuring that there are no artifacts in the RF inputs during frequency or power steps. EXAMPLE: Procedure for each frequency step: • start with maximum forward power or with the level that caused a malfunction at the previous frequency step, • in case of malfunction at this power level reduce the power level by 6 dB and repeat the test, • increase the power stepwise until a malfunction occurs or the maximum forward power is reached, • the immunity level at this frequency is the maximum forward power that causes no malfunction	
Evaluation procedure for functional status class C_{IC} or D_{IC}	Apply the test power for each frequency step and evaluate the functional status after each test.	

Table 6-3: DPI test specification

The tests for functional status class A_{IC} evaluation shall be performed according to Table 6-4. For each test an immunity threshold curve with the forward power as the parameter shall be determined and documented in a diagram in the test report. Recommended limits are given in Annex 0.

Transceiver mode	Coupling port type [g]	Pin	MDI test network (BIN)	Failure validation for error / function					
				CRC, DTT	SNR or SQI [f]	Sum or RX, ED [c]	DPI dis-tortion	Other pin function	Wake-up
Ethernet system configuration				PLCA [i]					
normal mode / Ethernet test communication	RF1	MDI	Min-BIN [a]			X			
			Std-BIN [b]		(X)	X		(X)	
			Opt-BIN [b]		X	X		X	
	RF1c,d		Std-BIN [b]	(X)	(X)	X			
			Opt-BIN [b]	X	X	X			
	RF1e,f		Opt-BIN [b]		X	X			
	RF2	V_{BAT}	Opt-BIN [a]			X		X	
	RF3	WAKE	Opt-BIN [a]			X		X	
normal mode /no communication	RF1	MDI	Opt-BIN [b]				X [h]		
low power mode / DPI distortion test and test of unwanted wakeup [d]	RF1	MDI	Min-BIN [a]						X
			Std-BIN [b]						X
			Opt-BIN [b]						X
	RF1c,d		Std-BIN [b]						X
			Opt-BIN [b]						X
	RF1e,f		Std-BIN [b]						X
			Opt-BIN [b]						X
	RF2	V_{BAT}	Opt-BIN [a]						X
	RF3	WAKE	Opt-BIN [a]						X
low power mode / test of wanted wakeup [d,e]	RF1	MDI	Min-BIN [a]						X
			Std-BIN [b]						X
			Opt-BIN [b]						X
	RF1c,d		Std-BIN [b]						X
			Opt-BIN [b]						X
	RF1e,f		Std-BIN [b]						X
			Opt-BIN [b]						X
unpowered / DPI distortion test	RF1	MDI	Opt-BIN [b]				X [h]		

X	A test shall be performed.
(X)	Test is optional. It shall be performed if there is no definition of Opt-BIN for DUT.
a	Test shall be done with CW and modulation (AM, PM), maximum test power 36 dBm.
b	Test shall be done only with modulation (AM, PM), maximum test power 39 dBm.
c	Sum error: CRC and DTT or BIST / PRBS tests status evaluated in parallel for PHY and MAC-PHY, RX and ED evaluation for PMD transceiver.
d	Test of wanted or unwanted wake up or Ethernet signal activity detection, depending on implemented function.
e	One node is set to low power mode, second node sends a periodic signal to be detected as wakeup by node in low power mode.
f	Documentation of SNR value (e.g. signal quality indicator or MSE value) if implemented for PHY and MAC-PHY. The test should be done for information only. There is no immunity limit defined.
g	For definition of coupling ports see Table 5-4.
h	Test shall be performed for frequency range 1 MHz to 40 MHz with two different central bus terminations R_{t3} = 50 Ω (representing the transceiver when used on an end node in the application) and R_{t3} = 100 Ω (representing the transceiver when is used on a drop node in the application) while decentral bus terminations R_{t1} and R_{t2} are removed.
i	PLCA mode is only valid for PHY and MAC-PHY.

Table 6-4: DPI tests for functional status class A_{IC} evaluation of Ethernet transceivers

The tests for functional status class C_{IC} or D_{IC} shall be performed according to Table 6-5. Recommended limits are given in Annex 0.

Transceiver mode	**Coupling port** [d]	**Pin**	**MDI test network (BIN)**	**Failure validation for error / function** **Sum or ED, RX** [c]
Ethernet system configuration				PLCA [f]
normal mode / Ethernet test communi-cation	RF1 [a]	MDI	Opt-BIN [e]	X
	RF2 [b]	V_{BAT}	Opt-BIN [e]	X
	RF3 [b]	WAKE	Opt-BIN [e]	X

X	A test shall be performed.
a	Test shall be done with modulation (AM, PM), maximum test power 39 dBm.
b	Test shall be done with CW, maximum test power 36 dBm.
c	Sum error: CRC and DTT evaluated in parallel for PHY and MAC-PHY, RX and ED evaluation for PMD transceiver.
d	For definition of coupling ports see Table 5-4.
e	The test shall be performed with Std-BIN if there is no definition of Opt-BIN for DUT.
f	PLCA mode is only valid for PHY and MAC-PHY.

Table 6-5: DPI tests for functional status class C_{IC} or D_{IC} evaluation of Ethernet transceivers

6.3 Immunity to impulses

6.3.1 Test method

The test of the impulse immunity shall be performed by using the non-synchronous transient injection method according to IEC 62215-3 [16].

6.3.2 Test setup

The impulse immunity tests of transceiver shall be carried out using a setup according to Figure 6-4 with the coupling network as defined in Table 5-4.

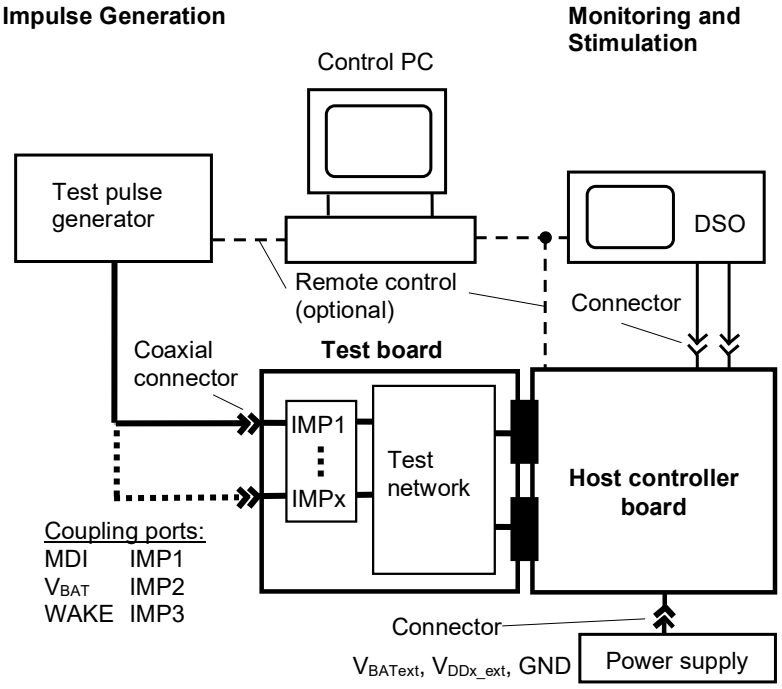


Figure 6-4: Impulse immunity test setup

The test equipment definitions are the following:

- test pulse generator (according to ISO 7637-2 [18]);
- test board;
- host controller board;
- power supply;
- control PC (optional);
- digital storage oscilloscope (DSO, optional).

6.3.3 Test procedure and parameters

To determine the immunity of the transceiver against impulses defined in ISO 7637-2 [18], tests with the definitions and parameters given in Table 6-6 and Table 6-7 shall be performed.

Item	Definitions and parameters
Test pulses	1, 2a, 3a, 3b (see Table 6-7)
Amplitude step size	10 V
Dwell time	1 min for tests of functional status class A_{IC} 10 min for tests of functional status class C_{IC} or D_{IC}
Test procedure for functional status class AIC	Before each single test If shall be ensured that the transceiver is in proper function in relation to function status class A_{IC} for the related test case (e.g. no CRC or DTT error occur, or DUT is set into low power mode for test of unwanted or wanted wake-up). Searching for malfunction in relation to function status classes $A1_{IC}$, $A3_{IC}$ or $A4_{IC}$ during a dwell time of minimum 5 s while pulse amplitude is stepwise increased up to the defined test pulse levels (as e.g. given in Table 6-7). At the determined maximum voltage, the achieved immunity level shall be proved with a dwell time of 1 min. An optimized control procedure can be used to reduce test time. The immunity level is the maximum amplitude that causes no malfunction.
Test procedure for functional status class C_{IC} or D_{IC}	Apply the defined test pulses (as e.g. given in Table 6-7) and evaluate the functional status after each test.

Table 6-6: Impulse immunity test specification

Test pulse [a]	Vs max [V]	Pulse repetition frequency (1/t1) [Hz]	Ri [Ω]	Remarks
1	− 100	2	10	battery shall be off only during the pulse
2a	+ 75	2	2	–
3a	− 150	10 000	50	–
3b	+ 100	10 000	50	–

a according to ISO 7637-2 [18], pulse amplitudes are defined under open load conditions, parameters for rise time and duration of 12 V systems are set as default. Other pulse values for target applications in other power domains as e.g. 24 V or pulses defined in IEC standards (e.g. IEC 61000-4-4 and IEC 61000-4-5) can be used if required of the transceiver application.

Table 6-7: Impulse immunity test parameters

The tests for functional status class A_{IC} evaluation shall be performed according to Table 6-8. For each test, an impulse immunity level shall be determined and documented in the test report. Recommended limits are given in Annex C.3.

Transceiver mode	Coupling port type [d]	Pin	MDI test network (BIN)	Failure validation for error / function				
				CRC, DTT	SNR or SQI [f]	Sum or RX, ED [a]	Other pin function	Wake-up
Ethernet system configuration				PLCA [e]				
normal mode / Ethernet test communi-cation	IMP1	MDI	Min-BIN			X		
			Std-BIN	(X)	(X)	X	(X)	
			Opt-BIN	X	X	X	X	
	IMP2	V_{BAT}	Opt-BIN			X	X	
	IMP3	WAKE	Opt-BIN			X	X	
low power mode / test of unwanted wakeup [b]	IMP1	MDI	Min-BIN					X
			Std-BIN					X
			Opt-BIN					X
	IMP2	V_{BAT}	Opt-BIN					X
	IMP3	WAKE	Opt-BIN					X
low power mode / test of wanted wakeup [b,c]	IMP1	MDI	Min-BIN					X
			Std-BIN					X
			Opt-BIN					X

X A test shall be performed.

(X) Test is optional. It shall be performed if there is no definition of Opt-BIN for DUT.

a Sum error: CRC and DTT or BIST / PRBS tests status evaluated in parallel for PHY and MAC-PHY, RX and ED evaluation for PMD transceiver.

b Test of wanted or unwanted wake up or Ethernet signal activity detection, depending on implemented function.

c One node is set to low power mode, second node sends a periodic signal to be detected as wakeup by node in low power mode.

d For definition of coupling ports see Table 5-4.

e PLCA mode is only valid for PHY and MAC-PHY.

Table 6-8: Impulse immunity tests for functional status class A_{IC} evaluation of Ethernet transceivers

The tests for functional status class C_{IC} or D_{IC} shall be performed according to Table 6-9. Recommended limits are given in Annex C.3.

Transceiver mode	Coupling port [b]	Pin	MDI test network (BIN)	Failure validation for error / function Sum or RX, ED [a]
Ethernet system configuration				PLCA [d]
normal mode / Ethernet test communi-cation	IMP1	MDI	Opt-BIN [c]	X
	IMP2	VBAT	Opt-BIN [c]	X
	IMP3	WAKE	Opt-BIN [c]	X

X A test shall be performed.

a Sum error: CRC, COL and DTT evaluated in parallel for PHY and MAC-PHY, RX and ED evaluation for PMD transceiver.

b For definition of coupling ports see Table 5-4.

c The test shall be performed with Std-BIN if there is no definition of Opt-BIN for DUT.

d PLCA mode is only valid for PHY and MAC-PHY.

Table 6-9: Impulse immunity tests for functional status class C_{IC} or D_{IC} evaluation of Ethernet transceivers

6.4 Electrostatic Discharge (ESD)

6.4.1 Test method

The ESD immunity test shall be performed in powered and unpowered mode by using the direct discharge method according to ISO 10605 [17].

6.4.2 Test setup

6.4.2.1 Test setup for powered test

ESD tests in powered mode tests of Ethernet transceivers shall be carried out using a test setup according to Figure 6-5 and Figure 6-6.

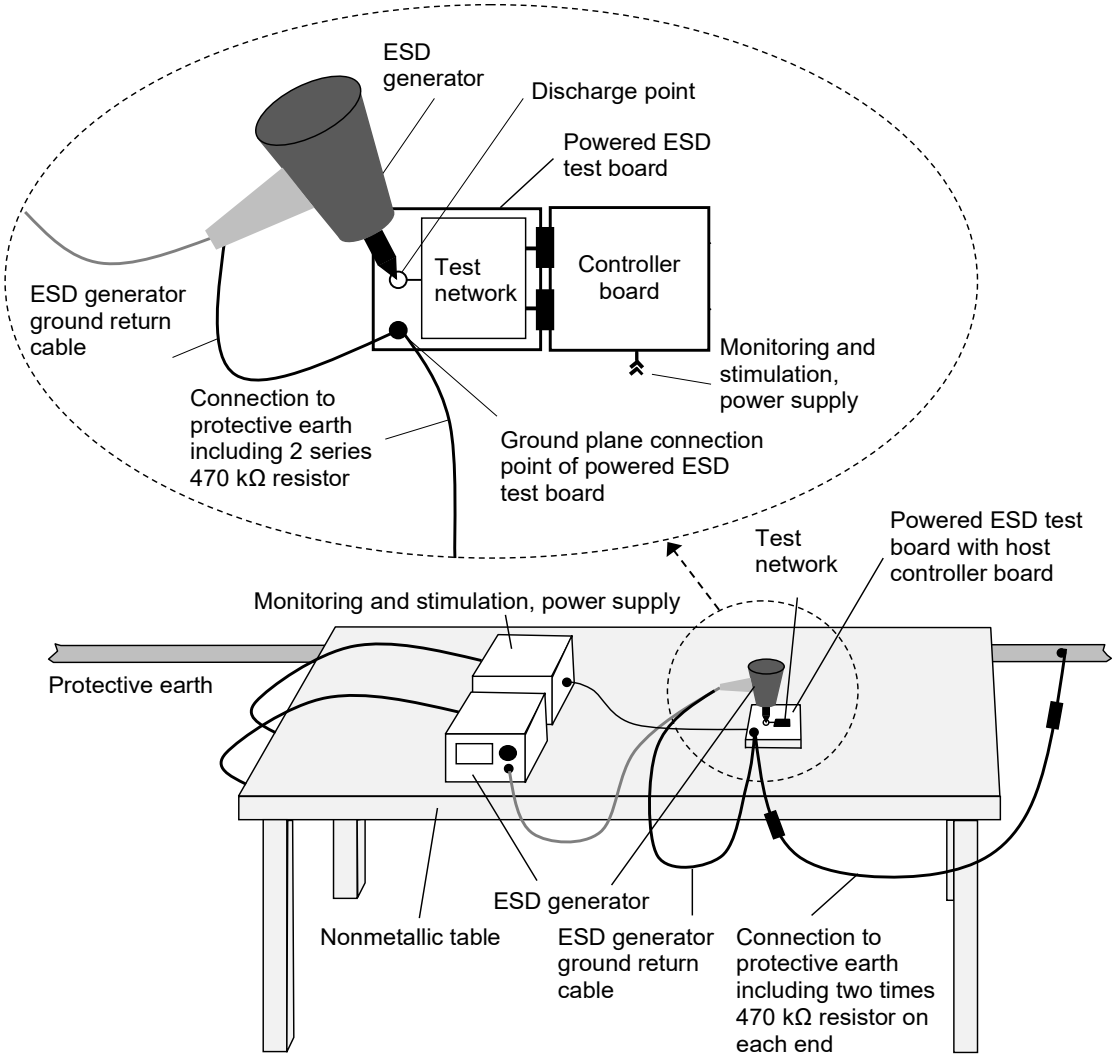


Figure 6-5: Powered ESD test setup – principal arrangement

The test equipment definitions for powered ESD tests are the following:

- ESD generator (according to ISO 10605 [17], discharge storage capacitor C = 150 pF and discharge resistor R = 330 Ω);

- powered ESD test board;
- host controller board;
- auxiliary equipment as power supply, monitoring and stimulation (optional, only needed for tests in powered mode and functional pre/post validation).

The ESD generator ground return cable shall be directly connected to ground plane of the powered ESD test board. This point shall be connected to protective earth of the electrical grounding system of the test laboratory. An optional ground plane with a minimum size of 0.5 m × 0.5 m can be used but shall be also connected to protective earth.

The tip of the ESD generator shall be directly contacted with the discharge point ESD1 IND of the powered ESD test board (described in Annex B) for testing.

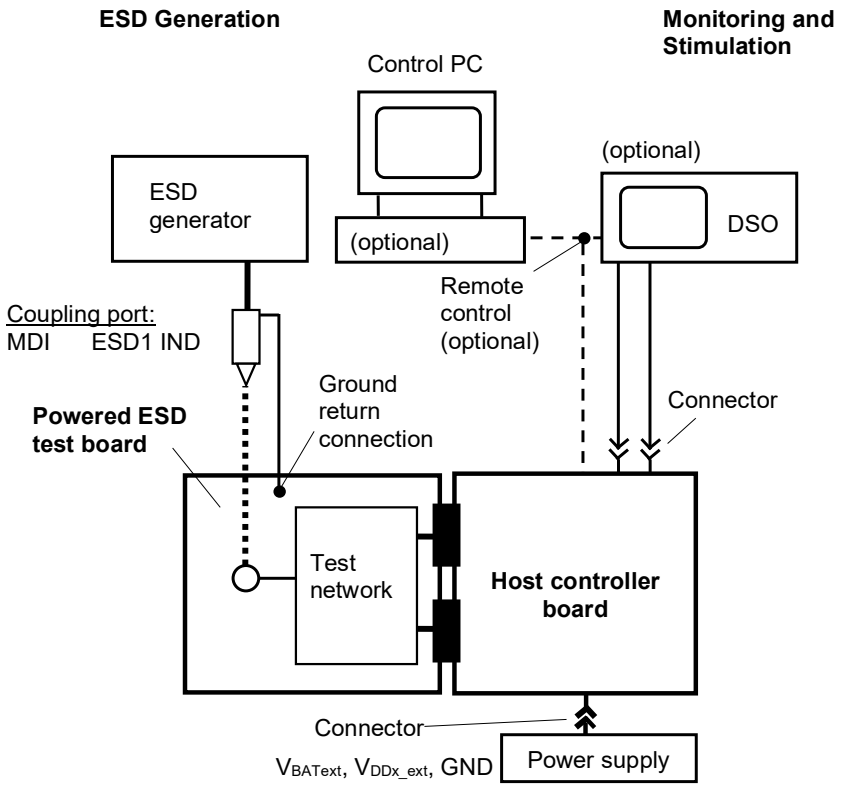


Figure 6-6: Powered ESD test setup – stimulation and monitoring

6.4.2.2 Test setup for unpowered test

Unpowered ESD tests of Ethernet transceivers shall be carried out using a test setup according to Figure 6-7 for ESD tests itself and according to Figure 6-8 for function validation pre and post ESD test.

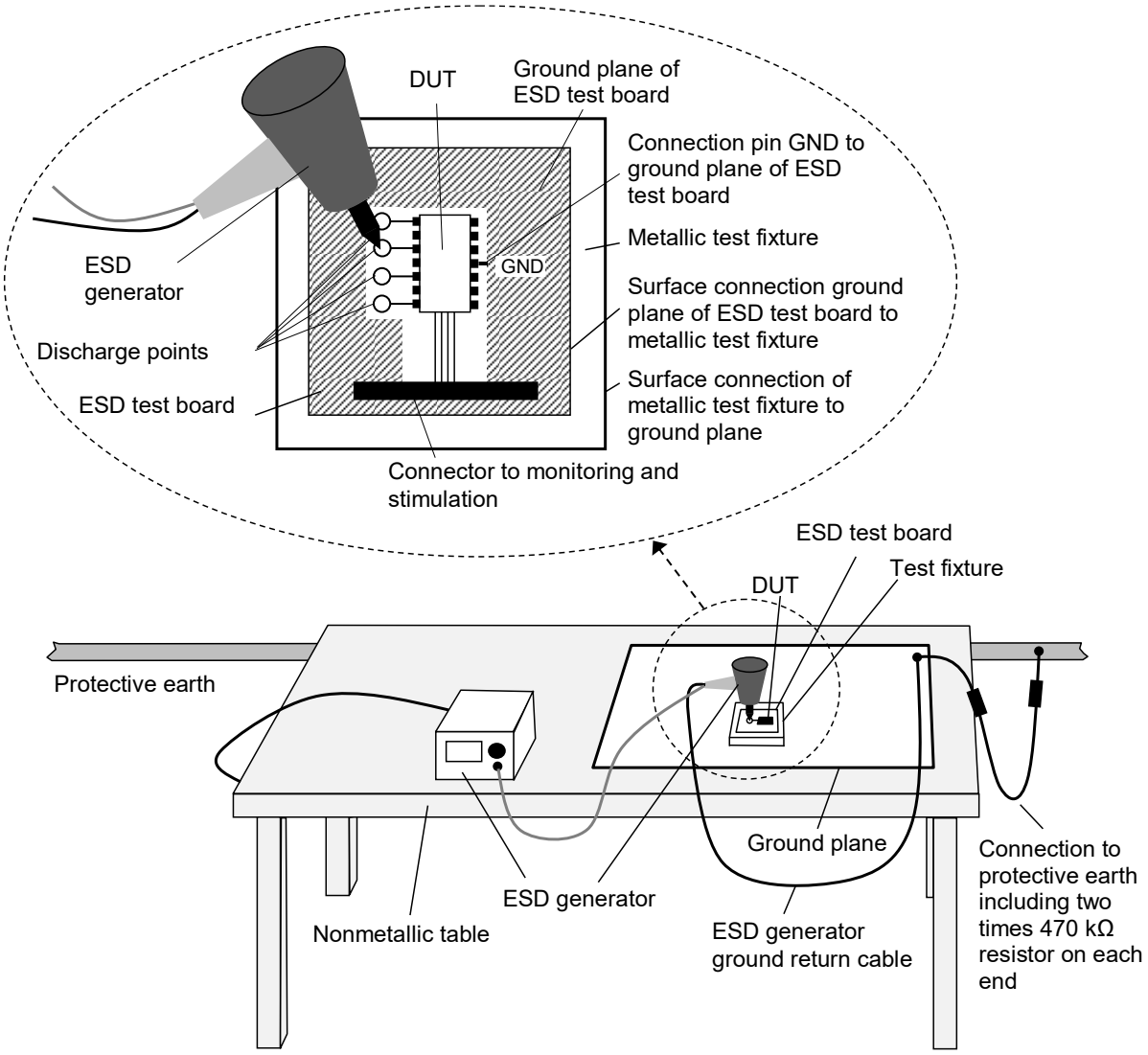


Figure 6-7: Unpowered ESD test setup – principal arrangement

The test equipment definitions for unpowered ESD tests are the following:

- ESD generator (according to ISO 10605 [17], discharge storage capacitor C = 150 pF and discharge resistor R = 330 Ω);
- ESD test board;
- test fixture;
- ground plane.

The ground plane with a minimum size of 0.5 m × 0.5 m shall be connected to protective earth of the electrical grounding system of the test laboratory. The ESD generator ground return cable shall be directly connected to this ground plane.

The metallic test fixture positions the ESD test board and directly connects the ESD test board ground plane to the reference ground plane. The ground connection of the test fixture shall be connected to ground plane with low impedance and low inductance. This surface connection should have a contact area of at least 4 cm^2. If necessary, conductive (copper) tape can be used in addition to increase the contact area.

The tip of the ESD generator shall be directly contacted with one of the discharge points ESD1a, ESD1b, ESD2 and ESD3 of the ESD test board (described in Annex B) for testing.

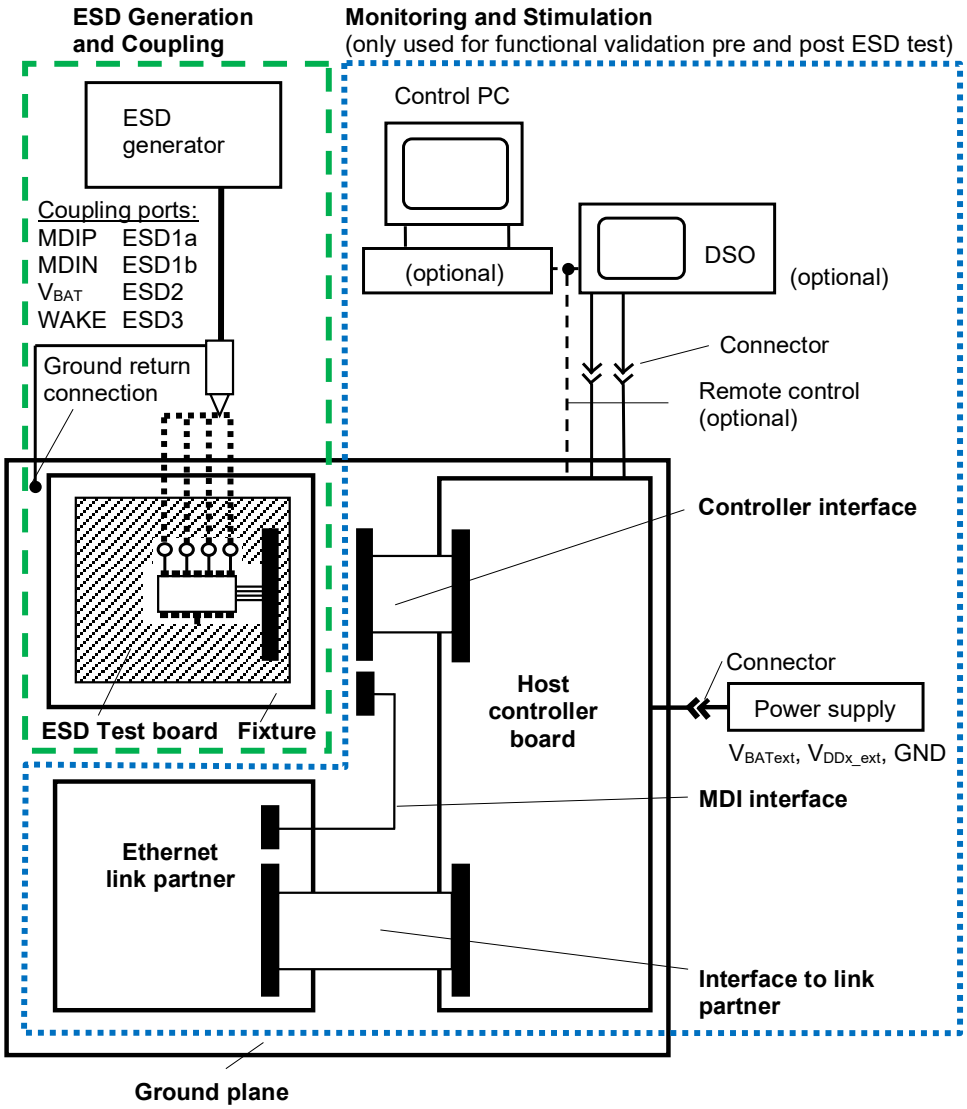


Figure 6-8: Unpowered ESD test setup – stimulation and monitoring for function validation pre and post ESD test

The test equipment definitions for function validation pre and post ESD test are the following:

- ESD test board;
- test fixture;
- host controller board;
- board with Ethernet link partner (test board as used for RF emission, DPI and transient tests is proposed), and
- auxiliary equipment as power supply, monitoring and stimulation.

For tests in unpowered mode the interfaces between the ESD test board and the host controller board (controller interface) and ESD test board and Ethernet link partner (line interface) are disconnected during test. For functional pre and post validation they are connected.

6.4.3 Test procedure and parameters

To determine the ESD robustness of Ethernet transceiver tests shall be carried out with the parameters given in Table 6-10.

Item	Parameter
Type of discharge	contact
Discharge circuit	R = 330 Ω, C = 150 pF
Discharge voltage levels and voltage steps for powered ESD tests	start level: 0.5 kV stop level: VESD_damage or 8 kV voltage step: 0.5 kV for VESD < 1 kV 1 kV for VESD ≥ 1 kV
Discharge voltage levels unpowered ESD tests	start level: 1 kV stop level: VESD_damage or 15 kV voltage step: 1 kV

Table 6-10: ESD test specification

The tests in powered mode for functional status class A_{IC}, C_{IC} and D_{IC} evaluation shall be performed according to Table 6-11. For each test an ESD immunity level shall be determined and documented in the test report. Recommended limits are given in Annex C.4.

Transceiver mode	Coupling port [a]	Pin	MDI test network (BIN)	Failure validation for status class			
				$A2_{IC}$ (CRC, DTT error)	$A5_{IC}$ (unwanted wake up)	C_{IC}	D_{IC}
Ethernet system configuration				PLCA [c]			
Test sequence from low power mode to normal mode	ESD1 IND	MDI	Opt-BIN [b]	X			

X A test shall be performed with a minimum of 3 DUTs according to the following procedure:

1. disconnect DUT from power supply
2. perform a reference measurement for the I/V characteristic curve (pin to GND) on all MDI pins
3. connect DUT to power supply and set it to low power mode
4. perform 3 discharges with positive polarity on discharge pad DP IND with 5 s delay between the discharges with evaluation of unwanted wake-up according to function status class $A5_{IC}$ during test
5. send wake-up signal by Ethernet link partner and check for proper wake-up function according to function status class $A5_{IC}$ after test
6. set DUT to normal mode with Ethernet test communication
7. perform a reference test for proper function according to function status class $A5_{IC}$
8. perform 3 discharges with positive polarity on discharge pad DP IND with 5 s delay between the discharges with evaluation of function status classes $A2_{IC}$ (only valid for PHY and MAC-PHY) and C_{IC} according to Table 5-9 during test
9. disconnect DUT from power supply
10. connect the pin or discharge pad to the ground reference plane via a 1 MΩ resistor to ensure zero potential on the pin (only needed if resistor R_{CP1t} is not used).
11. perform the I/V characteristic curve measurement (tested pin to GND) and failure validation of function status classes DIC according to Table 5-9
12. proceed with point 1) to 11) with negative polarity
13. proceed with point 1) to 12) with the next higher ESD test voltage up to damage of the tested pin or maximum defined ESD test level is reached

a For definition of coupling ports see Table 5-4.

b The test shall be performed with Std-BIN if there is no definition of Opt-BIN for DUT.

c PLCA mode is only valid for PHY and MAC-PHY.

Table 6-11: ESD tests in powered mode for functional status class A_{IC}, C_{IC} and D_{IC} evaluation of Ethernet transceivers

The tests in unpowered mode for functional status class D_{IC} evaluation shall be performed according to Table 6-12. For each test, an ESD immunity level shall be determined and documented in the test report. Recommended limits are given in Annex C.4.

Transceiver mode	Coupling port [a]	Pin	MDI test network (BIN)	Failure validation for status class D_{IC}
Unpowered	ESD1a, ESD1b	MDI	Min-BIN	X
			Std-BIN	X
			Opt-BIN	X
	ESD2	V_{BAT}	Opt-BIN	X
	ESD3	WAKE	Opt-BIN	X

X A test shall be performed with a minimum of 3 transceiver according to the following procedure:

1. perform reference test for proper function (check sum error) while connecting DUT to power supply and set it to normal mode
2. perform a reference measurement for the I/V characteristic of all pins to be tested (pin to GND)
3. apply 3 ESD pulses with positive polarity on discharge point ESD2 (VBAT) with 5 s delay in between, after each single ESD pulse the pin or discharge point should be discharged to the ground to ensure zero potential before the next ESD pulse (only needed if resistor R1a and R1b are not used)
4. perform failure validation according to 5.6.3
5. proceed with points 3) to 4) with discharge points ESD3 (WAKE)
6. proceed with points 3) to 4) with discharge points ESD1a (MDI+ network)
7. proceed with points 3) to 4) with discharge points ESD1b (MDI- network)
8. proceed with point 3) to 7) with negative polarity
9. proceed with point 3) to 8) with the next higher ESD test voltage up to damage of the tested pin or maximum defined ESD test level is reached

If one pin is damaged, a new IC should be used to continue the test of the other pins.

a For definition of coupling ports, see Table 5-5.

Table 6-12: ESD tests in unpowered mode for functional status class D_{IC} evaluation of Ethernet transceiver ICs

ANNEX A: TEST CIRCUITS FOR ETHERNET TRANSCEIVERS

A.1 General

The Ethernet test circuits define the details of the complete test circuitry for testing Ethernet transceivers in functional operating modes under network condition and for a single transceiver for ESD. It defines mandatory components, protection and filter components and optional components for Ethernet transceiver functions and components for coupling networks, decoupling networks, which are used for power supply, stimulation, monitoring and testing of the DUT.

The Ethernet test circuit is basic for the test results and their interpretation.

A.2 Test circuit for functional tests

A general drawing of the test circuit diagram of the Ethernet test network for testing 10BASE-T1S transceivers in functional operating modes for conducted tests is given in Figure A-1 .

A 10BASE-T1S Ethernet node consists of transceiver (A10, A20) with external mandatory components and protection and filter components (X11, X12, X13, X14, X21, X22, X23, X24) and the BIN (L10, L20, C12, C13, C22, C23, R11, R12, R13, R21, R22, R23, C11, C21) and decoupling networks at monitored pins (R16, R26).

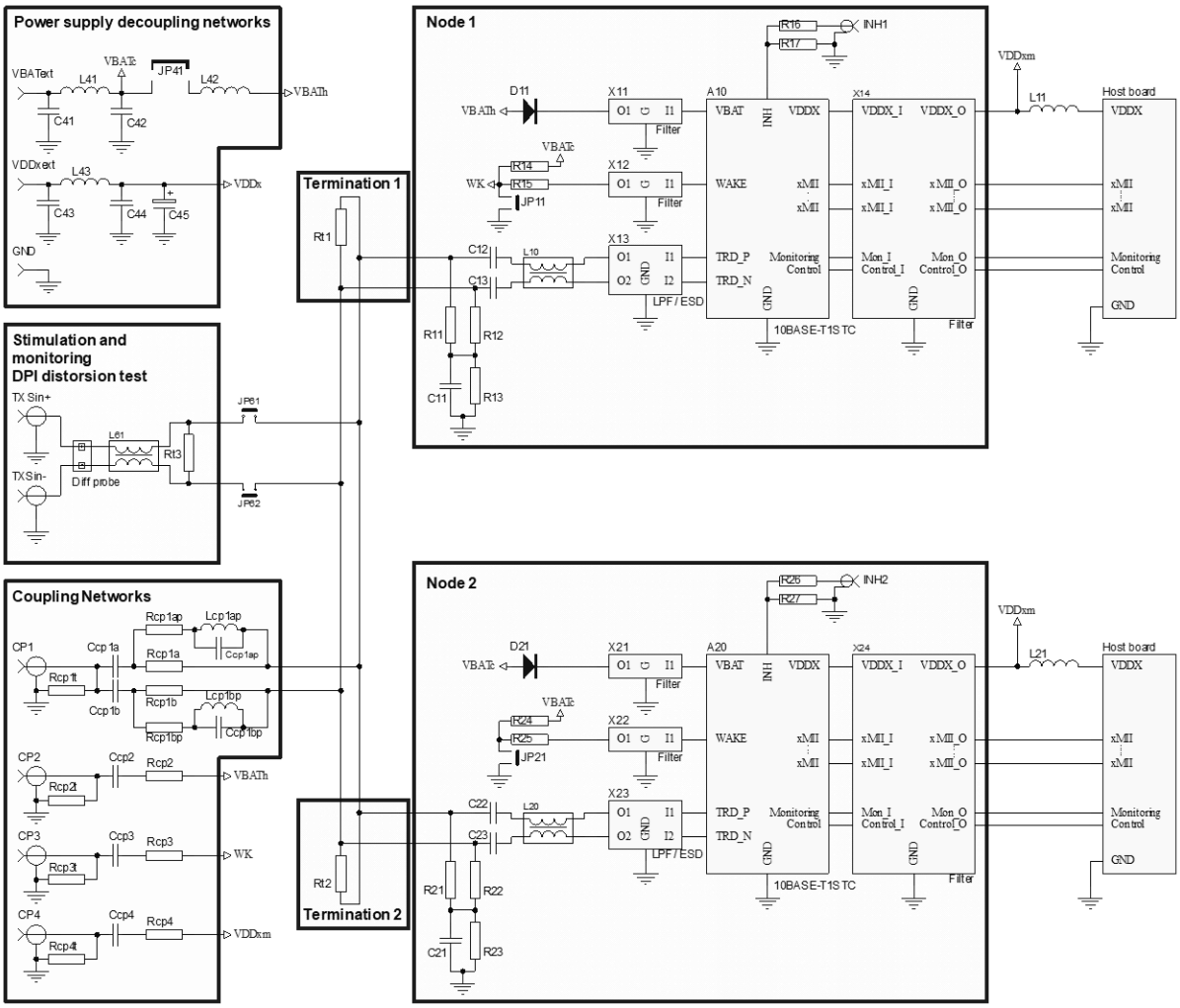
All external mandatory components and protection and filter components (except components for MDI) shall be used according to the specification of the Ethernet transceiver. If special components for MDI are defined in the specification, this circuitry should be tested in addition.

The resistor values at the WAKE pin shall be set to the maximum specified value (default R = 3.3 kΩ) for R14, R24 and to the minimum specified value (default R = 33 kΩ) for R15, R25.

For RF decoupling of monitored pins INH the default value for resistor (R16, R26) is set to R = 1 kΩ for all tests.

In order to avoid a floating voltage at pin INH in sleep mode a pull down resistor (R17, R27) shall be used with values according to the IC specifications (default R = 10 kΩ).

For decoupling of external power supplies two-stage LC-filters (L41, L42, C41, C42 and L43, C43, C44, C45) are used separately for V_{BAT} and V_{DDx}. The impedance of L42 should be greater than 400 Ω in the frequency range of interest. Jumper JP41 is opened to disconnect the supply voltage and the RF decoupling filter network at V_{BAT} during the impulse tests at V_{BAT}. In this case the voltage supply V_{BAT} is directly provided via the IMP2 coupling network.



Key Components

A10, A20	Ethernet transceiver 10BASE-T1S
C11, C21	capacitor *C* = 100 nF (optional, given value is default value, placement depends on test case)
C12, C13, C22, C23	capacitor *C* = 100 nF
C41, C43	capacitor *C* = 1 nF
C42, C44	capacitor *C* = 330 pF
C45	capacitor *C* = 22 µF
Ccp1a, Ccp1b, Ccp2, Ccp3, Ccp4	capacitor (value depends on test case)
Ccp1ap, Ccp1bp	capacitor (value depends on test case), only used for RF immunity tests with frequency selective unbalance coupling on MDI
D11, D21	diode, general purpose rectifier type
JP11, JP21	Jumper
L10, L20	Common mode choke that fulfills the requirements of [2] (placement depends on test case)

L11, L21	inductor L = 4.7 µH (only populated for emission measurements at V_{DDx})
L41, L43	inductor L = 47 µH
L42	impedance should be greater than 400 Ω in the frequency range of interest
Lcp1ap, Lcp1bp	inductor (value depends on test case), only used for RF immunity tests with frequency selective unbalance coupling on MDI
R11, R12, R21, R22	resistor R = 1.5 kΩ (± 1 %, optional, given value is default value, placement depends on test case)
R13, R23	resistor R = 100 kΩ (optional, given value is default value, placement depends on test case)
R14, R24	resistor R = 3.3 kΩ
R15, R25	resistor R = 33 kΩ
R16, R26	resistor R = 1 kΩ
R17, R27	resistor R = 10 kΩ
Rcp1a, Rcp1b, Rcp2, Rcp3, Rcp4	resistor (value dependent on test)
Rcp1pa, Rcp1pb	resistor (value dependent on test), only used for RF immunity tests with frequency selective unbalance coupling on MDI
Rcp1t, Rcp2t, Rcp3t, Rcp4t	resistor (value dependent on test)
Rt1, Rt2	resistor R = 100 Ω (± 1 %)
Rt3	resistor R = 100 Ω (± 1 %) or R = 50 Ω (± 1 %) (only used for DPI distortion test, placement and value depend on test case, if used: Rt1 and Rt2 needs to be unpopulated)
X11, X12, X13, X14, X21, X22, X23, X24	Filter network or external circuitry defined by semiconductor manufacturer

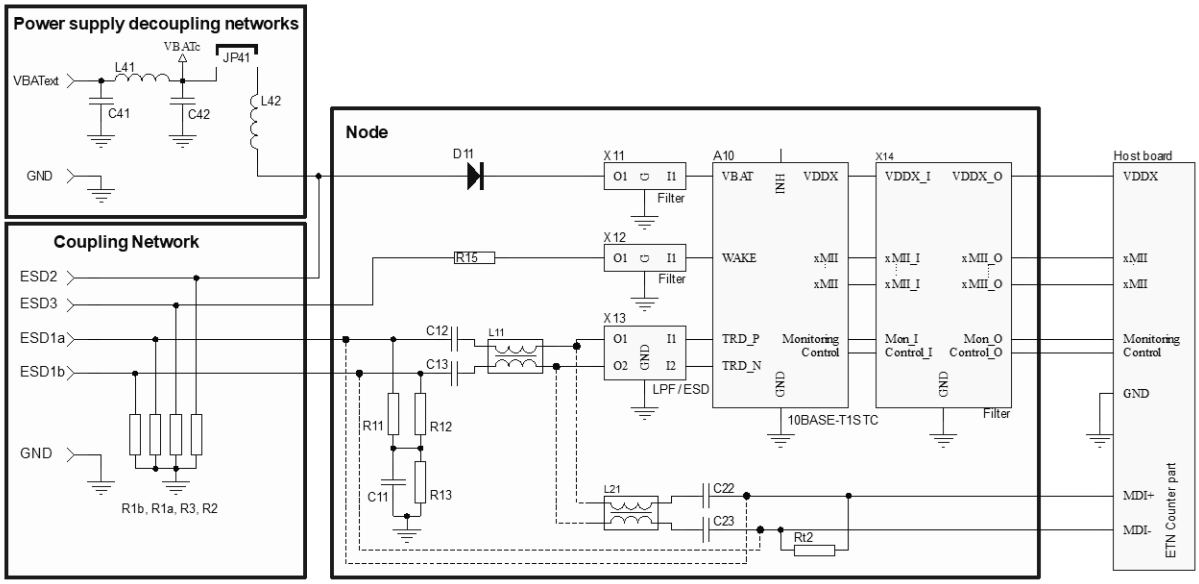
Figure A-1: General circuit diagram of conducted test network for functional test of 10BASE-T1S Ethernet

A.3 Test circuit for unpowered ESD test

A general drawing of the test circuit diagram for testing immunity against ESD of Ethernet transceivers in unpowered mode is given in Figure A-1.

The test circuit for unpowered ESD tests consists of a single Ethernet transceiver (A10) with external mandatory components and protection and filter components (X11, X12, X13, X14), the BIN (L11, C12, C13, R11, R12, R13, C11) and a second BIN (L21, C22, C23) for connection to the Ethernet counterpart node. It is also possible to connect the Ethernet counterpart node for functional operation check after ESD test at the line side of AC coupling capacitors (C12, C13) without using the second BIN network. In this case any parasitic feedback to the ESD coupling path shall be avoided (e.g. spark-over to GND or other parts of the test circuit).

The value for the series resistor on the pin WAKE (R15) should be chosen according to the IC specification with minimum value (default R = 33 kΩ). All external mandatory components and protection and filter components (except components for MDI) shall be used according to the specification of the Ethernet transceiver. If special components for MDI are defined in the specification, this circuitry should be tested in addition. The default parameters of the passive components in ESD coupling paths are for capacitors a tolerance of ± 10 %, material X7R according to electronic industry association (EIA-198) or similar, voltage rating ≥ 50 V and dimension 1206 or 0805. The default parameters for resistors are ±1 % tolerance and dimension 1206 or 0805. For tests in unpowered mode the discharge points ESD1a, ESD1b, ESD2 and ESD3 and optional discharge resistors (R1, R2, R3, R4 with R ≥ 200 kΩ) will be used for ESD coupling. The second BIN (L21, C22, C23) and termination (Rt2) is not connected during ESD test but is used to check the proper functionality of the transceiver after each single ESD test. Alternatively, the connection to the Ethernet link partner device for function check after the ESD test can be done direct at the MDI ESD discharge points and the second BIN remains unconnected. In this case, the used interconnection shall be implemented to avoid parasitic ESD discharge to GND up to the maximum applied ESD test voltage.



Key Components	
A10	Ethernet transceiver 10BASE-T1S
C11	capacitor *C* = 100 nF (optional, given value is default value, placement depends on test case)
C12, C13, C22, C23	capacitor *C* = 100 nF
C41	capacitor *C* = 1 nF
C42	capacitor *C* = 330 pF
D11	diode, general purpose rectifier type
L11, L21	Common mode choke that fulfills the requirements of [2] (placement depends on test case)
L41	inductor *L* = 47 µH
L42	impedance should be greater than 400 Ω in the frequency range of interest
R1a, R1b, R2, R3	resistor $R \geq 200$ kΩ (placement is optional)
R11, R12	resistor *R* = 1.5 kΩ (± 1 %, optional, given value is default value, placement depends on test case)
R13	resistor *R* = 100 kΩ (optional, given value is default value, placement depends on test case)
R15	resistor *R* = 33 kΩ
Rt2	resistor *R* = 100 Ω (± 1 %)
X11, X12, X13, X14	Filter network or external circuitry defined by semiconductor manufacturer

Figure A-1: General circuit diagram for unpowered ESD tests of Ethernet transceivers

ANNEX B: TEST CIRCUIT BOARDS

B.1 Test circuit board for transceiver network configuration

For functional conducted and powered ESD tests of Ethernet transceivers the test network shall be designed on a printed circuit board. To ensure good RF characteristics of transceiver with external circuitry and the coupling and decoupling networks, an equal design of the circuitry for node 1 and node 2 on a minimum four-layer PCB with a GND layer should be used. A layout example for functional conducted tests is shown in Figure B-1.

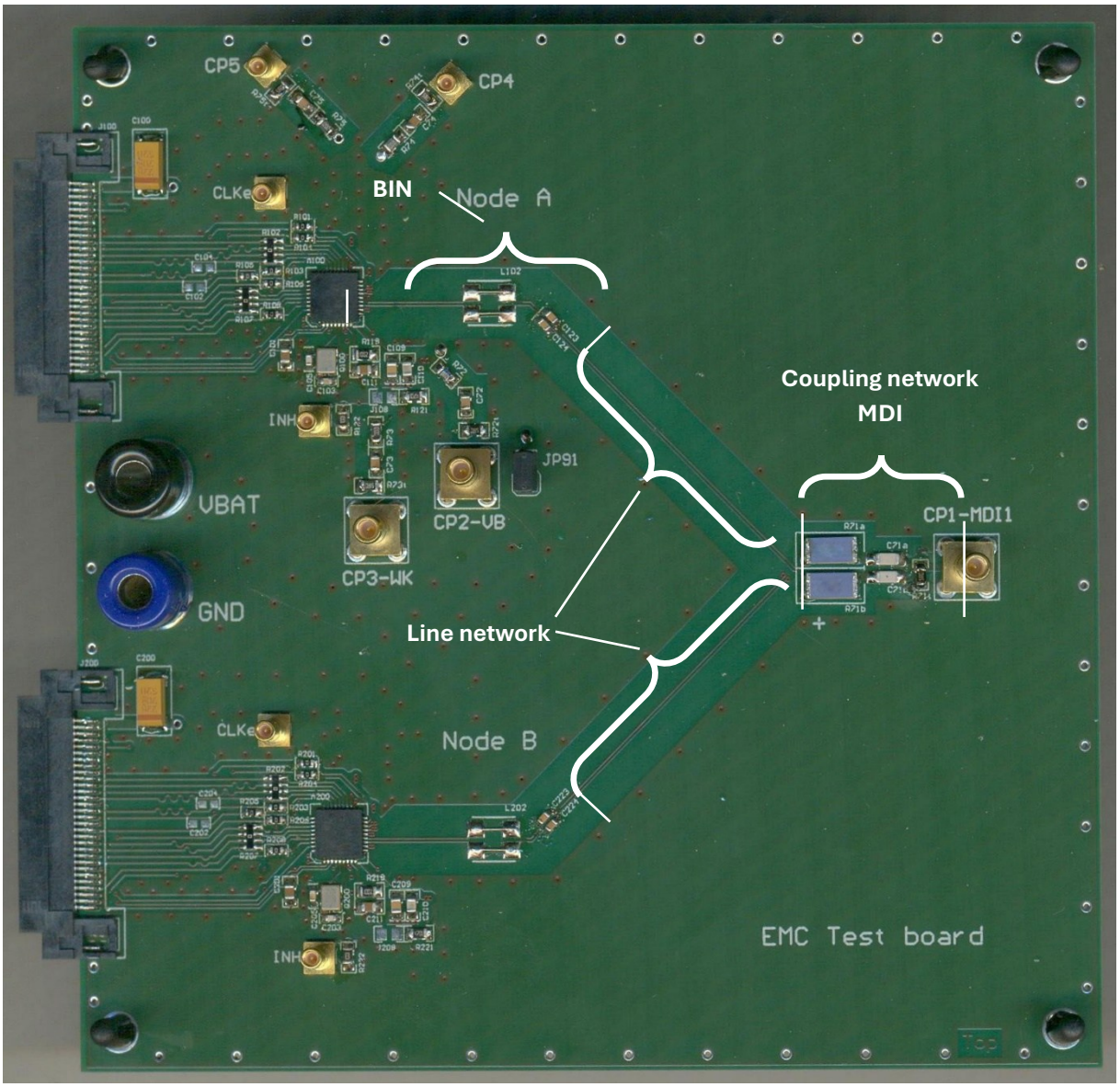


Figure B-1 Example of functional conducted test board for Ethernet transceiver ICs

The traces of line network between the BIN of node 1 and the BIN of node 2 (see Figure B.1) shall have a length of 90 (± 10) mm with a differential line impedance of 100 (± 5) Ω. The single-ended trace impedance of BI_DA+ and BI_DA- shall be 50 (± 5) Ω. Voiding on the reference plane used for the MDI traces underneath the

BIN components (coupling capacitors, CM termination resistors, CMC) and termination resistors should be avoided. This is in order to maintain a consistent parasitic capacitance from one implementation to the next.

The length of the coupling paths on the test board should be kept as short as possible to ensure a parasitic inductance value of traces less than 5 nH. The DUT shall be soldered on the test board to minimize parasitic effects. For proper shielding, all connections from the test board to peripheral devices should be connected via coaxial printed circuit board sockets except for the filtered power supplies and GND.

A layout example for powered ESD tests is shown in Figure B.2. The pad for the discharge points ESD1 IND shall be carried out in a way that a proper contact to the discharge tip of the test generator is ensured (e.g. by rounded vias in the layout of the ESD test board).

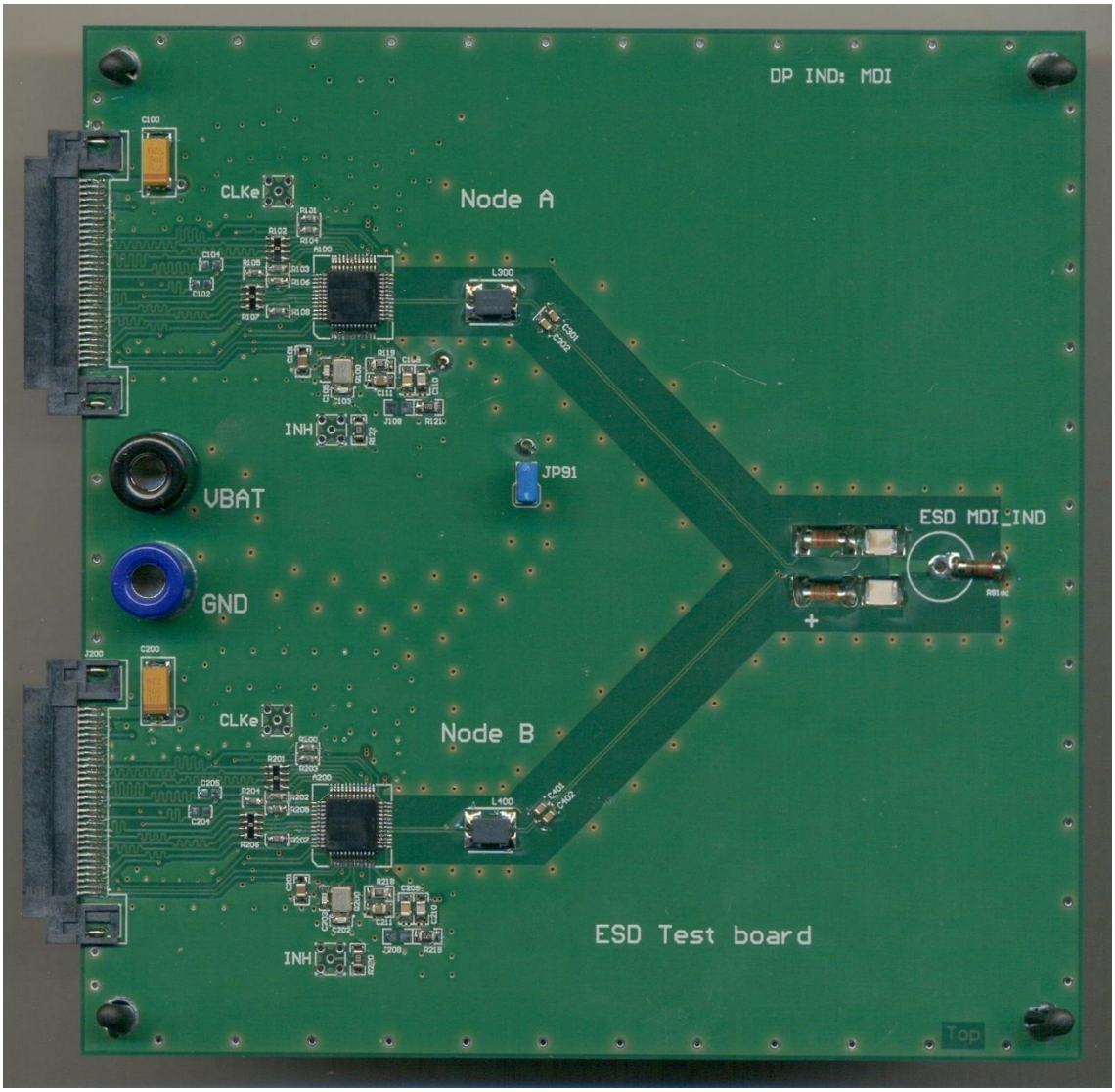


Figure B-2: Example of powered ESD test board for Ethernet transceivers ICs

B.2 Test circuit board for single transceiver configuration

For unpowered ESD tests, a printed circuit board shall be used. At least a four-layer construction of the PCB with GND layer shall be chosen. The pads for the discharge points ESD1a to ESD3 shall be carried out in a

way that a proper contact to the discharge tip of the test generator is ensured (e.g. by rounded vias in the layout of the ESD test board). The discharge point shall be directly connected by a trace to the respective pin under test of the transceiver. The passive components of the network shall be placed close to the transceiver to reduce parasitic effects. The DUT should be soldered on the test board to ensure application like conditions and avoid parasitic setup effects by sockets. The insulation distance between the signal lines and pads of the passive components and the extensive ground area should be designed in a way that a spark over at these points can be prevented up to the intended test voltage level. A layout example is shown in Figure B-3 and Figure B-4

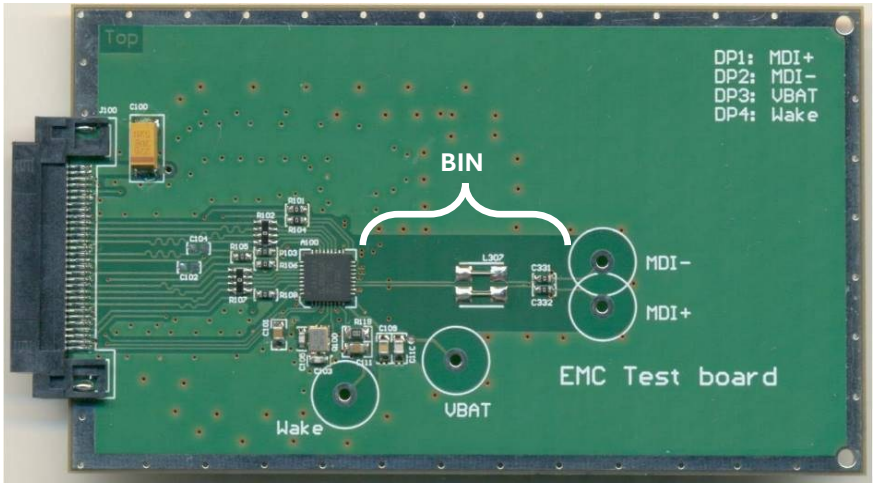


Figure B-3: Example of unpowered ESD test board for Ethernet transceivers ICs, top layer

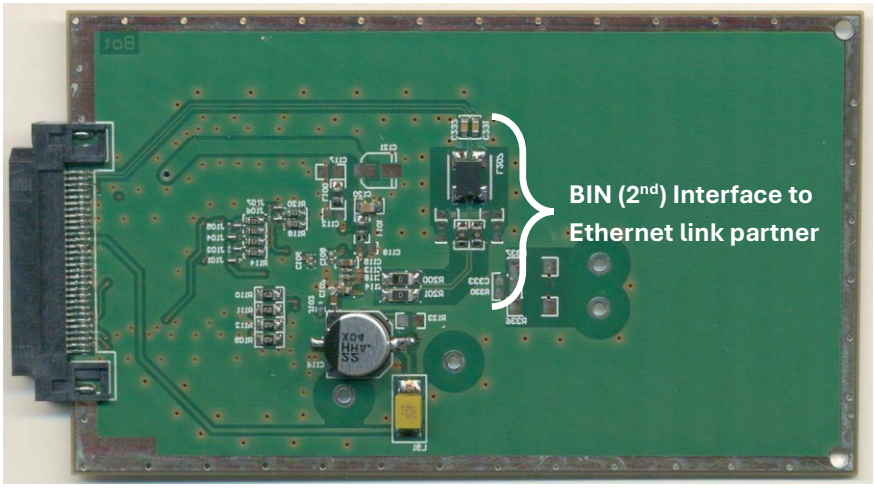


Figure B-4: Example of unpowered ESD test board for Ethernet transceivers ICs, bottom layer

Further requirements for the ESD test board are defined in Table B-1.

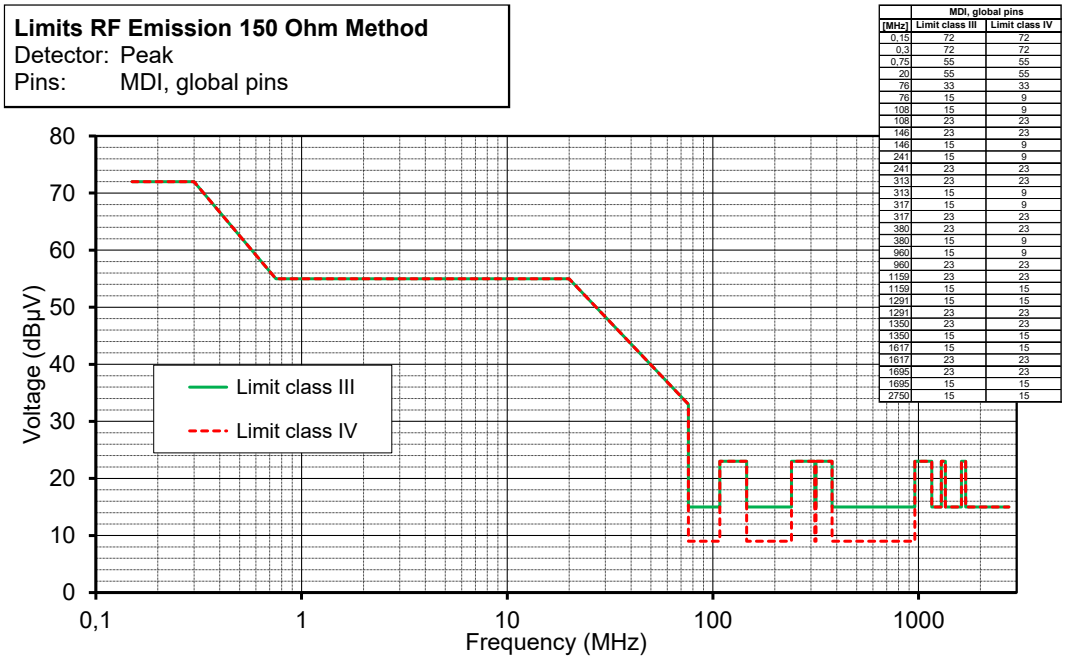
Parameter	Value
Trace length between BIN and discharge point	15 (±5) mm
Trace width of the conducting path	0.254 mm

Table B-1: Parameter ESD test circuit board

ANNEX C: RECOMMENDED LIMITS FOR TESTS

C.1 Emission of RF disturbances

For evaluation of RF emissions at the MDI (symmetrical coupling and ± 5 % unbalanced coupling), other global pins and voltage supply pins the limits given in Figure C.1 and Figure C-2 are recommended. The required limit class depend on the application conditions and will be defined by the customer.



	MDI, global pins	
[MHz]	Limit class III	Limit class IV
0,15	72	72
0,3	72	72
0,75	55	55
20	55	55
76	33	33
76	15	9
108	15	9
108	23	23
146	23	23
146	15	9
241	15	9
241	23	23
313	23	23
313	15	9
317	15	9
317	23	23
380	23	23
380	15	9
960	15	9
960	23	23
1159	23	23
1159	15	15
1291	15	15
1291	23	23
1350	23	23
1350	15	15
1617	15	15
1617	23	23
1695	23	23
1695	15	15
2750	15	15

Figure C-1: Recommended RF emission limits for MDI and other global pins

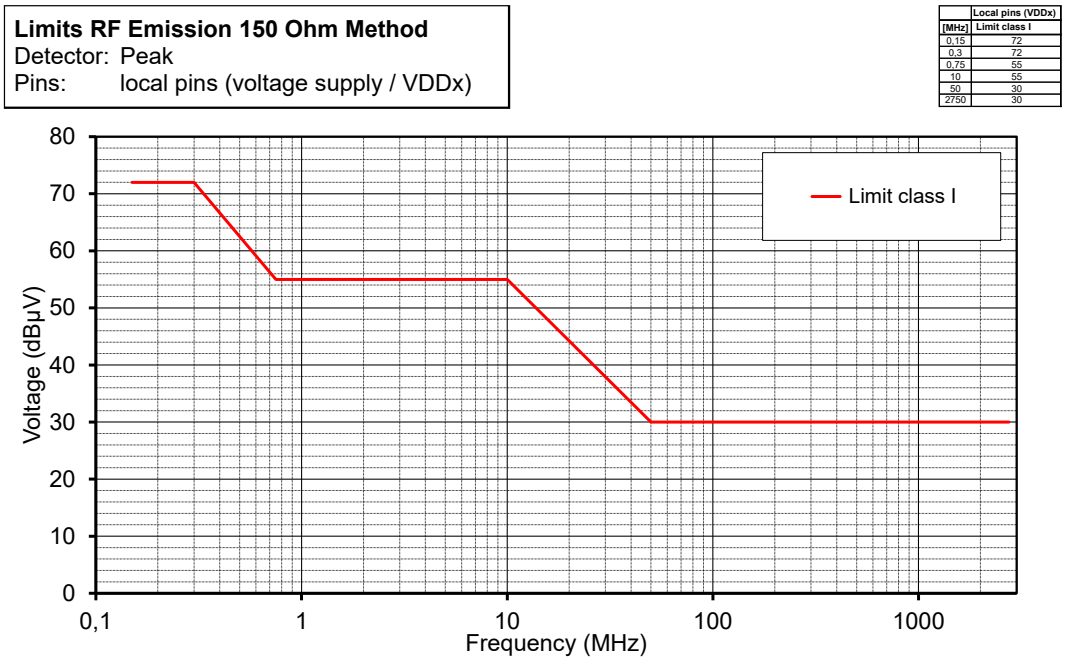


Figure C-2: Recommended RF emission limits for local pins

C.2 Immunity to RF disturbances

For evaluation of RF immunity at the MDI (symmetrical coupling, ± 10 % and frequency selective unbalanced coupling) and other global pins the limits given in Figure C-3 for damage tests and Figure C-4 for malfunction tests are recommended.

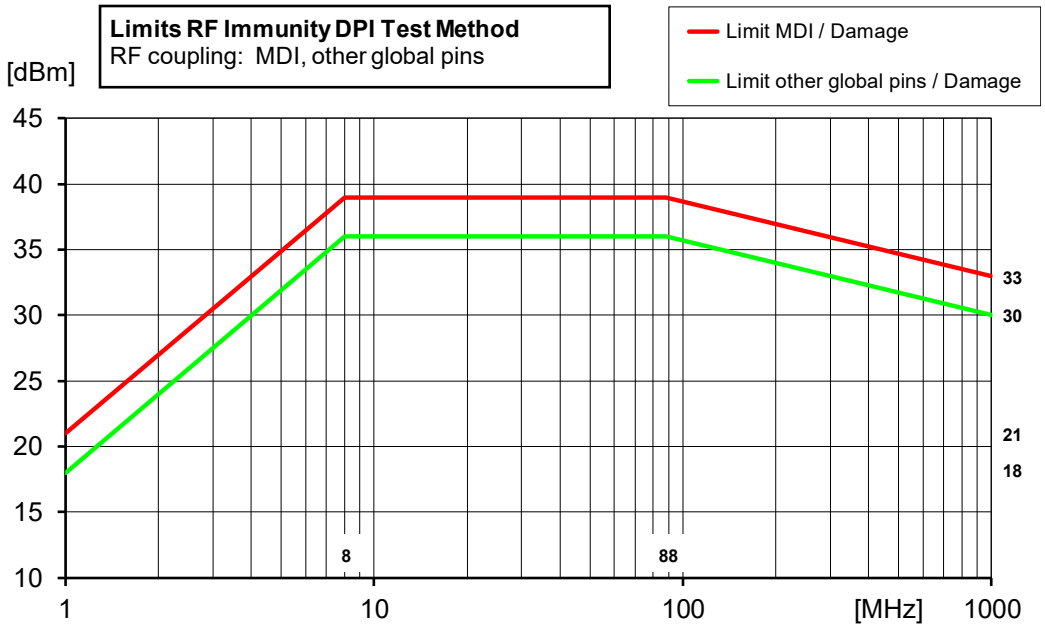


Figure C-3: Recommended limits for RF immunity damage tests

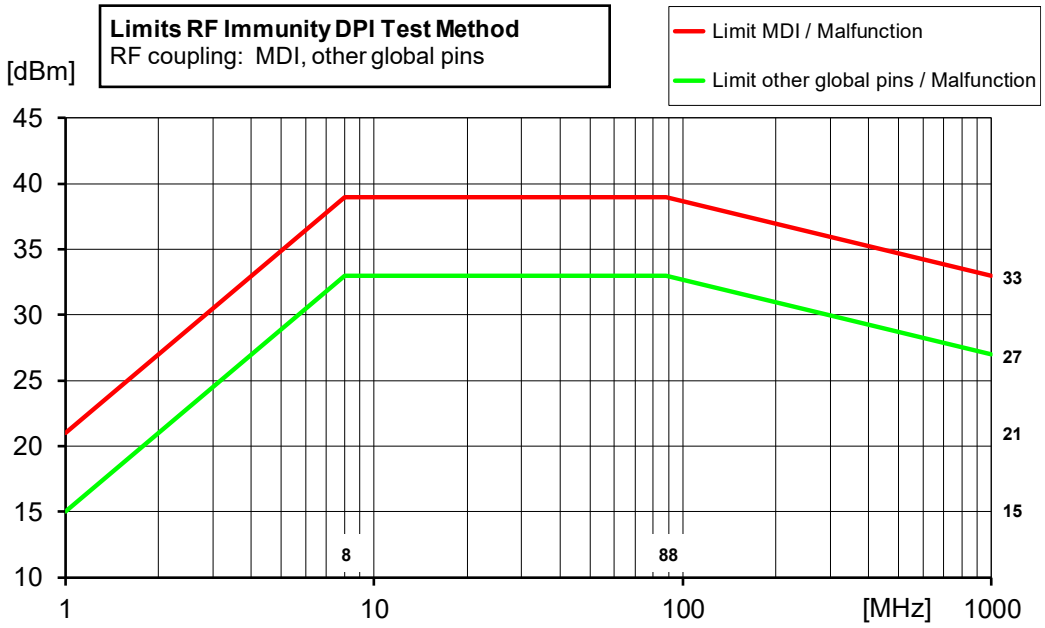


Figure C-4: Recommended limits for RF immunity malfunction tests

C.3 Immunity to transients

For evaluation of transient immunity at the MDI and other global pins only limits for damage are recommended:

Test pulse	Vs [V]
1	- 100
2a	+ 75
3a	- 150
3b	+ 100

Table C-1: Recommended voltage levels for transient immunity to damage

C.4 ESD

For ESD immunity to damage of the MDI with standard or optimized BIN in powered and unpowered mode and other global pins in unpowered mode ± 6 kV ESD test voltage is recommended.

For ESD immunity tests of the MDI with standard or optimized BIN in powered mode to function status class $A3_{IC}$ (no unwanted wake-up caused by ESD discharges, proper wake-up functionality and correct change into normal mode on request) ± 3 kV ESD test voltage is recommended.

ANNEX D: (INFORMATIVE) RADIATED RF EMISSION AND RF IMMUNITY TEST OF ETHERNET TRANSCEIVER

D.1 General

This annex describes tests of Ethernet transceiver in regards to radiated disturbances coupled via the IC package instead of the IC pins. It contains definitions for test methods, test conditions, performance criteria, test procedures, test setups, test boards and recommended limits. The test methods covered by this annex include

- the radiated RF emission, and
- the radiated RF immunity.

D.2 General configuration for transceiver network

For evaluation of radiated RF emission and RF immunity characteristic of an Ethernet transceiver in functional operation mode a minimal Ethernet test network consisting of one Ethernet transceiver (DUT) and an Ethernet link partner of the same type (including line termination) is used. The test configuration in general consists of line termination (Term 1), Ethernet transceivers with external mandatory components and protection and filter components (Ethernet node) in a minimal test network, where filtered power supplies, signals, monitoring probes and coupling networks are connected as shown in Figure D-1.

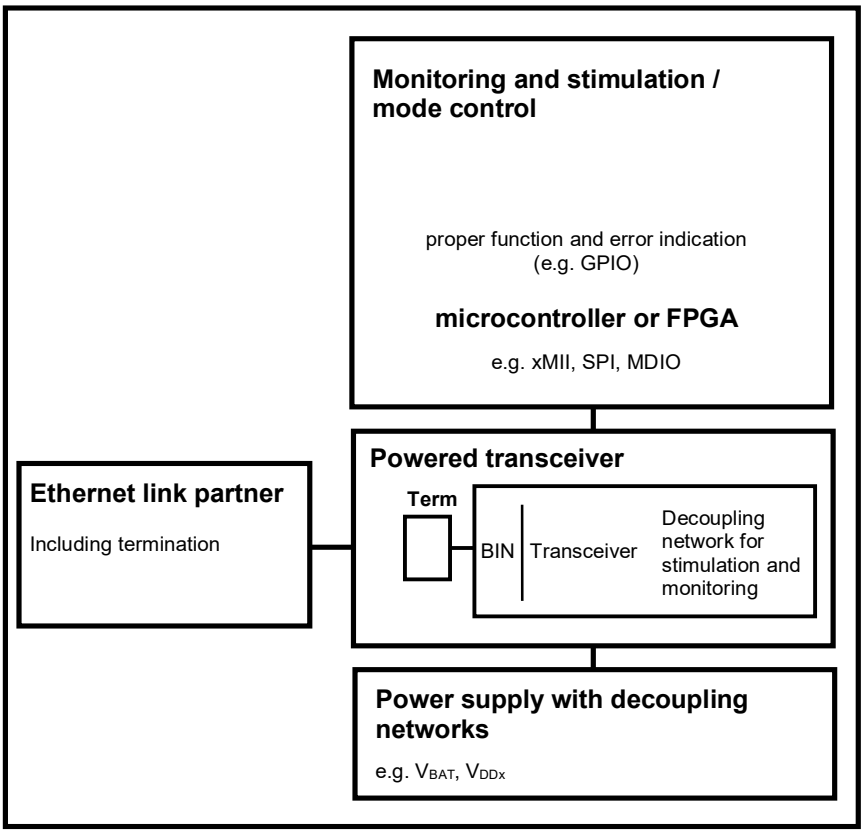


Figure D-1: General test configuration for radiated tests of the transceiver network

NOTE In specific cases or for analyses a deviation from this setup can be agreed between the users of this document and will be noted in the test report.

The BIN configurations are described in 5.3. The DUT node is configured according to data sheet definitions of the semiconductor manufacturer to establish a half duplex Ethernet link with the Ethernet link partner. The connection to the Ethernet link partner should have a length of 200 (± 20) mm and its characteristic should fulfill the definitions of the related Ethernet standard [4]. Multiple external link partner connections of an EAS with a higher number of MDI ports (e.g. 6 and more) could be limited because of test board constrains. In this case, the Ethernet test links can be realized between different MDI ports of the EAS itself but at least one ports should be connected to an external link partner.

All available interfaces of the Ethernet transceiver to the host microcontroller (e.g. xMII or SPI) should be tested separately as described in 5.4.1.

D.3 Tests

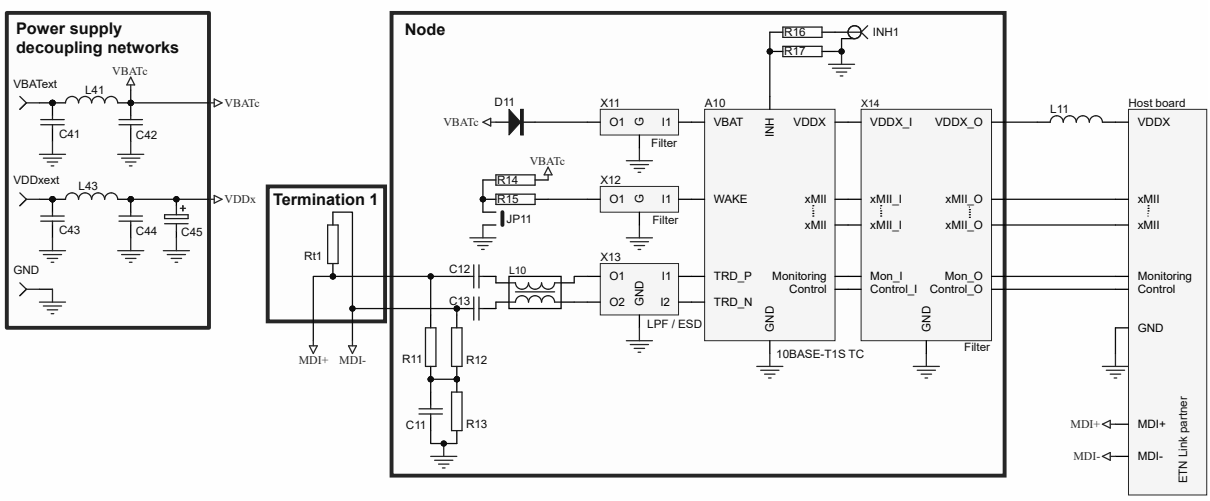
D.3.1 General

The Ethernet test circuits for radiated RF tests define the complete test circuitry details for testing Ethernet transceivers in functional operating modes under network condition. It defines mandatory, protection and filter components and optional components for Ethernet transceiver functions, decoupling networks, which are used for power supply, stimulation and monitoring of the DUT. A general drawing of the test circuit diagram of the Ethernet test network for radiated RF testing of 10BASE-T1S Ethernet transceivers in functional operating modes is given in Figure D-1.

A 10BASE-T1S node consists of transceiver (A10) with external mandatory components and protection and filter components (X11, X12, X13, X14) and the BIN (L11, C12, C13, R11, R12, R13) and the decoupling network at monitored pins (R16). All mandatory external components and protection and filter components (except components for MDI) should be used according to the specification of the Ethernet transceiver. If special components for MDI are defined in the specification, this circuitry should be tested in addition.

The resistor values at the WAKE pin should be set to the maximum specified value (default R = 3.3 kΩ) for R14 and to the minimum specified value (default R = 33 kΩ) for R15. For RF decoupling of monitored pins INH the default resistor value is set to R = 1 kΩ for all tests. In order to avoid a floating voltage at pin INH in sleep mode a pull down resistor (R17) should be used with values according to the IC specifications (default R = 10 kΩ).

For decoupling of external power supplies two-stage LC-filters (C41, L41, C42 and C43, L43, C44, C45) are used separately for V_{BAT} and V_{DDx}.



Key Components

A10	Ethernet transceiver 10BASE-T1S
C11	capacitor *C* = 100 nF (default value, placement depends on test case)
C12, C13	capacitor *C* = 100 nF
C41, C43	capacitor *C* = 1 nF
C42, C44	capacitor *C* = 330 pF
C45	capacitor *C* = 22 µF
D11	diode, general purpose rectifier type
JP11	Jumper
L10	Common mode choke that fulfills the requirements of [2] (placement depends on test case)
L11	inductor *L* = 4,7 µH (only populated for emission measurements at V_{DDx})
L41	inductor *L* = 47 µH
R11, R12	resistor *R* = 1.5 kΩ (± 1 %, default value, placement depends on test case)
R13	resistor *R* = 100 kΩ (default value, placement depends on test case)
R14	resistor *R* = 3.3 kΩ
R15	resistor *R* = 33 kΩ
R16	resistor *R* = 1 kΩ
R17	resistor *R* = 10 kΩ
X11, X12, X13, X14	Filter network or external circuitry defined by semiconductor manufacturer

Figure D-2: General circuit diagram of radiated RF test network for functional test of 10BASE-T1S Ethernet

For radiated tests of Ethernet transceivers the test network should be designed on a printed circuit board that is different to the test board for conducted RF and transient tests and follows the definitions of IEC 61967-1 [8] and IEC 62132-1 [12]. An example for radiated RF test board is given in Figure D-3 and Figure D-4.

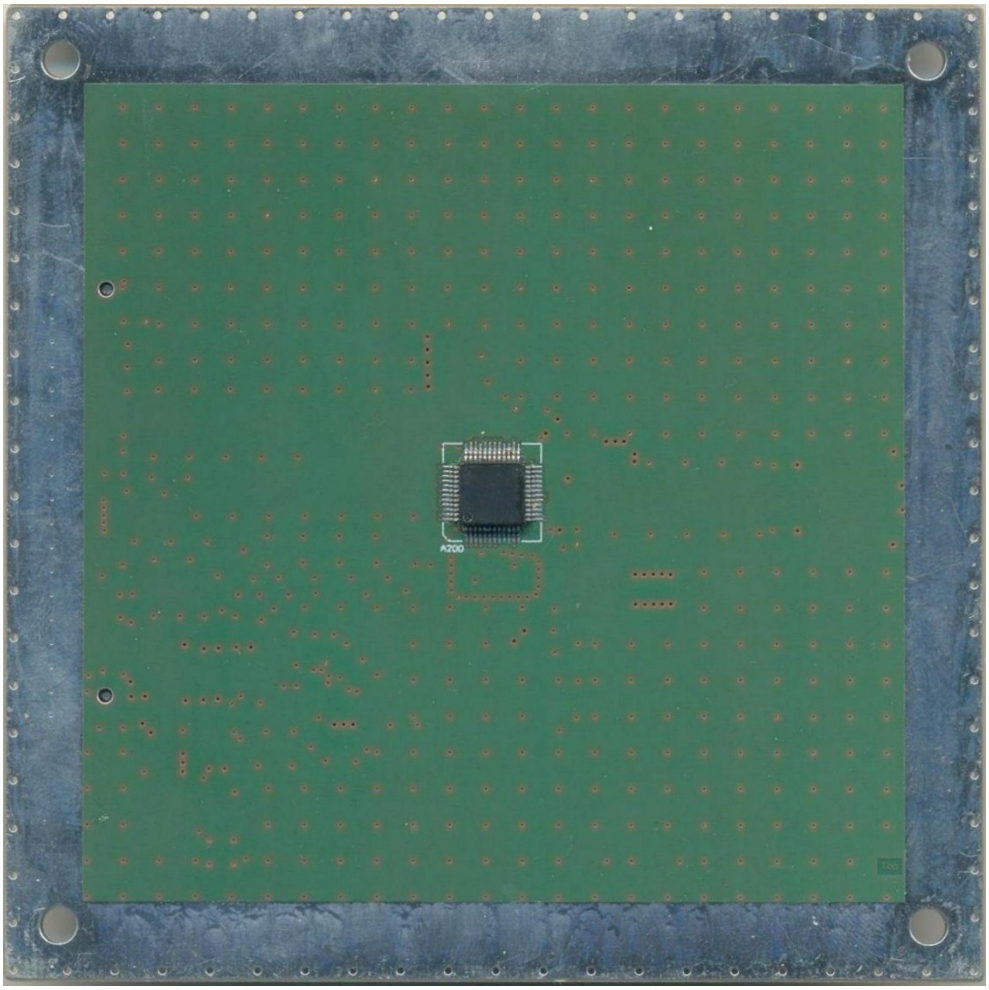


Figure D-3: Example of functional radiated test board for Ethernet transceiver ICs, top layer (DUT side)

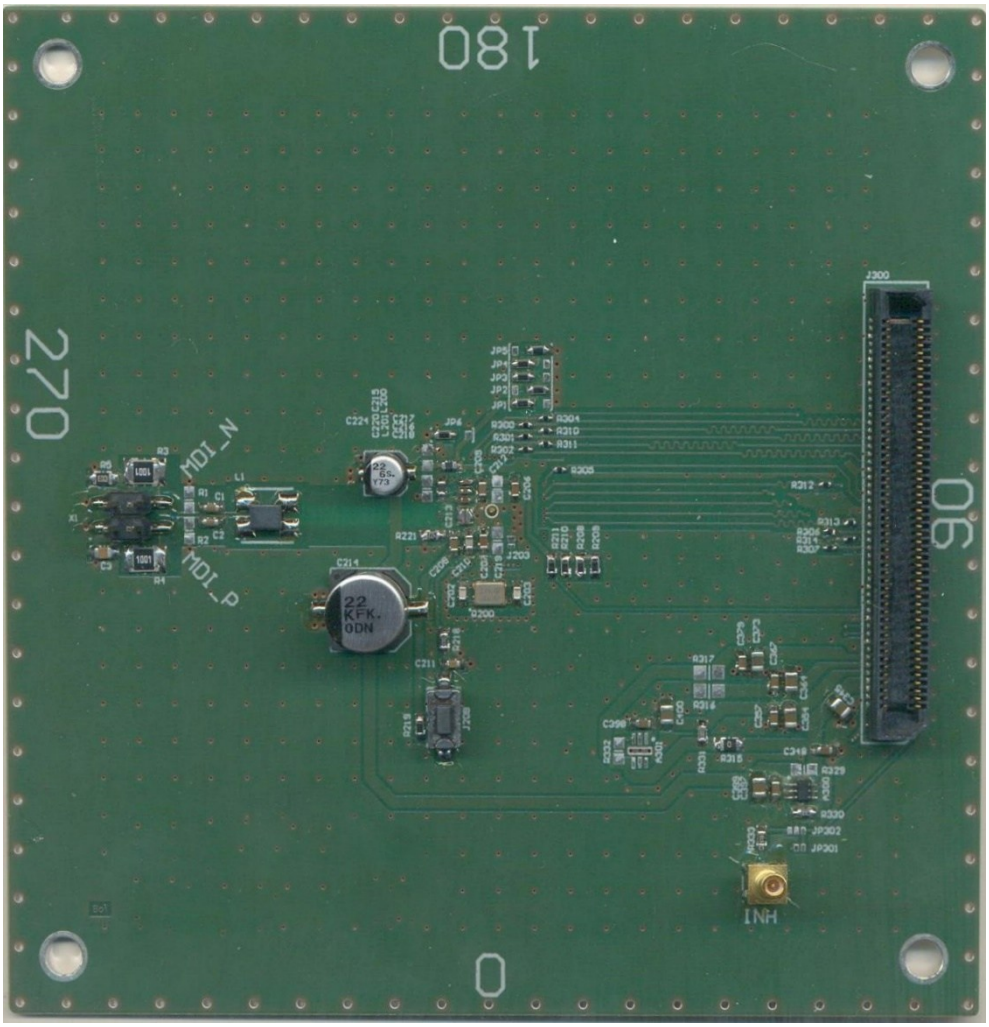


Figure D-4: Example of functional radiated test board for Ethernet transceiver ICs, bottom layer (external circuitry side)

D.3.2 Emission of radiated RF disturbances

The measurement of the radiated RF emission should be performed by IC stripline method according to IEC 61967-8 [11] or by GTEM cell method according to IEC 61967-2 [9].

The test setup for radiated RF emission measurement of transceiver is shown in Figure D-5.

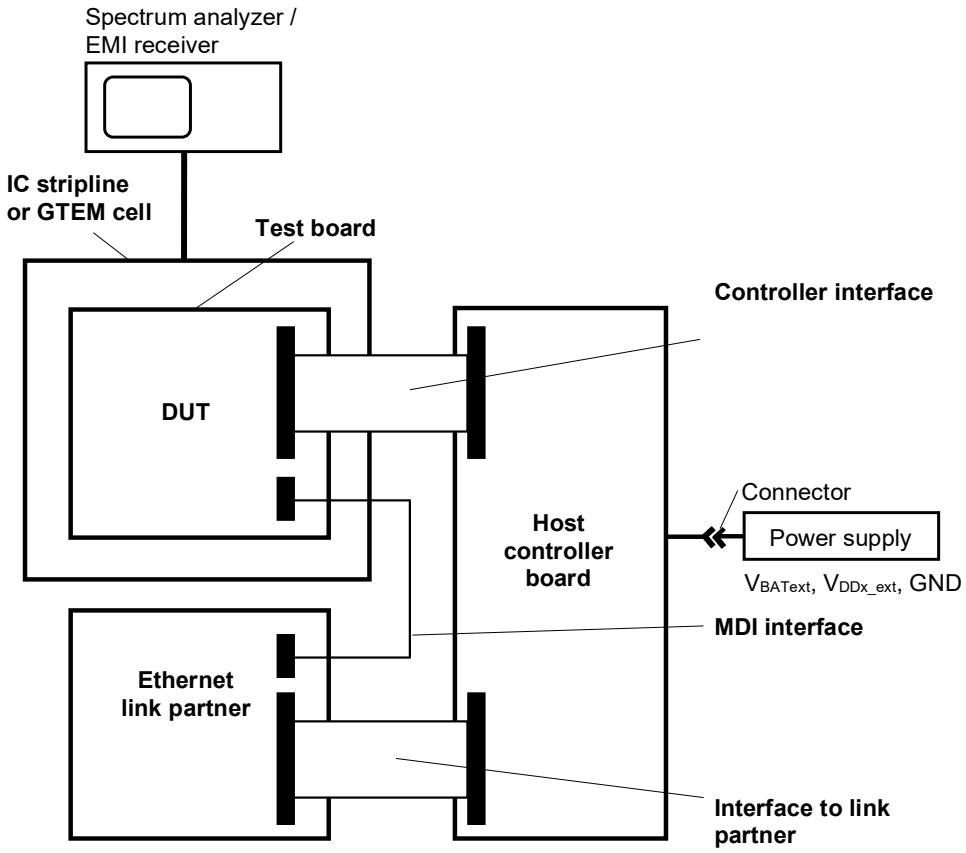


Figure D-5: Radiated RF emission test setup

The test equipment definitions are the following:

- spectrum analyzer / EMI receiver;
- IC stripline including 50 Ω RF termination resistor for output or GTEM cell;
- test board for radiated RF tests;
- host controller board;
- board with Ethernet link partner (test board as used for conducted RF emission, DPI and transient tests is proposed), and
- power supply.

The settings of the radiated RF measurement equipment are given in Table D-1.

RF Measurement equipment	Spectrum analyzer	EMI receiver
Detector	Peak	
Frequency range	0.15 MHz to 3000 MHz (6000 MHz optional)	
Resolution bandwidth (RBW)		
150 kHz to 30 MHz:	10 kHz	9 kHz
30 MHz to 6000 MHz:	100 kHz	120 kHz
Video bandwidth (VBW)	≥ 3 times RBW	–
Numbers of sweeps	10 (max hold)	–
Measurement time per step	–	≥ 100 ms
Frequency sweep time	≥ 100 s	–
Frequency step width		
150 kHz to 30 MHz:	–	≤ 5 kHz
30 MHz to 6000 MHz:	–	≤ 50 kHz
FFT based EMI receivers can be used as well if they meet CISPR 16-1-1 [19] definitions.		

Table D-1: Test equipment settings for radiated RF measurement

The radiated RF emission measurements should be performed according to Table D-2.

Transceiver mode	DUT orientation [a]	MDI test network (BIN)	Specific mode PLCA [c]
normal mode / with Ethernet test communication	0°, 90°	Opt-BIN [b]	X

X A test should be performed.
a DUT orientation within IC stripline or GTEM cell
b Opt-BIN is defined as default configuration. Other BINs can be tested as well.
c PLCA mode is only valid for PHY and MAC-PHY.

Table D-2: Radiated RF emission measurements

Recommended limits for evaluation using a 6.7 mm IC stripline according to IEC 61967-8 [11] are given in Figure D-6. The required limit class depend on the application conditions and will be defined by the customer.

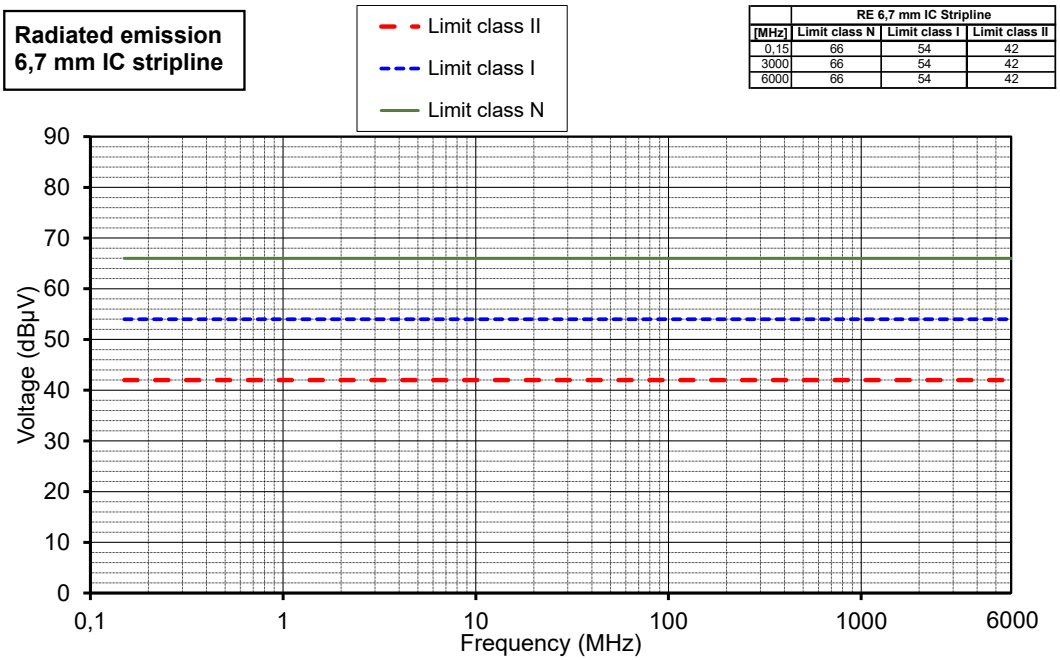


Figure D-6 Recommended limits for radiated RF emission for IC stripline with 6.7 mm active conductor height

A conversion factor (X) to correlate measuring results of IC striplines with different heights or GTEM cells to the default IC stripline height of 6.7 mm (IEC 61967-8 [11]) can be calculated by:

$$X = 20 \times \log \frac{h_1}{h_2}$$

where

X = conversion factor (in dB) to IC stripline 6.7 mm height type results;
h_1 = active conductor height (in mm) of IC stripline type or GTEM cell;
h_2 = active conductor height of 6.7 mm type.

D.3.3 Immunity to radiated RF disturbances

Radiated RF immunity tests should be performed by IC Stripline method according to IEC 62132-8 [15] or by GTEM cell method according to IEC 62132-2 [13]. The test setup for radiated RF immunity tests of transceiver is shown in Figure D-7.

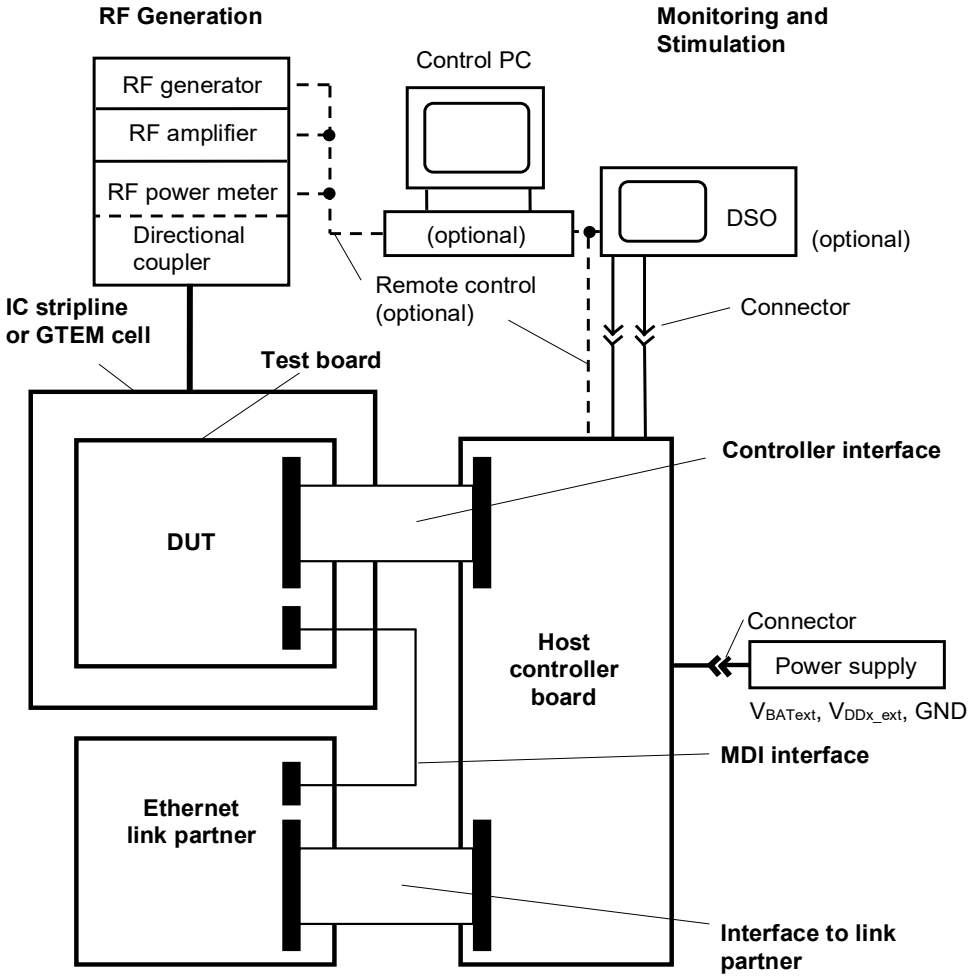


Figure D-7: Test setup for radiated RF immunity tests

The test equipment definitions are the following:

- RF generator, RF amplifier, power meter with directional coupler;
- IC Stripline including 50 Ω RF termination resistor for output or GTEM cell;
- test board for radiated RF tests;
- host controller board;
- board with Ethernet link partner (test board as used for conducted RF emission, DPI and transient tests is proposed);
- power supply, control PC (optional), digital storage oscilloscope (DSO, optional).

To determine the radiated RF immunity of the Ethernet transceiver, tests with the parameters given in Table D-3 should be carried out.

Item	Parameter	
Frequency	Range	Step
	1 MHz to 10 MHz	0.25 MHz
	10 MHz to 100 MHz	1 MHz
	100 MHz to 200 MHz	2 MHz
	200 MHz to 400 MHz	4 MHz
	400 MHz to 3000 MHz	10 MHz
	3000 MHz to 6000 MHz (optional)	20 MHz
Minimum test field strength	50 V/m	
Maximum field strength	800 V/m	
Field strength step size	50 V/m	
Dwell time	1 s	
Modulation (including optional frequency ranges)	*f* = 1 MHz to 6 000 MHz: CW *f* = 1 MHz to 380 MHz: AM 80 % 1 kHz ($\hat{P}_{PM} = \hat{P}_{CW}$) *f* = 380 MHz to 2 700 MHz: PM 1 kHz, ton 500 µs ($\hat{P}_{PM} = \hat{P}_{CW}$) *f* = 2 700 MHz to 3 100 MHz: PM 300 Hz, ton 3 µs ($\hat{P}_{PM} = \hat{P}_{CW}$) *f* = 3 100 MHz to 6 000 MHz: PM 1 kHz, ton 500 µs ($\hat{P}_{PM} = \hat{P}_{CW}$)	
Test procedure for evaluation of functional status class A_{IC}	Before each single test If shall be ensured that the transceiver is in proper function in relation to function status class A_{IC} for the related test case (e.g. no CRC or DTT error occur). Searching for malfunction in relation to function status classes $A2_{IC}$ during the complete dwell time while test field strength is stepwise increased. An optimized control procedure can be used to reduce the test time but ensuring that there are no artifacts in DUT response during frequency or test field strength steps. EXAMPLE: Procedure for each frequency step: • start with maximum test value or with the level that caused a malfunction at the previous frequency step, • in case of malfunction at this test level reduce the test value by 6dB and repeat the test, • increase the test value stepwise until a malfunction occurs or the maximum field strength is reached, • the immunity level at this frequency is the maximum field strength that causes no malfunction	

Table D-3: Radiated RF immunity tests specification

The tests for functional status class A_{IC} evaluation should be performed according to Table D-4. For each test an immunity threshold curve with the field strength as the parameter should be determined and documented in a diagram in the test report.

Transceiver mode	DUT orientation [a]	MDI test network (BIN)	Failure validation for error / function				
			CRC, DTT	SNR or SQI	Sum or RX, ED [b]	Other pin function	Wake-up
Ethernet system configuration			PLCA [d]				
normal mode / Ethernet test communi-cation	0°, 90°	Opt-BIN [c]			X	X	

X A test should be performed.

a DUT orientation within IC stripline or GTEM cell

b Sum error: CRC and DTT or BIST / PRBS tests status evaluated in parallel for PHY and MAC-PHY, RX and ED evaluation for PMD transceiver.

c Opt-BIN is defined as default configuration. Other BINs can be tested as well.

d PLCA mode is only valid for PHY and MAC-PHY.

Table D-4: Radiated RF immunity tests for functional status class AIC evaluation

Recommended limits for evaluation are given in Figure D-8. The required limit class depend on the application conditions and will be defined by the customer.

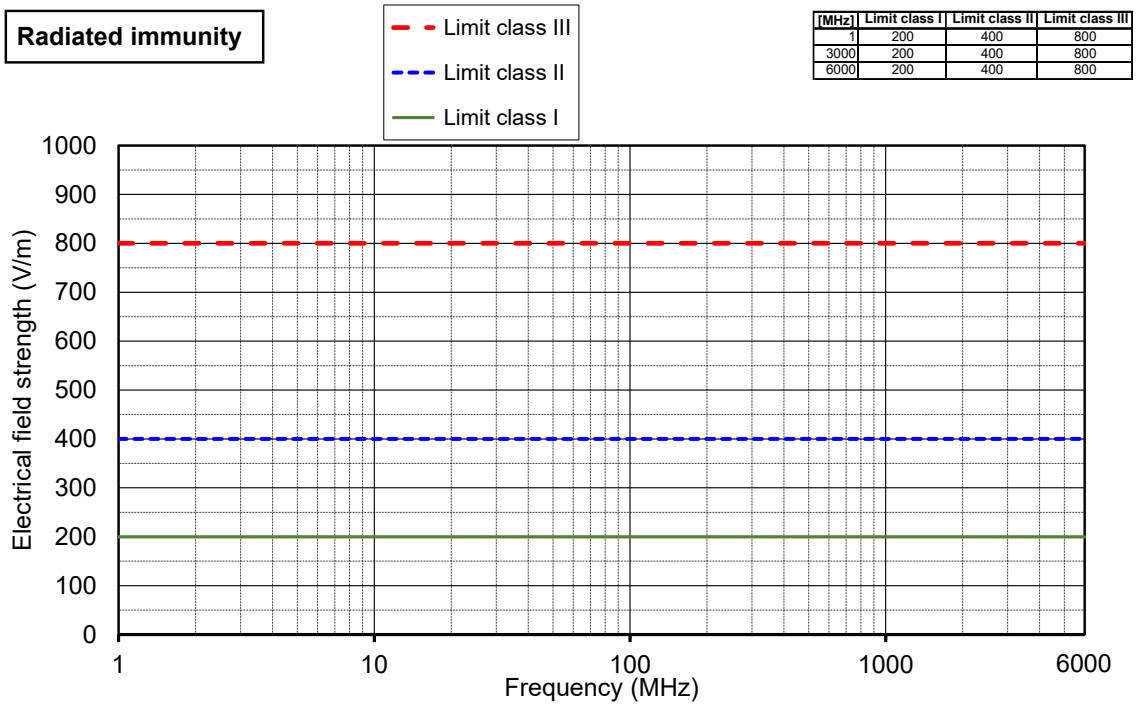


Figure D-8: Recommended limits for radiated RF immunity tests