nGBASE-AU Physical Layer System Requirements and Test Plan

Interoperability and System Test Plan for Multi-Gigabit Optical Automotive Ethernet

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INTRODUCTION

This document specifies three different test plans, each one focused on a different portion of the Automotive Optical Multigigabit Ethernet communication system.

- Clause 10 specifies the interoperability test plan for a complete Automotive Optical Multigigabit Ethernet communication system composed of at least one device and a link partner (LP), each of them implementing at least one nGBASE-AU type PHY transceiver as specified in [1]. The implementation of an nGBASE PHY transceiver is referred to as an nGBASE-AU entity.
- Clause 13 specifies the device-level conformance test plan for a device that implements at least one nGBASE-AU type transceiver, that is, at least one nGBASE-AU entity.
- Clause 14 specifies the physical layer (PHY) -level conformance test plan for an nGBASE-AU entity in a device.

The portion of the complete system which is under test is different for each of the three test plans, and in this document, they are referred to as Implementation Under Test (IUT), Device Under Test (DUT) and PHY Under Test (PUT), as shown in Figure 1.

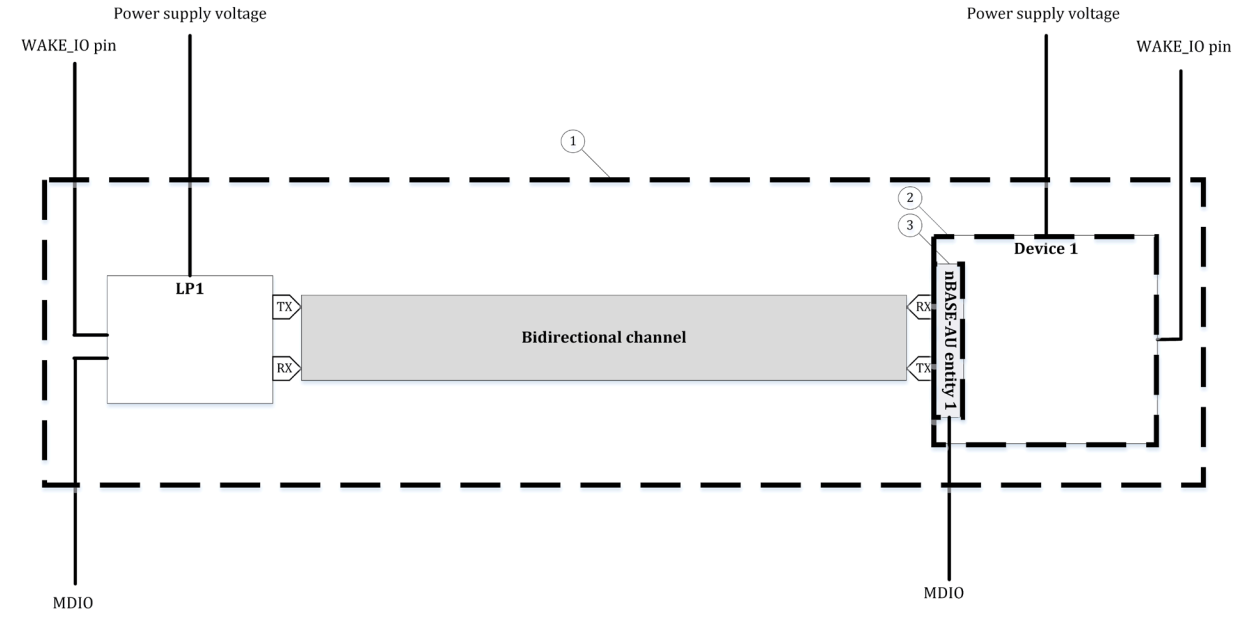


Figure 1 — The three different portions of the Automotive Optical Multigigabit Ethernet communication system under test defined in this document

This document also specifies general test requirements (see Clause 4) and system requirements, structured according to the functionality that they cover:

- nGBASE-AU link status and link up time, which comprises the physical layer system requirements related to the time and accuracy for the network system to signal a new status in the nGBASE-AU link, as well as the time for the network system to signal a reliable nGBASE-AU link status from a given initial power state of the two physical entities involved in the nGBASE-AU link (see Clause 5),
- channel quality, which comprises the physical layer system requirements related to the time and accuracy for the network system to signal a change in the channel quality of the nGBASE-AU link (see Clause 6),
- climatic load requirements, which comprises the physical layer system requirements related with the communication reliability when the devices in the network system are under certain climatic loads in a specific communication channel configuration (see Clause 7).

The interoperability test set-up requirements are specified in Clause 9. They include requirements on the channels that are used in the test set-ups and requirements on the device and LP used in the test set-ups. The objective of the interoperability test plan is to verify the physical layer system requirements with at least two devices and two nGBASE-AU entities. These test set-ups are relevant for the network system designer. The relevant portion of the system for this test plan is the complete Automotive Optical Multigigabit Ethernet communication system that includes at least two or more nGBASE-AU physical entities implemented at least in one device and its LP. This portion is called IUT for the interoperability test.

The device-level test set-up requirements are specified in Clause 11. They include the requirements for which a given link partner shall comply to be considered a qualified link partner. The objective of the device-level conformance test plan is to verify the device-level requirements. These test set-ups are relevant for the device provider. The relevant portion of the system for this test plan is the device that includes at least one nGBASE-AU physical entity. This device is called DUT for the device-level conformance test.

The objective of the PHY-level conformance test plan is to verify a relevant set of 802.3cz requirements, specified in the PICS section of [1]. These test set-ups are relevant for the transceiver and device provider.

The relevant portion of the system for this test plan is the implementation of the nGBASE-AU PHY specified in [1] that is referred to in this document as the nGBASE-AU physical entity. This entity is called PUT for the PHY compliance test.

The IUT (or DUT, or PUT) and the Upper Tester (UT) are controlled by the test controller (TC). The TC implements the functionality of the test coordination procedure specified in ISO 9646-1:1994.

The IUT (or DUT, or PUT) has communication with the UT. The UT can generate and analyze data from the unit under test and determine if the result complies with the desired requirements, as specified in ISO 9646-1:1994.

Figure 2 shows the relationship between the different components of the test environment.

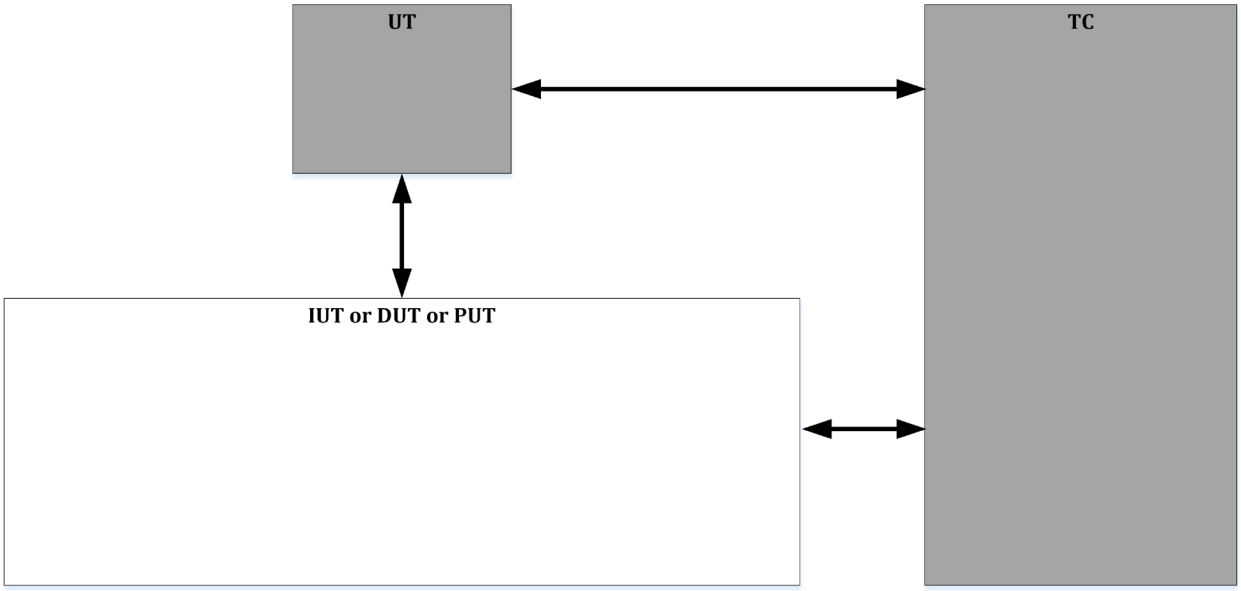


Figure 2 — Interoperability test environment

ABBREVIATION/SYMBOLS

DUT	Device Under Test
I/O	Input/Output
IUT	Implementation Under Test
LP	Link Partner
MAC	Media Access Control
MDI	Media Dependent Interface
MDIO	Management Data Input/Output
MII	Media Independent Interface
PCB	Printed Circuit Board
PCS	Physical Coding Sublayer
PHY	Physical Layer
PMA	Physical Medium Attachment
PUT	PHY Under Test
TC	Test Controller
UT	Upper Tester

*	May indicate either the arithmetical multiply operation or the logical AND function
+	May indicate either the arithmetical sum operation or the logical OR function

1 SCOPE

This document specifies:

- general requirements on the IUT (or DUT, or PUT), LP and the test procedure,
- requirements on the physical layer at the system level,
- requirements on the interoperability test set-ups,
- interoperability test plan that checks the requirements for the physical layer at the system level,
- requirements on the device-level physical layer conformance test set-ups,
- device-level physical layer conformance test plan that checks a set of requirements for the OSI physical layer that are relevant for device vendors, and
- PHY-level physical layer conformance test plan that checks a set of requirements specified in [1] that are relevant for transceivers and device vendors.

The interoperability test plan checks the physical layer system requirements specified in this document and in [1]. This test plan is structured in three different test groups, according to the type of system requirements covered:

- link status and link-up, which includes the test cases that check the status of the link by using the content of the available registers and its accuracy with the actual status of the link, as well as the test cases that check the time required for the DUT to reach a reliable link status from specific state
- channel quality, which includes test cases that check the quality of the optical channel by using the content of the available registers and its accuracy with the measured quality of the optical channel, and
- wake-up and sleep, which includes the test cases that check that the transmission and reception of the wake-up and sleep events.

The requirements covered by the device-level physical layer conformance test plan are specified in the ISO 21111 series and in [1]. This test plan is structured in five different test groups, according to the test set-up required:

- high-attenuation channel,
- low-attenuation channel,
- optical transmitter measurements,
- optical receiver measurements, and
- wake-up and synchronized link sleep.

2 TERMS AND DEFINITIONS

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- ISO Online browsing platform: available at https://www.iso.org/obp
- IEC Electropedia: available at http://www.electropedia.org/

3 NORMATIVE REFERENCES

The following documents are referred to in the text in such a way that some or all their content constitutes the requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

[1] IEEE 802.3cz Task Force, "IEEE Std 802.3cz™-2023, Amendment 7: Physical Layer Specifications and Management Parameters for Multi-Gigabit Glass Optical Fiber Automotive Ethernet," IEEE Standards Association, New York, 2023.

4 GENERAL REQUIREMENTS

This subclause specifies general requirements on wake-up and synchronized sleep optional features, and on the IUT and LP used in the test setups, in addition to general requirements on how to perform the test cases and generate test reports.

4.1 Wake-up and synchronised link sleep optional features

REQ	4.1.1 PHY — Wake-up and synchronised link sleep optional features
Wake-up and synchronised link sleep as specified in ISO 21111-2 are optional features. Physical entities implementing these optional features shall comply with the requirements given in Clause 8 of this document.	

4.2 IUT requirements

REQ	4.2.1 PHY — IUT requirements — nGBASE-AU entity definition and components
A nGBASE-AU entity shall be composed by a nGBASE-AU PHY implementation that fulfils the requirements specified in [1], and, optionally, the implementation of the wake-up and synchronized link sleep functionality as specified in ISO 21111-2	

REQ	4.2.2 PHY — IUT requirements — IUT definition and components
The IUT shall be composed by the following components: • one or more nGBASE-AU entities, • one optical connector per each nGBASE-AU entity, • the configuration of each nGBASE-AU entity, and • the PCB layout and other components needed for power supply.	

REQ	4.2.3 PHY — IUT requirements — PCB requirements
The PCB layout and components shall comply with the nGBASE-AU entity silicon provider reference design requirements, including those referred to power supply, power decoupling, and MAC interface.	

REQ	4.2.4 PHY — IUT requirements — nGBASE-AU entity configuration requirements
The configuration of the nGBASE-AU entities in the IUT shall comply with the nGBASE-AU entities silicon provider configuration requirements. This configuration shall be documented using a closed list of registers and its value.	

REQ	4.2.5 PHY — IUT requirements — MDIO interface
The IUT shall include at least one accessible MDIO interface as specified in ISO/IEC/IEEE 8802-3 that allows the individual access to each set of MDIO registers of each nGBASE-AU entity in the IUT.	

REQ	4.2.6 PHY — IUT requirements — Wakeup and Sleep functionality control
If the IUT or the LP implements the wake-up and synchronized link sleep functionality, it shall include a way to access and control PHY service interface and neighbour service interface, as specified in ISO 21111-2:2019.	

REQ	4.2.7 PHY — IUT requirements — Access to registers
The IUT shall provide access at least once each 1 ms to BASE-U PCS status 1 register (register 3.2349), as specified in IEEE 802.3cz. This register includes information about current link status, local receiver status, and remote receiver status, among others.	

4.3 Qualified Link Partner (LP) requirements

REQ	4.3.1 PHY — Qualified Link Partner (LP) requirements — Qualified LP definition and requirements
A qualified LP shall comply with the device-level requirements defined for an IUT specified in subclause 4.2 and covered by the test plan specified in Clause 12.	

REQ	4.3.2 PHY — Qualified Link Partner (LP) requirements — LP definition and requirements
A qualified LP shall comply with the interoperability requirements defined for an IUT specified in Clauses 5, 6, 7, and 8, and covered by the test plan specified in Clause 10	

REQ	4.3.3 PHY — Qualified Link Partner (LP) requirements — LP requirements for test plans
A previously Qualified Link Partner shall be used as LP when conducting test plans to qualify a DUT as a new Qualified Link Partner. When there are no previous Qualified Link Partner available, the same components and configuration as the DUT shall be used as LP for the test plans specified in Clause 10 and Clause 12.	

4.4 General test case and report requirements

REQ	4.4.1 PHY — General test case and report requirements — Test case pass definition
A test case shall be passed if and only if all test iterations which compose the test case are tested and the test result of each one is passed.	

REQ	4.4.2 PHY — General test case and report requirements — Test with all qualified LP
For the interoperability test cases specified in Clause 10, the IUT shall be tested against a closed list of qualified Link Partners (LPs).	

REQ	4.4.3 PHY — General test case and report requirements — Test report requirements for qualified LP
The test report of each interoperability test case shall include the test case result for each combination of IUT and qualified LP.	

REQ	4.4.4 PHY — General test case and report requirements — Test report requirements for traceability
The test report of each test case shall include documentation describing univocally, for the IUT and the LP when applicable, the following items: • the nGBASE entity implementation version and vendor, • the optical connector reference, • the configuration of the nGBASE entity, • the PCB layout version, and, if applicable, • the harness reference used for the test case.	

5 NGBASE-AU LINK STATUS REQUIREMENTS

Besides the requirements specified in this Clause, there are several basic assumptions that are made on the behavior of DUT signals:

- DUT dependability signals and registers are in accordance with the link state detected by the DUT at any time.
- The DUT can start sending Ethernet data frames as soon as the DUT signals that the link state is up.

Additionally, the link partner (LP) used in the definition of the requirements is assumed to be a qualified link partner as specified in 4.3, which complies with the requirements defined in IEEE 802.3cz.

5.1 Link Up Status: Time between link established status change and initial frame reception

REQ	5.1.1 PHY — Time between link established and reception of Ethernet frame
The time measured from the instant when the nGBASE-AU link status changes to "bidirectional reliable link is established" till the reception of the first Ethernet frame in the device shall be lower than 0.5 ms when Ethernet frames are sent continuously from the LP.	

5.2 Link Down Status: Time between link down and link status change

REQ	5.2.1 PHY — Time between link down and link status change
The time measured from the instant when the nGBASE-AU link becomes unreliable till the nGBASE-AU link status changes to "bidirectional unreliable link" shall be lower than 5 ms. NOTE: A link is considered unreliable when the received signal is below the sensitivity of the receiver.	

5.3 Link Status: Wake up and reset status change

REQ	5.3.1 PHY — PHY Link wake up status change
The time measured from the instant when the nGBASE-AU entity 1 receives a PHY_WakeUp.request from the data link layer as specified in ISO 21111-2 till the nGBASE-AU link status in nGBASE-AU entity changes to "bidirectional reliable link is established" shall be lower than 100 ms. The initial power state of the nGBASE-AU entity in device 1 shall be Sleep as defined in ISO 21111-2. The initial power state of the LP to measure this time shall be Sleep as defined in ISO 21111-2.	

REQ	5.3.2 PHY — Link wake up status change, configuration 1
The time measured from the instant when the nGBASE-AU entity 1 receives a WakeUp_request event as specified in ISO 21111-2 till the nGBASE-AU link status in nGBASE-AU entity changes to "bidirectional reliable link is established" shall be lower than 100 ms. The initial power state of the nGBASE-AU entity in device 1 shall be Sleep as defined in ISO 21111-2. The initial power state of the LP shall be Normal as defined in ISO 21111-2.	

REQ	5.3.3 PHY — Link wake up status change, configuration 2
The time measured from the instant when the nGBASE-AU entity 1 receives a WakeUp_request event as specified in ISO 21111-2 till the nGBASE-AU link status in nGBASE-AU entity changes to "bidirectional reliable link is established" shall be lower than 100 ms. The initial power state of the nGBASE-AU entity in device 1 shall be Normal as defined in ISO 21111-2. The initial power state of the LP shall be Normal as defined in ISO 21111-2.	

REQ	5.3.4 PHY —Link reset status change initiated from device 1
The time measured from the instant when the nGBASE-AU entity 1 is reset till the nGBASE-AU link status in nGBASE-AU entity changes to "bidirectional reliable link is established" shall be lower than 100 ms. The initial power state of the nGBASE-AU entity in device 1 shall be Normal as defined in ISO 21111-2. The initial power state of the LP shall be Normal as defined in ISO 21111-2.	

REQ	5.3.5 PHY — Link reset status change initiated from LP
The time measured from the instant when the LP is reset till the nGBASE-AU link status in nGBASE-AU entity changes to "bidirectional reliable link is established" shall be lower than 100 ms. The initial power state of the nGBASE-AU entity in device 1 shall be Normal as defined in ISO 21111-2. The initial power state of the LP shall be Normal as defined in ISO 21111-2.	

6 CHANNEL REQUIREMENTS

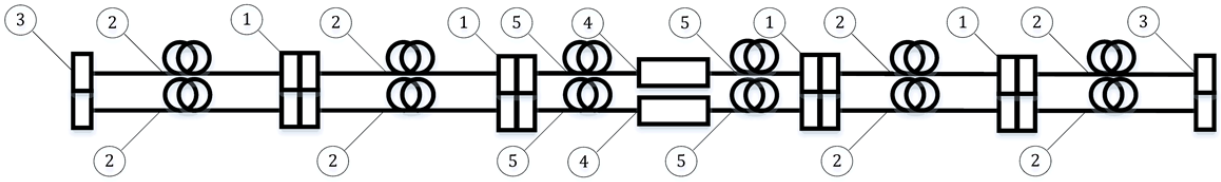
6.1 Channel quality indications

REQ	6.1.1 PHY - Channel quality decrease
The nGBASE-AU entity 1 shall indicate the channel quality decrease in terms of attenuation of at least 0.5 dB with decrease quality. This requirement applies for values of link margin lower than 10 dB.	

REQ	6.1.2 PHY – Channel quality increase
The nGBASE-AU entity 1 shall indicate the channel quality increase in terms of attenuation of at least 0.5 dB with increase quality. This requirement applies for values of link margin lower than 10 dB.	

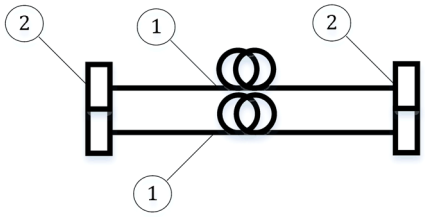
REQ	6.1.3 PHY – Channel quality optional test cases
If an nGBASE-AU entity supports a feature specified as “optional” in the standard, then the test cases associated with that feature are mandatory.	

The channel quality requirements measure the performance of a device over the specified channel to the LP with the channel link components as shown in Figure 3, Figure 4 or Figure 5. The requirements of the channel device and its LP are listed in the following subclauses.



Legend
1: In-line connector
2: 8-m of simplex OM3 cable
3: Cable plug
4: Mode-insensitive attenuator
5: 4-m of simplex OM3 cable

Figure 3 – Channel components for unidirectional high attenution link testing



Legend
1: 0,5-m of simplex OM3 cable
2: Cable plug

Figure 4 – Channel components for unidirectional low attenuation link testing

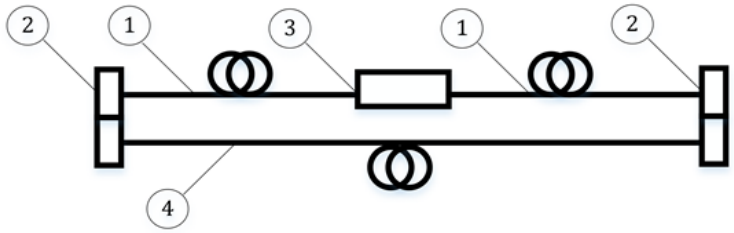


Figure 5 – Channel components for variable attenuation channel link testing

6.2 Channel types

REQ	6.2.1 PHY – Bidirectional high attenuation
The bidirectional high attenuation channel type shall be composed of two unidirectional high attenuation channels with construction specified in Figure 3. Each of the unidirectional high attenuation channels shall comply with requirement 6.2.2.	

REQ	6.2.2 PHY - Unidirectional high attenuation
The unidirectional high attenuation channel shall have an insertion loss measured at 0 Hz of 10.5 dB for 2.5GBASE-AU, 5BASE-AU or 10GBASE-AU, 8.5 dB for 25GBASE-AU, and 4.5 dB for 50GBASE-AU with a tolerance of 0.1 dB per IEEE 802.3cz Table 166-11. The maximum optical return loss tolerance shall be less than 12 dB in both high attenuation channel ends when a LP is connected at the other end per IEEE 802.3cz Table 166-9. The insertion loss and maximum optical return loss tolerance requirement shall be fulfilled at (23 ± 5)°C.	

REQ	6.2.3 PHY – Bidirectional low attenuation
The bidirectional low attenuation channel type shall be composed of two unidirectional low attenuation channels with construction specified in Figure 4. Each of the unidirectional low attenuation channels shall comply with requirement 6.2.4.	

REQ	6.2.4 PHY – Unidirectional low attenuation
The unidirectional low attenuation channel shall have a maximum insertion loss measured at 0 Hz of 2 dB. The maximum optical return loss tolerance shall be less than 12 dB in both low attenuation channel ends per IEEE 802.3cz Table 166-9. The maximum optical return loss tolerance shall be less than 12 dB in both low attenuation channel ends when a LP is connected at the other end per IEEE 802.3cz Table 166-9. The insertion loss and maximum optical return loss tolerance requirement shall be fulfilled at (23 ± 5)°C.	

REQ	6.2.5 PHY – Variable attenuation, configuration 1
The variable attenuation channel type shall be composed of one unidirectional variable attenuation channel that shall comply with requirement 6.2.6 and one unidirectional low attenuation channel that shall comply with requirement 6.2.4 with the construction specified in Figure 5. The unidirectional low attenuation channel shall connect the lower-left and lower-right ports of the variable attenuation channel. The unidirectional variable attenuation channel shall connect the upper-left and upper-right ports of the variable attenuation channel.	

REQ	6.2.6 PHY - Variable attenuation, configuration 2
The variable attenuation channel type shall have an insertion loss measured at 0 Hz programmable between 2 dB and 10.5 dB for 2.5GBASE-AU, 5BASE-AU or 10GBASE-AU, 8.5 dB for 25GBASE-AU, and 4.5 dB for 50GBASE-AU with a tolerance of 0.1 dB per IEEE 802.3cz Table 166-11. The maximum optical return loss tolerance shall be less than 12 dB in both variable attenuation channel ends when a LP is connected at the other end per IEEE 802.3cz Table 166-9. The insertion loss and maximum optical return loss tolerance requirement shall be fulfilled at (23 ± 5)°C.	

7 CLIMATIC LOAD REQUIREMENTS

7.1 Temperature and attenuation test conditions

REQ	7.1.1 PHY —Entity 1 at T_{max}, LP at T_{min}, high attenuation
The communication between nGBASE-AU entity 1 and its LP shall be reliable as specified in IEEE 802.3cz when: - the device that includes the nGBASE-AU entity 1 is located into an oven with temperature set to T_{max}, - the LP is located into an oven with temperature set to T_{min}, and - the communication channel between them is set as bidirectional high attenuation as specified in 6.2.1 and 6.2.2.	

REQ	7.1.2 PHY —Entity 1 at T_{min}, LP at T_{max}, high attenuation
The communication between nGBASE-AU entity 1 and its LP shall be reliable as specified in IEEE 802.3cz when: - the device that includes the nGBASE-AU entity 1 is located into an oven with temperature set to T_{min}, - the LP is located into an oven with temperature set to T_{max}, and - the communication channel between them is set as bidirectional high attenuation as specified in 6.2.1 and 6.2.2.	

REQ	7.1.3 PHY —Entity 1 at T_{min}, LP at T_{min}, high attenuation
The communication between nGBASE-AU entity 1 and its LP shall be reliable as specified in IEEE 802.3cz when: - the device that includes the nGBASE-AU entity 1 is located into an oven with temperature set to T_{min}, - the LP is located into an oven with temperature set to T_{min}, and - the communication channel between them is set as bidirectional high attenuation as specified in 6.2.1 and 6.2.2.	

REQ	7.1.4 PHY —Entity 1 at T_{max}, LP at T_{max}, high attenuation
The communication between nGBASE-AU entity 1 and its LP shall be reliable as specified in IEEE 802.3cz when: - the device that includes the nGBASE-AU entity 1 is located into an oven with temperature set to T_{max}, - the LP is located into an oven with temperature set to T_{max}, and - the communication channel between them is set as bidirectional high attenuation as specified in 6.2.1 and 6.2.2.	

REQ	7.1.5 PHY —Entity 1 at T_{max}, LP at T_{min}, low attenuation
The communication between nGBASE-AU entity 1 and its LP shall be reliable as specified in IEEE 802.3cz when: - the device that includes the nGBASE-AU entity 1 is located into an oven with temperature set to T_{max}, - the LP is located into an oven with temperature set to T_{min}, and	

- the communication channel between them is set as bidirectional low attenuation as specified in 6.2.3 and 6.2.4.

REQ	7.1.6 PHY —Entity 1 at T_{min}, LP at T_{max}, low attenuation
The communication between nGBASE-AU entity 1 and its LP shall be reliable as specified in IEEE 802.3cz when: - the device that includes the nGBASE-AU entity 1 is located into an oven with temperature set to T_{min}, - the LP is located into an oven with temperature set to T_{max}, and - the communication channel between them is set as bidirectional low attenuation as specified in 6.2.3 and 6.2.4.	

REQ	7.1.7 PHY —Entity 1 at T_{min}, LP at T_{min}, low attenuation
The communication between nGBASE-AU entity 1 and its LP shall be reliable as specified in IEEE 802.3cz when: - the device that includes the nGBASE-AU entity 1 is located into an oven with temperature set to T_{min}, - the LP is located into an oven with temperature set to T_{min}, and - the communication channel between them is set as bidirectional low attenuation as specified in 6.2.3 and 6.2.4.	

REQ	7.1.8 PHY —Entity 1 at T_{max}, LP at T_{max}, low attenuation
The communication between nGBASE-AU entity 1 and its LP shall be reliable as specified in IEEE 802.3cz when: - the device that includes the nGBASE-AU entity 1 is located into an oven with temperature set to T_{max}, - the LP is located into an oven with temperature set to T_{max}, and - the communication channel between them is set as bidirectional low attenuation as specified in 6.2.3 and 6.2.4.	

8 WAKE-UP AND SLEEP REQUIREMENTS

8.1 Sleep mode initiation

REQ	8.1.1 PHY —Sleep request initiated from Entity 1
The DUT shall be able to enter the sleep mode as specified in ISO 21111-2 and remain in this state after link-up is established when the sleep request is issued on the DUT side.	

REQ	8.1.2 PHY —Sleep request initiated from LP
The DUT shall be able to enter the sleep mode as specified in ISO 21111-2 and remain in this state after link-up is established when the sleep request is issued on the LP side.	

8.2 Power state control and detection

The power state diagram for Entity 1 is shown in Figure 6. This state diagram specifies the transitions between the power states of the physical entity.

REQ	8.2.1 PHY —Entity 1 power-off MDI signal detection
When the physical entity power supply is in power-off mode, it shall still provide sufficient current to enable the detection of a signal in the MDI (see 8.3.19).	

REQ	8.2.2 PHY —Entity 1 control of power_off_entity
The physical entity can control the power_off_entity variable.	

REQ	8.2.3 PHY —Entity 1 power state value validation
The physical entity shall be in one of the two following power states: - sleep, or - normal The power state of the physical entity is defined by the value of pd_status variable.	

REQ	8.2.4 PHY — Entity 1 Sleep power state validation
When the physical entity is in the sleep power state, it shall have its pd_status variable set to TRUE.	

REQ	8.2.5 PHY —Entity 1 Normal power state validation
When the physical entity is in the normal power state, it shall have its pd_status variable set to FALSE.	

REQ	8.2.6 PHY —Entity 1 Sleep power state MDI signal detect validation
When the physical entity is in the sleep power state, it shall still be able to detect a wake signal at the MDI.	

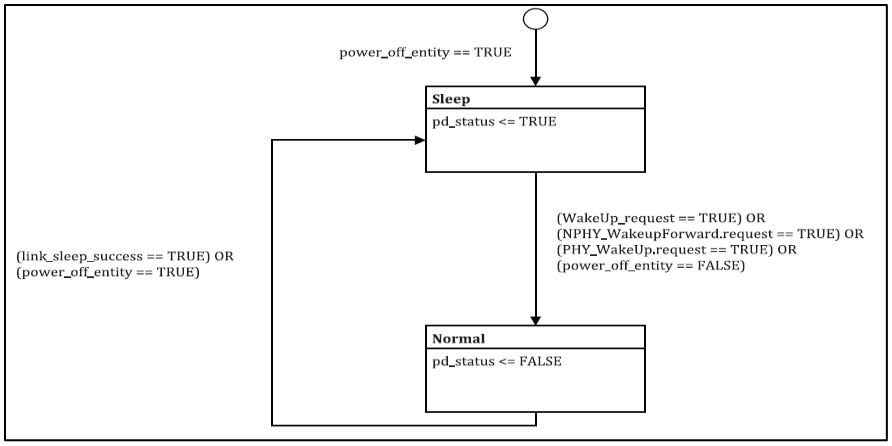


Figure 6 – Physical Entity Power State Diagram

REQ	8.2.7 PHY —Entity 1 refusal of sleep power state change request (Optional)
A configuration to refuse the request from the called physical entity to go to the sleep power state may be provided (see 8.3.19).	

REQ	8.2.8 PHY — Power supply configuration
All physical entities in a device shall share the same power supply.	

8.3 Link Sleep and Wake

REQ	8.3.1 PHY — Synchronized sleep implemented
The physical entity shall support the synchronised link sleep algorithm. A successful synchronised link sleep exchange of events follows this sequence: 1) the calling physical entity shall receive a PHY_LinkSleep.request service primitive from the MAC layer; 2) the calling physical entity shall generate a LinkSleep_request event that is transmitted to its link partner; 3) whenever a LinkSleep_request event is received, and the link partner is configured to *not* reject this request, the called physical entity shall respond to the calling physical entity with a LinkSleep_acknowledge event; 4) the link partner may generate the optional PHY_LinkSleepRequestEvent.indication service primitive and may allow its MAC layer to abort the sleep procedure. In case that the link partner MAC layer aborts the sleep procedure, the link partner shall not generate the LinkSleep_acknowledge event [see 3) above]; 5) when the LinkSleep_acknowledge event is received by the calling physical entity, and further media dependent optional conditions are fulfilled, the calling physical entity shall set its internal variable link_sleep_success to TRUE and may generate the PHY_LinkSleep.indication service primitive with the link_sleep_success parameter set to TRUE.	

REQ	8.3.2 PHY — Synchronized sleep request rejected (Optional)
The physical entity may optionally reject a synchronized sleep request according to the sequence below. A rejected synchronised link sleep exchange of events follows this sequence:	

1) the calling physical entity shall receive a PHY_LinkSleep.request service primitive from the MAC layer; 2) the calling physical entity shall generate a LinkSleep_request event that is transmitted to its link partner; 3) if the link partner is configured to reject the LinkSleep_request event or the MAC layer of the link partner aborts the LinkSleep_request, the link partner shall respond to the calling physical entity with a LinkSleep_reject event, when the LinkSleep_request event is received; 4) in the case that the link partner implements the optional PHY_LinkSleepRequestEvent.indication service primitive, it shall be generated and sent to MAC layer of the link partner; 5) when the LinkSleep_reject event is received by the calling physical entity, the calling physical entity shall set its internal variable link_sleep_success to FALSE and shall generate the PHY_LinkSleep.indication service primitive with the link_sleep_success parameter set to FALSE.

REQ	8.3.3 PHY — Link sleep acknowledge timeout
A timeout of the LinkSleep_acknowledge event shall be also interpreted as a valid LinkSleep_reject event.	

REQ	8.3.4 PHY — Link sleep to normal indication set
When a transition from the sleep power state to the normal power state is made, the physical entity shall generate the service primitive NPHY_WakeUpForward.indication with its parameter set to TRUE.	

REQ	8.3.5 PHY — Wake up request to link partner
The physical entity shall generate and send to its link partner a WakeUp_request, except if it received the WakeUP_request from this link partner.	

REQ	8.3.6 PHY — Wake up indication set
When a WakeUp_request event is received from the link partner on an active link, the physical entity shall generate the service primitive NPHY_WakeUpForward.indication with its parameter set to TRUE.	

REQ	8.3.7 PHY — Normal to sleep indication set
When a transition from the normal power state to the sleep power state is made, the physical entity shall generate the service primitive NPHY_WakeUpForward.indication with its parameter set to FALSE.	

REQ	8.3.8 PHY — Wake IO signal generation
When the incoming service primitive NPHY_WakeUpForward.request has its parameter equal to TRUE, the electrical signal generated in the WAKE_IO (TX) shall change from a low-voltage level to a high-voltage level.	

REQ	8.3.9 PHY — Receiver wake signal indication set
The wake I/O functional entity shall convert an electrical signal consisting of a transition from low-voltage level followed by a high-voltage level with duration of more than 40 µs in the WAKE_IO (RX) interface into a service primitive NPHY_WakeUpForward.indication as specified in ISO 21111-2 with its parameter set to TRUE.	

REQ	8.3.10 PHY — Receiver wake signal indication not set
An electrical signal consisting of a transition from low-voltage level followed by a high-voltage level with duration below 10 µs incoming to the WAKE_IO (RX) shall not generate an NPHY_WakeUpForward.indication as specified in ISO 21111-2 with its parameter set to TRUE.	

REQ	8.3.11 PHY — Synchronized sleep timing
The synchronised link sleep algorithm as specified in ISO 21111-2 shall be completed within 50 ms.	

REQ	8.3.12 PHY — Wake sequence timing
The time to complete the wake-up algorithm as specified in ISO 21111-2 shall be less than 2 ms, in case the two physical entities involved in the algorithm are in the normal power state. This requirement is valid regardless of the status of the link on the MDI between the two physical entities.	

REQ	8.3.13 PHY — Wake up forwarding - active link timing
The wake-up forwarding time over an active link (link established) defined as TWU_Link_Active shall be less than 2 ms.	

REQ	8.3.14 PHY — Wake up forwarding - passive link timing
The wake-up forwarding time over a passive link (link down) defined as TWU_Link_Passive shall be less than 2 ms.	

REQ	8.3.15 PHY — Wake forwarding glue logic timing
The forwarding glue logic shall generate any NPHY_WakeUpForward.request from the reception of any NPHY_WakeUpForward.indication after a maximum specified time TWU_Forwarding. The time TWU_Forwarding shall be less than 1 ms.	

REQ	8.3.16 PHY — Wake power supply stabilization timing
The time t_Powersupply_Stable shall be less than 5 ms.	

REQ	8.3.17 PHY — Wake initialization timing
The time t_Initialization shall be less than 10 ms.	

REQ	8.3.18 PHY — Wake IO timing
The time TWU_WakeIO shall be less than 1 ms.	

REQ	8.3.19 PHY — Entity sleep state current consumption limit
The physical entity design target concerning current consumption in the sleep power state shall be less than 35 µA. This covers the signal detection circuitry (10 µA) and the control circuitry (25 µA). The control circuitry can be shared among several physical entities in a device.	

9 INTEROPERABILITY TEST PLAN SET-UPS

9.1 Interoperability test set-up 1

The interoperability test set-up 1 is composed of one device and its LP connected by one bidirectional channel that fulfils the requirements for the bidirectional high attenuation channel type specified in 6.2.

The device is placed inside a temperature chamber set to a controlled temperature T_{Device}.

The device is powered by a controlled power supply voltage U_{Device}.

The LP is placed inside a temperature chamber set to a controlled temperature T_{LP}.

The LP is powered by a controlled power supply voltage U_{LP}.

The device, LP1 and LP2 may include a wake I/O block connected to a WAKE_IO pin as specified in ISO 21111-2:2019, 6.6.

For the test cases that use this test set-up, to power up the device or LP means to set the power_off_entity variable specified in ISO 21111-2:2019 to FALSE for the nGBASE-AU entity included in the device or LP.

Symmetrically, to power down the device or LP means to set the power_off_entity variable specified in ISO 21111-2:2019 to TRUE for the nGBASE-AU entity included in the device or LP.

REQ	9.1.1 PHY — Interoperability test set-up 1
The interoperability test setup 1 shall include the elements and the placement specified in Figure 7	

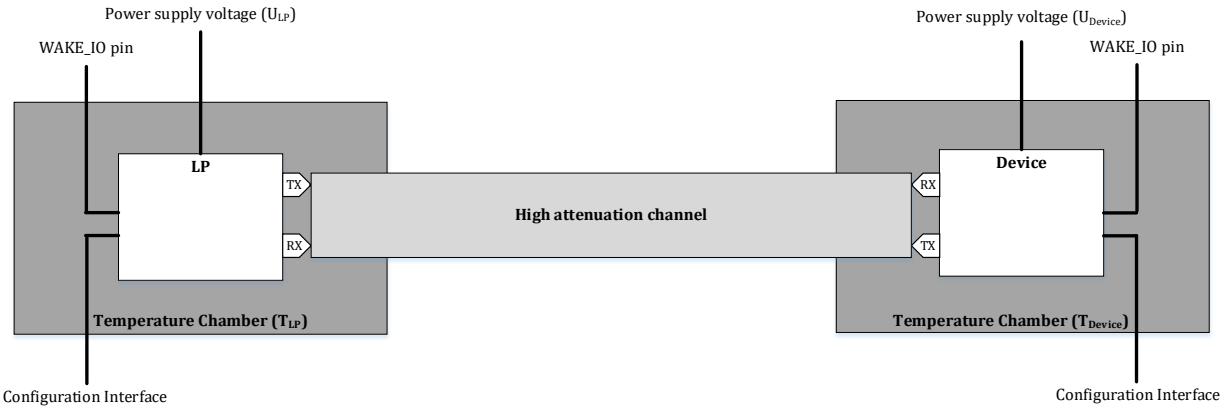


Figure 7 - High attenuation channel Interoperability test set-up 1

9.2 Interoperability test set-up 2

The interoperability test set-up 2 is composed of one device and its LP connected by one bidirectional channel that fulfils the requirements for the bidirectional variable attenuation channel type specified in 6.2.5 and 6.2.6.

The device is placed inside a temperature chamber set to a controlled temperature T_{Device}.

The device is powered by a controlled power supply voltage U_{Device}.

The LP is placed inside a temperature chamber set to a controlled temperature T_{LP}.

The LP is powered by a controlled power supply voltage U_{LP}.

The device, LP1 and LP2 may include a wake I/O block connected to a WAKE_IO pin as specified in ISO 21111-2:2019, subclause 6.6.

For the test cases that use this test set-up, to power up the device or LP means to set the power_off_entity variable specified in ISO 21111-2:2019 to FALSE for the nGBASE-AU entity included in the device or LP.

Symmetrically, to power down the device or LP means to set the power_off_entity variable specified in ISO 21111-2:2019 to TRUE for the nGBASE-AU entity included in the device or LP.

REQ	9.2.1 PHY — Interoperability test set-up 2
The interoperability test setup 1 shall include the elements and the placement specified in Figure 8.	

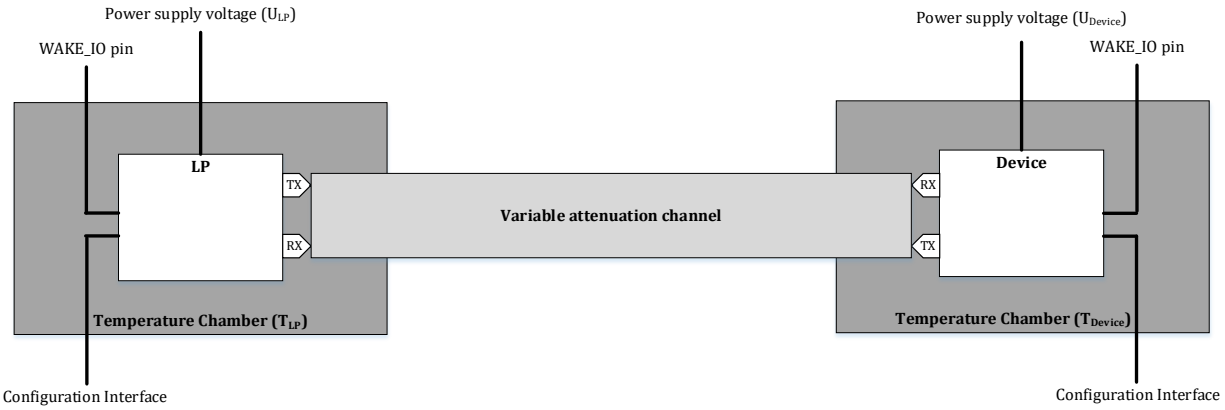


Figure 8 - Variable attenuation channel interoperability test setup 2

9.3 Interoperability test set-up 3

The interoperability test set-up 3 is composed of two link entities within a device and two LPs, each connected by one bidirectional channel that fulfils the requirements for the low attenuation channel type specified in 6.2.

The two link entities with a device are placed inside a temperature chamber set to a controlled temperature T_{Device}.

The device is powered by a controlled power supply voltage U_{Device}.

The LPs are not required to be placed inside a temperature chamber.

The LPs are each powered by a controlled power supply voltage, U_{LP1} and U_{LP2}.

The devices, LP1 and LP2 may include a wake I/O block connected to a WAKE_IO pin as specified in ISO 21111-2:2019, 6.6. A common WAKE_IO is implemented through a logic bridge to both link entities within the device.

For test cases that use this test set-up, to power up the device or a LP means to set the power_off_entity variable specified in ISO 21111-2:2019 to FALSE for the nGBASE-AU entity included in the device or LP.

Symmetrically, to power down the device or a LP means to set the power_off_entity variable specified in ISO 21111-2:2019 to TRUE for the nGBASE-AU entity included in the device or LP.

REQ	9.3.1 PHY — Interoperability test set-up 3
The interoperability test setup 3 shall include the elements and the placement specified in Figure 9.	

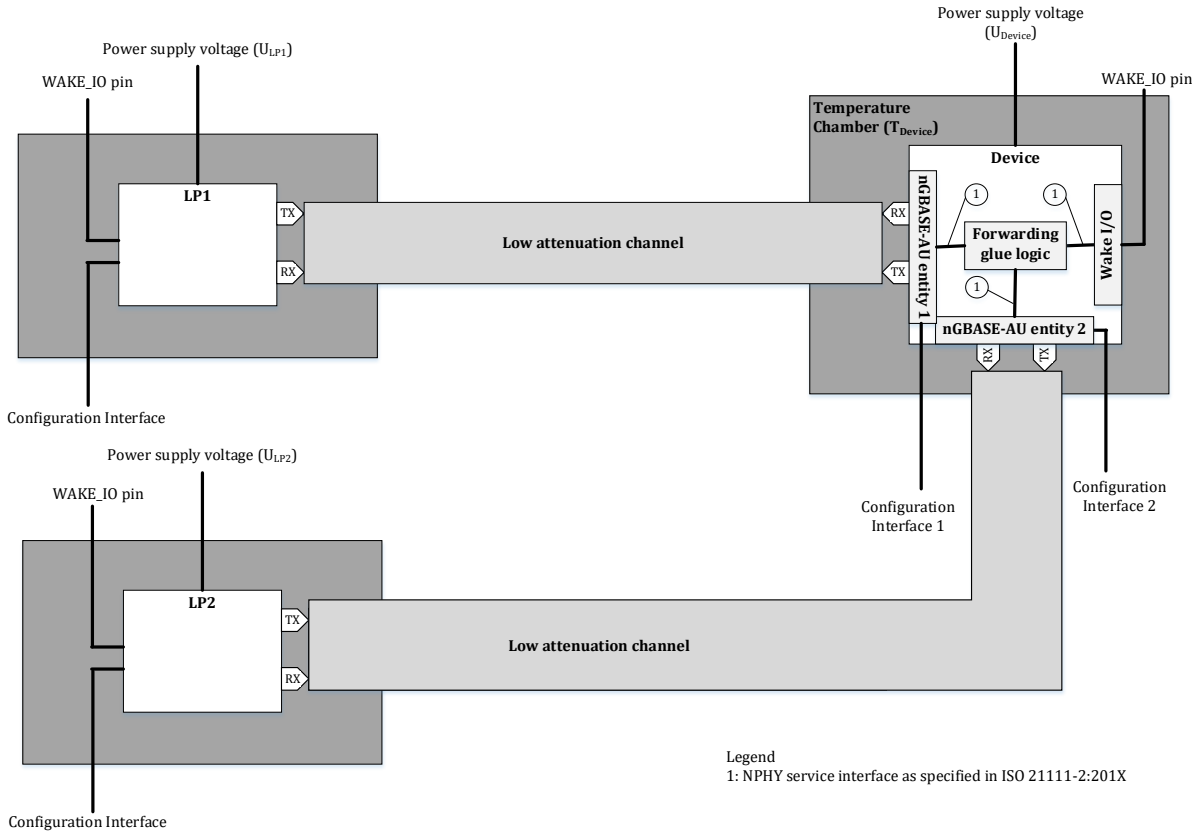


Figure 9 - Low attenuation channel interoperability test setup 3

10 INTEROPERABILITY TEST PLAN

10.1 General

The interoperability test plan is a set of test cases that checks system network requirements and needs a test set-up with at least one nGBASE-AU entity and its LP. This test plan is relevant for system network designers.

This test plan is structured in test groups. The test cases in the same test group share the same test set-up. The first three groups of tests are intended to ensure that the DUT is able to establish an active link before the required time under different temperature, voltage and channel environments.

Some of the test cases refer to different values of the climatic chamber temperature T and different values of the voltage U that is supplied to the device and to the LP.

REQ	10.1.**1 PHY — General — Temperature and voltage values**
The typical, minimum, and maximum values T_{typ}, T_{min}, T_{max}, U_{typ}, U_{min}, and U_{max} shall be provided by the test person.	

10.2 High attenuation channel with climatic load

Table 1 specifies the interoperability test case ITC_01_link-up_1_device_sleep for the high attenuation channel specified in subclause 13.2.

Table 1 — ITC_01_link-up_1_device_sleep — High attenuation channel with climatic load

Item	Content
Number – Title	**ITC_01_link-up_1_device_sleep — Link-up time when device is in sleep power state under high attenuation channel**
Purpose	This test case determines the link-up time from reset when the device is in sleep power state in a controlled network system at typical temperature and power supply voltage. The test case verifies that the calculated link up time is lower than 100 ms.
Reference	REQ 5.3.1
Prerequisites	Device shall provide access to the interfaces specified in 4.2
Set-up	9.1 Interoperability test set-up 1.
Step	1. The TC shall set the device power supply voltage U_{Device} to U_{typ}. 2. The TC shall set the LP power supply voltage U_{LP} to U_{typ}. 3. The TC shall power up the LP. 4. The TC shall power up the device. 5. The TC shall wait 100 ms. 6. The UT shall write the device MDIO register bit 15 of the MDIO register 1.0 with 1_2. Then the TC shall reset to zero the T_LINKUP timer and start it. 7. The TC shall wait till the device MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 8. The UT shall get the device link status at least once each ms. 9. When the device link status is equal to "bidirectional reliable link is established", the TC shall stop the T_LINKUP timer. 10. The UT shall monitor whether the IUT link status remains active for at least 750 ms. 11. The TC shall check that the value in the T_LINKUP timer is lower than 100 ms, and that the link did no go down during the monitoring time.
Iterations	N/A
Expected response	Result of check in step 13 shall be OK.
Remarks	N/A

Table 2 specifies the interoperability test case ITC_02_link-up_2_LP_sleep for the high attenuation channel specified in subclause 13.2.

Table 2 — ITC_02_link-up_2_LP_sleep — High attenuation channel with climatic load

Item	Content
Number – Title	**ITC_02_link-up_2_LP_sleep — Link-up time when LP is in sleep power state under high attenuation channel**
Purpose	This test case determines the link-up time when the LP is in sleep power state in a controlled network system at typical temperature and power supply voltage. The test case verifies that the calculated link up time is lower than 100 ms.
Reference	REQ 5.3.1.
Prerequisites	Device shall provide access to the interfaces specified in 4.2.
Set-up	9.1 Interoperability test set-up 1.
Step	1. The TC shall set the device power supply voltage U_{Device} to U_{typ}. 2. The TC shall set the LP power supply voltage U_{LP} to U_{typ}. 3. The TC shall power up the LP. 4. The TC shall power up the device. 5. The TC shall wait 100 ms. 6. The UT shall write the device MDIO register bit 15 of the MDIO register 1.0 with 1. 7. The TC shall wait till the device MDIO register bit 15 of the MDIO register 1.0 is equal to 0. 8. The UT shall write the LP MDIO register bit 15 of the MDIO register 1.0 with 1. Then the TC shall reset to zero the T_LINKUP timer and start it. 9. The TC shall wait till the LP MDIO register bit 15 of the MDIO register 1.0 is equal to 0. 10. The UT shall get the device link status at least once each ms. 11. When device link status is equal to "bidirectional reliable link is established", the TC shall stop the T_LINKUP timer. 12. The UT shall monitor whether the IUT link status remains active for at least 750 ms. 13. The TC shall check that the value in the T_LINKUP timer is lower than 100 ms, and that the link did no go down during the monitoring time.
Iterations	N/A
Expected response	Result of check in step 13 shall be OK.
Remarks	N/A

Table 4 specifies the interoperability test case ITC_03_temp_1 for the high attenuation channel specified in subclause 13.2. The iterations for this test case are specified in Table 3.

Table 3 — Required test case conditions T_{Device} and T_{LP} for ITC_03_temp_1

Iteration	T_{Device}	T_{LP}
1	T_{max}	T_{min}
2	T_{min}	T_{max}
3	T_{min}	T_{min}
4	T_{max}	T_{max}

Table 4 — ITC_03_temp_1 — High attenuation channel with climatic load

Item	Content
Number – Title	**ITC_03_temp_1 — System reliability under high attenuation channel and different extreme temperature for device and LP**
Purpose	This test case determines the system reliability when the device and LP are connected by a high attenuation channel and the temperature in the device is in one extreme of the range of temperatures specified by the device vendor and the LP is in the opposite extreme of the range of temperatures specified by the LP vendor.
Reference	REQ 7.1.1, REQ 7.1.2, REQ 7.1.3, REQ 7.1.4.
Prerequisites	Device shall provide access to the interfaces specified in 4.2.
Set-up	9.1 Interoperability test set-up 1
Step	1. The TC shall set the device climatic chamber temperature T_{Device} to the corresponding value for the current iteration. Allow the chamber to stabilize at the target temperature before proceeding. 2. The TC shall set the device power supply voltage U_{Device} to U_{typ}. 3. The TC shall set the LP climatic chamber temperature T_{LP} to the corresponding value for the current iteration. 4. The TC shall set the LP power supply voltage U_{LP} to U_{typ}. 5. The TC shall power up the LP. 6. The TC shall power up the device. 7. The TC shall wait 100 ms. 8. The UT shall write the device MDIO register bit 15 to bit 13 of the MDIO register 3.2348 with 001_2. 9. The UT shall write the device MDIO register bit 15 of the MDIO register 1.0 with 1_2. 10. The TC shall wait till the device MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 11. The UT shall write the LP MDIO register bit 15 to bit 13 of the MDIO register 3.2348 with 001_2. 12. The UT shall write the LP MDIO register bit 15 of the MDIO register 1.0 with 1_2. 13. The TC shall wait till the LP MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 14. The UT shall read bit 15 to bit 0 from the device MDIO register 3.522. 15. The UT shall read bit 15 to bit 0 from the LP MDIO register 3.522. 16. The TC shall wait for 15 min. 17. The UT shall read bit 15 to bit 0 from the device MDIO register 3.522. The TC shall check that it is equal to 0000_{16}. 18. The UT shall read bit 15 to bit 0 from the LP MDIO register 3.522. The TC shall check that it is equal to 0000_{16}.

Item	Content
Number – Title	**ITC_03_temp_1 — System reliability under high attenuation channel and different extreme temperature for device and LP**
Iterations	Perform iteration with test case conditions T_{Device} and T_{LP} specified in Table 3.
Expected response	Result of check in steps 17 and 18 shall be OK for all iterations.
Remarks	N/A

10.3 Low attenuation channel with climatic load

Table 6 specifies the interoperability test case ITC_05_temp_3 for the low attenuation channel specified in subclause 13.3. The iterations for this test case are specified in Table 5.

Table 5 — Required test case conditions T_{Device} and T_{LP} for ITC_05_temp_3

Iteration	T_{Device}	T_{LP}
1	T_{max}	T_{min}
2	T_{min}	T_{max}
3	T_{min}	T_{min}
4	T_{max}	T_{max}

Table 6 — ITC_05_temp_3 — Low attenuation channel with climatic load

Item	Content
Number – Title	**ITC_05_temp_3 — System reliability under low attenuation channel and different extreme temperature for device and LP**
Purpose	This test case determines the system reliability when the device and LP are connected by a low attenuation channel and the temperature in the device is in one extreme of the range of temperatures specified by the device vendor and the LP is in the opposite extreme of the range of temperatures specified by the LP vendor.
Reference	REQ 7.1.5, REQ 7.1.6, REQ 7.1.7, REQ 7.1.8.
Prerequisites	Device shall provide access to the interfaces specified in 4.2.
Set-up	9.1 Interoperability test set-up 1
Step	1. The TC shall set the device climatic chamber temperature T_{Device} to the corresponding value for the current iteration. Allow the chamber to stabilize at the target temperature before proceeding. 2. The TC shall set the device power supply voltage U_{Device} to U_{typ}. 3. The TC shall set the LP climatic chamber temperature T_{LP} to the corresponding value for the current iteration. 4. The TC shall set the LP power supply voltage U_{LP} to U_{typ}. 5. The TC shall power up the LP. 6. The TC shall power up the device. 7. The TC shall wait 100 ms. 8. The UT shall write the device MDIO register bit 15 to bit 13 of the MDIO register 3.2348 with 001_2. 9. The UT shall write the device MDIO register bit 15 of the MDIO register 1.0 with 1_2. 10. The TC shall wait till the device MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 11. The UT shall write the LP MDIO register bit 15 to bit 13 of the MDIO register 3.2348 with 001_2. 12. The UT shall write the LP MDIO register bit 15 of the MDIO register 1.0 with 1_2. 13. The TC shall wait till the LP MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 14. The UT shall read bit 15 to bit 0 from the device MDIO register 3.522. 15. The UT shall read bit 15 to bit 0 from the LP MDIO register 3.522. 16. The TC shall wait for 15 min. 17. The UT shall read bit 15 to bit 0 from the device MDIO register 3.522. The TC shall check that it is equal to 0000_{16}. 18. The UT shall read bit 15 to bit 0 from the LP MDIO register 3.522. The TC shall check that it is equal to 0000_{16}.

Item	Content
Number – Title	**ITC_05_temp_3 — System reliability under low attenuation channel and different extreme temperature for device and LP**
Iterations	Perform iteration with test case conditions T_{Device} and T_{LP} specified in Table 5.
Expected response	Result of check in steps 17 and 18 shall be OK for all iterations.
Remarks	N/A

10.4 Link status time

Table 7 specifies the interoperability test case ITC_07_link_status_rx_Eth for the high attenuation channel specified in subclause 13.2.

Table 7 — ITC_07_link_status_rx_Eth — Link status time

Item	Content
Number – Title	**ITC_07_link_status_rx_Eth — Time from link status to first Ethernet frame reception under high attenuation channel**
Purpose	This test case determines the time from the link status changes to "bidirectional reliable link is established" to the reception of the first Ethernet frame.
Reference	REQ 5.1.1.
Prerequisites	Device shall provide access to the interfaces specified in 4.2.
Set-up	9.1 Interoperability test set-up 1
Step	1. The TC shall set the device climatic chamber temperature T_{Device} to T_{typ}. 2. The TC shall set the device power supply voltage U_{Device} to U_{typ}. 3. The TC shall set the LP climatic chamber temperature T_{LP} to T_{typ}. 4. The TC shall set the LP power supply voltage U_{LP} to U_{typ}. 5. The TC shall power up the LP. 6. The TC shall power up the device. 7. The TC shall wait 100 ms. 8. The UT shall set the IUT to transmit continuously valid Ethernet frames with 64 bytes length from LP to device. The inter frame gap is set to the minimum. 9. The UT shall write the device MDIO register bit 15 of the MDIO register 1.0 with 1_2. 10. The TC shall wait till the device MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 11. The UT shall write the LP MDIO register bit 15 of the MDIO register 1.0 with 1_2. 12. The TC shall wait till the LP MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 13. The TC shall wait till the device link status is equal to "bidirectional reliable link is established". 14. The TC shall check that the device receives correctly the Ethernet frames. 15. The UT shall write the device MDIO register bit 15 of the MDIO register 1.0 with 1_2. 16. The TC shall wait till the device MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 17. When the device link status is equal to "bidirectional reliable link is established", the TC shall start the T_LINKSTATUS timer. 18. When the device receives the first correct Ethernet frame, the TC shall stop the T_LINKSATUS timer. 19. The TC shall check that the value in the T_LINKSTATUS timer is lower than 0.5 ms.
Iterations	N/A

Item	Content
Number – Title	**ITC_07_link_status_rx_Eth — Time from link status to first Ethernet frame reception under high attenuation channel**
Expected response	Result of check in steps 14 and 19 shall be OK.
Remarks	N/A

Table 8 specifies the interoperability test case ITC_08_link_status_unreliable for the high attenuation channel specified in subclause 13.2.

Table 8 — ITC_08_link_status_unreliable — Link status time

Item	Content
Number – Title	**ITC_08_link_status_unreliable — Time from unreliable link to link status equal to "bidirectional link unreliable"**
Purpose	This test case determines the time from physically unreliable link to link status changes to "bidirectional link unreliable".
Reference	REQ 5.2.1
Prerequisites	Device shall provide access to the interfaces specified in 4.2.
Set-up	9.1 Interoperability test set-up 1
Step	1. The TC shall set the device climatic chamber temperature T_{Device} to T_{typ}. 2. The TC shall set the device power supply voltage U_{Device} to U_{typ}. 3. The TC shall set the LP climatic chamber temperature T_{LP} to T_{typ}. 4. The TC shall set the LP power supply voltage U_{LP} to U_{typ}. 5. The TC shall power up the LP. 6. The TC shall power up the device. 7. The TC shall wait 100 ms. 8. The UT shall write the device MDIO register bit 12 to bit 10 of the MDIO register 3.2348 with 001_2. 9. The UT shall write the device MDIO register bit 15 of the MDIO register 1.0 with 1_2. 10. The TC shall wait till the device MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 11. The UT shall write the LP MDIO register bit 12 to bit 10 of the MDIO register 3.2348 with 001_2. 12. The UT shall write the LP MDIO register bit 15 of the MDIO register 1.0 with 1_2.

Item	Content
Number – Title	**ITC_08_link_status_unreliable — Time from unreliable link to link status equal to "bidirectional link unreliable"**
	13. The TC shall wait till the LP MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 14. The TC shall wait till the device link status is equal to "bidirectional reliable link is established". 15. The TC shall disable the optical transmission in the LP. Then the TC shall reset to zero the T_LINKUP timer and start it. 16. The UT shall get the device link status at least once each ms. 17. When the device link status is equal to "bidirectional unreliable link", the TC shall stop the T_LINKUP timer. 18. The TC shall check that the value in the T_LINKUP timer is lower than 5 ms.
Iterations	N/A
Expected response	Result of check in step 18 shall be OK.
Remarks	N/A

10.5 Channel quality

Table 9 specifies the interoperability test case ITC_09_decrease_ch_quality for the variable attenuation channel specified in subclause 9.2.

Table 9 — ITC_09_decrease_ch_quality — Channel quality

Item	Content
Number – Title	**ITC_09_decrease_ch_quality — Decrease channel quality measurement**
Purpose	This test case determines that when the channel decreases its quality, the reported quality also decreases.
Reference	REQ 6.1.1
Prerequisites	Device shall provide access to the interfaces specified in 4.2.
Set-up	9.2 Interoperability test set-up 2
Step	1. The TC shall set the device power supply voltage U_{Device} to U_{typ}. 2. The TC shall set the LP power supply voltage U_{LP} to U_{typ}.

Item	Content
Number – Title	**ITC_09_decrease_ch_quality — Decrease channel quality measurement**
	3. The TC shall power up the LP. 4. The TC shall power up the device. 5. The TC shall set MINMARGIN to zero. 6. The TC shall set MAXMARGIN to zero. 7. The TC shall set channel attenuation to 3 dB. 8. The TC shall wait 100 ms. 9. The TC shall wait till the device link status is equal to "bidirectional reliable link is established". 10. The UT shall read bit 7 to bit 0 from the device MDIO register 3.520 and store it into LINKMARGIN variable. 11. If LINKMARGIN is lower than the current value of MINMARGIN, then the TC shall store LINKMARGIN into MINMARGIN. 12. If LINKMARGIN is greater than the current value of MAXMARGIN, then the TC shall store LINKMARGIN into MAXMARGIN. 13. The TC shall repeat steps 10 to 12 100 times. 14. The TC shall set MIDMARGIN to MAXMARGIN/2 + MINMARGIN/2. 15. The TC shall set MIDMARGIN_HIGH to MIDMARGIN. 16. The TC shall increase channel attenuation by 0.5 dB. 17. The TC shall repeat steps 10 to 14. 18. The TC shall set MIDMARGIN_LOW to MIDMARGIN. 19. The TC shall check that MIDMARGIN_HIGH – MIDMARGIN_LOW is equal to 0.5 dB within a margin error of 0.1 dB. 20. If link status is equal to "bidirectional reliable link is established", then the TC shall repeat steps 10 to 20.
Iterations	N/A
Expected response	Result of check in step 19 shall be OK.
Remarks	A graph with channel attenuation in the x axis and MIDMARGIN in the y axis after step 14 can be build.

Table 10 specifies the interoperability test case ITC_10_increase_ch_quality for the variable attenuation channel specified in 9.2.

Table 10 — ITC_10_increase_ch_quality — Channel quality

Item	Content
Number – Title	**ITC_10_increase_ch_quality — Increase channel quality measurement**
Purpose	This test case determines that when the channel increases its quality, the reported quality also increases.
Reference	REQ 6.1.2
Prerequisites	Device shall provide access to the interfaces specified in 4.2.
Set-up	9.2 Interoperability test set-up 2
Step	1. The TC shall set the device power supply voltage U_{Device} to U_{typ}. 2. The TC shall set the LP power supply voltage U_{LP} to U_{typ}. 3. The TC shall power up the LP. 4. The TC shall power up the device. 5. The TC shall set MINMARGIN to zero. 6. The TC shall set MAXMARGIN to zero. 7. The TC shall set channel attenuation to 10 dB. 8. The TC shall wait 100 ms. 9. If the device link status is not equal to "bidirectional reliable link is established", then the TC shall decrease the channel attenuation by 0.1 dB. 10. The UT shall read bit 7 to bit 0 from the device MDIO register 3.520 and store it into LINKMARGIN variable. 11. If LINKMARGIN is lower than the current value of MINMARGIN, then the TC shall store LINKMARGIN into MINMARGIN. 12. If LINKMARGIN is greater than the current value of MAXMARGIN, then the TC shall store LINKMARGIN into MAXMARGIN. 13. The TC shall repeat steps 10 to 12 100 times. 14. The TC shall set MIDMARGIN to MAXMARGIN/2 + MINMARGIN/2. 15. The TC shall set MIDMARGIN_LOW to MIDMARGIN. 16. Decrease channel attenuation in 0.5 dB. 17. The TC shall repeat steps 10 to 16. 18. The TC shall set MIDMARGIN_HIGH to MIDMARGIN. 19. The TC shall check that MIDMARGIN_HIGH – MIDMARGIN_LOW is equal to 0.5 dB within a margin error of 0.1 dB. 20. If channel attenuation is greater than 3 dB, then the TC shall repeat steps 16 to 20.
Iterations	N/A

Item	Content
Number – Title	**ITC_10_increase_ch_quality — Increase channel quality measurement**
Expected response	Result of check in step 19 shall be OK.
Remarks	A graph with channel attenuation in the x axis and MIDMARGIN in the y axis after step 14 can be build.

11 DEVICE-LEVEL PHYSICAL LAYER CONFORMANCE TEST SET-UPS REQUIREMENTS

11.1 General

This Clause specifies the requirements of the test set-ups that are used in the device-level physical layer conformance test plan.

Most of the test set-ups involve a communication channel between a nGBASE-AU qualified link partner and the IUT. The different types of communication channels specified in 6.2 are used for the test set-ups.

The requirements on the nGBASE-AU qualified link partner and IUT for the test set-ups are specified in 4.3.

12 DEVICE-LEVEL PHYSICAL LAYER CONFORMANCE TEST PLAN SET-UPS

12.1 General

The objective of the device-level physical layer conformance test plan is to verify a subset of requirements that are relevant for the device vendor.

The IUT for this test plan is a device that includes one or more nGBASE-AU physical entities.

Each test plan set-up in this subclause specifies the LT and service provider that are used.

The IUT, LT, service provider, and UT are controlled by the TC. The TC implements the functionality of the test coordination procedure specified in ISO 9646-1:1994.

The IUT has communication with the UT. The UT can generate and analyze data from the IUT and check if the result complies with the IUT requirements, as specified in ISO 9646-1:1994.

Figure 10 shows the relationship between the IUT, LT, service provider, UT, and the TC.

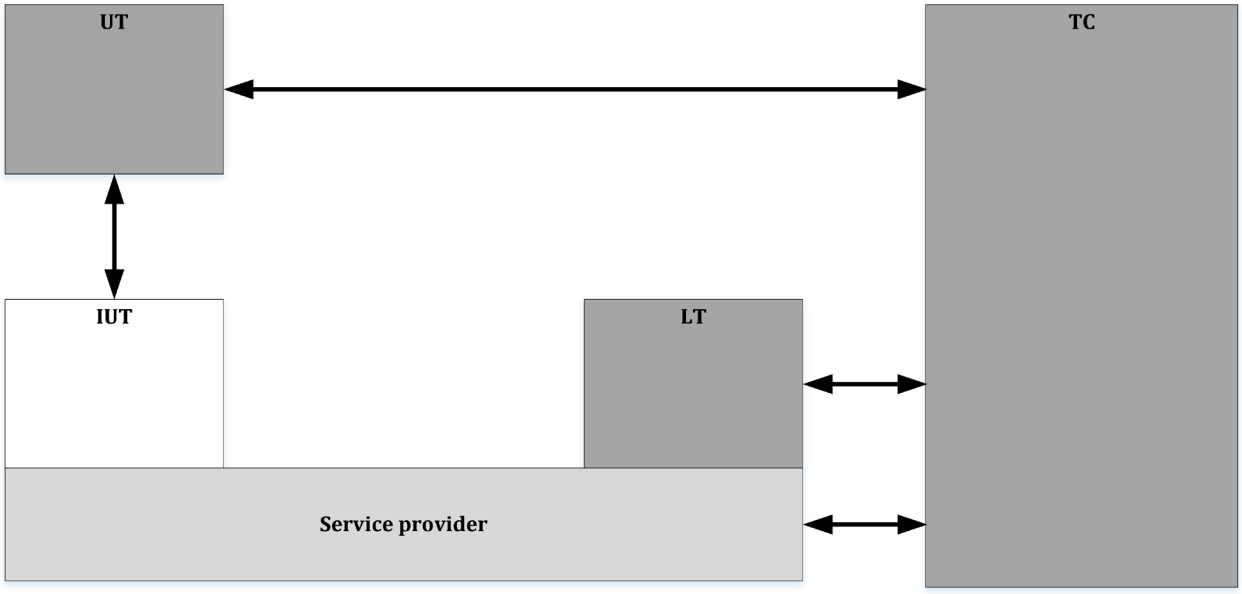


Figure 10 — Device-level physical layer conformance test environment

12.2 Device-level physical layer conformance test set-up 1

The device-level physical layer conformance test set-up 1 is composed of the IUT and one nGBASE-AU qualified link partner connected by a bidirectional channel that fulfils the requirements for the bidirectional high attenuation channel type specified in subclause 6.2.1.

The IUT is placed inside a temperature chamber set to a controlled temperature T.

The IUT is powered by a controlled power supply voltage U.

The IUT may include a wake I/O block connected to a WAKE_IO pin as specified in ISO 21111-2:2019, 6.6.

For the test cases that use this test set-up, to power up the IUT means to set the power_off_entity variable specified in ISO 21111-2:2019 to FALSE for the nGBASE-AU entity included in the IUT.

Symmetrically, to power down the IUT means to set the power_off_entity variable specified in ISO 21111-2:2019 to TRUE for the nGBASE_AU entity included in the IUT.

REQ	12.2.1 PHY — Device-level physical layer conformance test plan set-ups — Device-level physical layer conformance test set-up 1
The device-level physical layer conformance test setup 1 shall include the elements and the placement specified in Figure 11.	

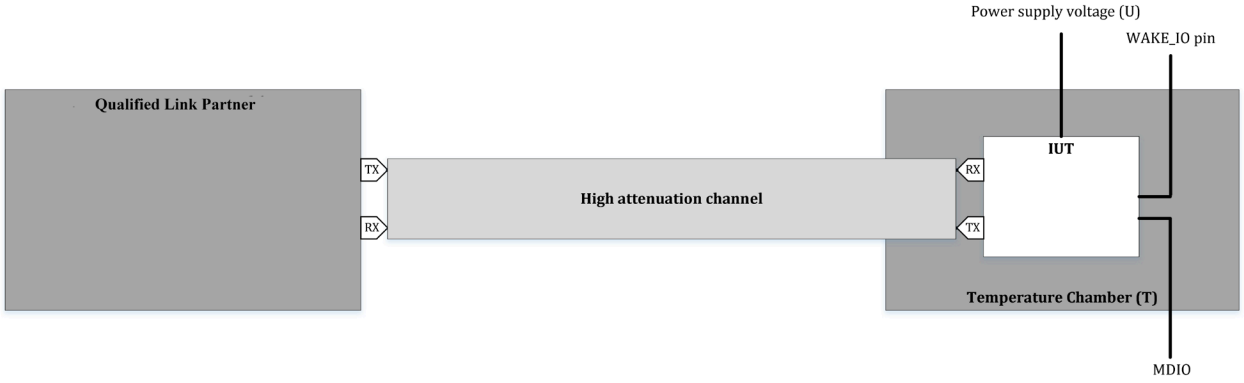


Figure 11 — Device-level physical layer conformance test set-up 1

12.3 Device-level physical layer conformance test set-up 2

The device-level physical layer conformance test set-up 2 is composed of the IUT and one nGBASE-AU qualified link partner connected by a bidirectional channel that fulfils the requirements for the bidirectional low attenuation channel type specified in subclause 6.2.3.

The IUT is placed inside a temperature chamber set to a controlled temperature T.

The IUT is powered by a controlled power supply voltage U.

The IUT may include a wake I/O block connected to a WAKE_IO pin as specified in ISO 21111-2:2019, 6.6.

For the test cases that use this test set-up, to power up the IUT means to set the power_off_entity variable specified in ISO 21111-2:2019 to FALSE for the nGBASE-AU entity included in the IUT.

Symmetrically, to power down the IUT means to set the power_off_entity variable specified in ISO 21111-2:2019 to TRUE for the nGBASE_AU entity included in the IUT.

REQ	12.3.1 PHY — Device-level physical layer conformance test plan set-ups — Device-level physical layer conformance test set-up 2
The device-level physical layer conformance test setup 1 shall include the elements and the placement specified in Figure 12.	

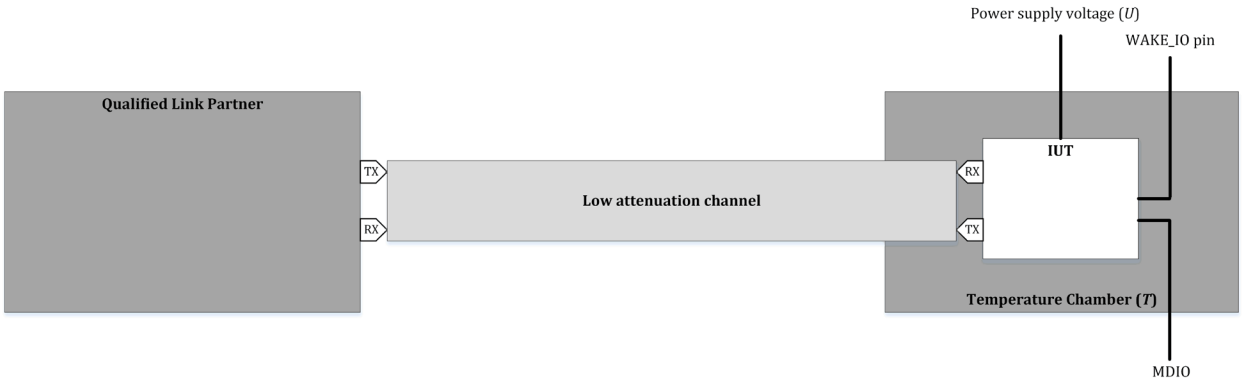


Figure 12 — Device-level physical layer conformance test set-up 2

13 DEVICE-LEVEL PHYSICAL LAYER CONFORMANCE TEST PLAN

13.1 General

The device-level physical layer conformance test plan is a set of test cases that check physical layer requirements that are relevant for device vendors.

This test plan is structured in test groups. The test cases in the same test group share the same test set-up.

First test group includes the test cases that use a high attenuation channel (see 13.2).

Second test group includes the test cases that use a low attenuation channel (see 13.3).

Third test group is the wake-up and synchronized link sleep test group (see 13.4), which is divided into two subgroups.

The first subgroup includes the test cases that shall be run for a device that implements the wake-up and synchronized link sleep functionality, regardless of the number of physical entities in the device (see 13.4.1).

The second subgroup includes the test cases that shall be run for a device that implements the wake-up and synchronized link sleep functionality and that includes more than one physical entity (see 13.4.2).

Some of the test cases are required to be repeated for different values of the climatic chamber temperature T and different values of the voltage U that is supplied to the IUT. Table 11 specifies the required test case conditions T, U for variable temperature and supply test cases.

REQ	13.1.1 PHY — Device-level physical layer conformance test plan — Temperature and voltage values
The typical, minimum and maximum values T_{typ}, T_{min}, T_{max}, U_{typ}, U_{min} and U_{max} shall be provided by the test person.	

Table 11 — Required test case conditions T, U for variable temperature and supply test cases.

Iteration	T	U
1	T_{typ}	U_{typ}
2	T_{min}	U_{min}
3	T_{min}	U_{max}
4	T_{max}	U_{max}
5	T_{max}	U_{min}

13.2 High attenuation channel

Table 12 specifies the device-level physical layer conformance test case DTC_01_system_reliability for the high attenuation channel specified in subclause 13.2.

Table 12 — DTC_01_system_reliability — High attenuation channel

Item	Content
Number – Title	**DTC_01_system_reliability — System reliability under high attenuation channel**
Purpose	This test case determines the communication reliability in a controlled network system at different temperatures and power supply voltages.
Reference	REQ 7.1.1, REQ 7.1.2, REQ 7.1.3, REQ 7.1.4.
Prerequisites	IUT shall provide access to the interfaces specified in 4.2.
Set-up	12.2 - Device-level physical layer conformance test set-up 1
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the qualified LP. 4. The TC shall power up the IUT. 5. The TC shall wait 100 ms. 6. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.2348 with 001_2. 7. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 8. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 9. The TC shall wait 100 ms. 10. The TC shall check that the IUT MDIO register bit 2 of the MDIO register 1.1 is equal to 1_2. 11. The TC shall set the qualified LP to transmit continuously Ethernet frames of length randomly chosen between 1 byte and 1518 byte. Ethernet inter-frame gap shall be at least 13 byte length. 12. The TC shall wait 15 min. 13. The TC shall check that the qualified LP Ethernet frame error counter is equal to zero. 14. The TC shall check that the bit error rate reported by the qualified LP is lower than 10^{-12}. 15. The TC shall check that the IUT MDIO register bit 2 of the MDIO register 1.1 is equal to 1_2.
Iterations	Perform iterations with test case conditions T and U as specified in Table 11.
Expected response	Result of checks in steps 10, 13, 14 and 15 shall be OK for all iterations.
Remarks	N/A

Table 13 specifies the device-level physical layer conformance test case DTC_02_link-up_LP_IUT_normal for the high attenuation channel specified in subclause 13.2.

Table 13 — DTC_02_link-up_LP_IUT_normal — High attenuation channel

Item	Content
Number – Title	**DTC_02_link-up_LP_IUT_normal — Link-up time when the LP and the IUT are in normal power state under high attenuation channel**
Purpose	This test case determines the link-up time when the LP and the IUT are in normal power state in a controlled network system at different temperatures and power supply voltages.
Reference	ISO 21111-3:2019 6.4, REQ 5.3.4, REQ 7.1.1, REQ 7.1.2, REQ 7.1.3, REQ 7.1.4.
Prerequisites	IUT shall provide access to the interfaces specified in 4.2.
Set-up	12.2 - Device-level physical layer conformance test set-up 1
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the qualified LP. 4. The TC shall disable qualified LP optical power transmission. 5. The TC shall power up the IUT. 6. The TC shall wait 100 ms. 7. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.2348 with 001_2. 8. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 9. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 10. The TC shall enable qualified LP optical power transmission. Then the TC shall reset to zero the T_LINKUP timer and start it. 11. The UT shall get the IUT link status at least once each ms. 12. When the IUT link status is equal to "bidirectional reliable link is established", the TC shall stop the T_LINKUP timer. 13. The UT shall monitor whether the IUT link status remains active for at least 750 ms. 14. The TC shall check that the value in the T_LINKUP timer is lower than 100 ms, and that the link did no go down during the monitoring time.
Iterations	Perform iterations with test case conditions T and U as specified in Table 11.

Item	Content
Number – Title	**DTC_02_link-up_LP_IUT_normal — Link-up time when the LP and the IUT are in normal power state under high attenuation channel**
Expected response	Result of check in step 14 shall be OK for all iterations.
Remarks	N/A

Table 14 specifies the device-level physical layer conformance test case DTC_03_link-up_IUT_sleep for the high attenuation channel specified in subclause 13.2.

Table 14 — DTC_03_link-up_IUT_sleep — High attenuation channel

Item	Content
Number – Title	**DTC_03_link-up_IUT_sleep — Link-up time when IUT is in sleep power state under high attenuation channel**
Purpose	This test case determines the link-up time when the IUT is in sleep power state in a controlled network system at different temperatures and power supply voltages. The procedure to wake-up the IUT is the reception of a WakeUp_request event.
Reference	ISO 21111-3:2019 6.4, REQ 5.3.2
Prerequisites	IUT shall provide access to the interfaces specified in 4.2.
Set-up	12.2 - Device-level physical layer conformance test set-up 1
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the qualified LP. 4. The TC shall disable qualified LP optical power transmission. 5. The TC shall power up the IUT. 6. The TC shall wait 100 ms. 7. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.2348 with 001_2. 8. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 9. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 10. The TC shall set IUT into sleep power state.

Item	Content
Number – Title	**DTC_03_link-up_IUT_sleep — Link-up time when IUT is in sleep power state under high attenuation channel**
	11. The TC shall enable qualified LP optical power transmission. Then the TC shall reset to zero the T_LINKUP timer and start it. 12. The UT shall get the IUT link status at least once each ms. 13. When the IUT link status is equal to "bidirectional reliable link is established", the TC shall stop the T_LINKUP timer. 14. The UT shall monitor whether the IUT link status remains active for at least 750 ms. 15. The TC shall check that the value in the T_LINKUP timer is lower than 100 ms, and that the link did no go down during the monitoring time.
Iterations	Perform iterations with test case conditions T and U as specified in Table 11.
Expected response	Result of check in step 15 shall be OK for all iterations.
Remarks	N/A

Table 15 specifies the device-level physical layer conformance test case DTC_04_link-up_LP_IUT_sleep for the high attenuation channel specified in subclause 13.2.

Table 15 — DTC_04_link-up_LP_IUT_sleep — High attenuation channel

Item	Content
Number – Title	**DTC_04_link-up_LP_IUT_sleep — Link-up time when the LP and the IUT are in sleep power state under high attenuation channel**
Purpose	This test case determines the link-up time when the LP and the IUT are in sleep power state in a controlled network system at different temperatures and power supply voltages. The LP wake-up is performed by a PHY_WakeUp_request.
Reference	ISO 21111-3:2019 6.4, REQ 5.3.1.
Prerequisites	IUT shall provide access to the interfaces specified in 4.2.
Set-up	12.2 - Device-level physical layer conformance test set-up 1
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration.

Item	Content
Number – Title	**DTC_04_link-up_LP_IUT_sleep — Link-up time when the LP and the IUT are in sleep power state under high attenuation channel**
	2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the qualified LP. 4. The TC shall power up the IUT. 5. The TC shall wait 100 ms. 6. The TC shall set IUT and qualified LP into sleep power state. 7. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.2348 with 001_2. 8. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 9. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 10. The TC shall set the qualified LP to generate the PHY_WakeUp.request. Then the TC shall reset to zero the T_LINKUP timer and start it. 11. The UT shall get the IUT link status at least once each ms. 12. When the IUT link status is equal to "bidirectional reliable link is established", the TC shall stop the T_LINKUP timer. 13. The UT shall monitor whether the IUT link status remains active for at least 750 ms. 14. The TC shall check that the value in the T_LINKUP timer is lower than 100 ms, and that the link did no go down during the monitoring time.
Iterations	Perform iterations with test case conditions T and U as specified in Table 11.
Expected response	Result of check in step 14 shall be OK for all iterations.
Remarks	N/A

Table 16 specifies the device-level physical layer conformance test case DTC_05_consumption_operation for the high attenuation channel specified in subclause 13.2.

Table 16 — DTC_05_consumption_operation — High attenuation channel

Item	Content
Number – Title	**DTC_05_consumption_operation — IUT power consumption in operation under high attenuation channel**
Purpose	This test case determines the IUT power consumption in operation in a controlled network system at different temperatures and power supply voltages.

Item	Content
Number – Title	**DTC_05_consumption_operation — IUT power consumption in operation under high attenuation channel**
Reference	REQ 8.3.19
Prerequisites	IDD_{min} and IDD_{max} shall be provided by the test person. IUT shall provide access to the interfaces specified in 4.2.
Set-up	12.2 - Device-level physical layer conformance test set-up 1
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. Allow the chamber to stabilize at the target temperature before proceeding. 2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the qualified LP. 4. The TC shall power up the IUT. 5. The TC shall wait 100 ms. 6. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.2348 with 001_2. 7. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 8. The TC shall wait util the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 9. The TC shall wait 100 ms. 10. The TC shall check that the IUT MDIO register bit 2 of the MDIO register 1.1 is equal to 1_2. 11. The TC shall set the qualified LP to transmit continuously Ethernet frames of length randomly chosen between 1 byte and 1518 byte. Ethernet inter-frame gap shall be at least 13 byte length. 12. The TC shall wait 15 min. 13. The TC shall measure IDD_{Device}. 14. The TC shall check that IDD_{Device} is higher than IDD_{min} and lower than IDD_{max}.
Iterations	Perform iterations with test case conditions T and U as specified in Table 11.
Expected response	Result of checks in steps 10 and 14 shall be OK for all iterations.
Remarks	N/A

Table 17 specifies the device-level physical layer conformance test case DTC_06_consumption_sleep for the high attenuation channel specified in subclause 13.2.

Table 17 — DTC_06_consumption_sleep — High attenuation channel

Item	Content
Number – Title	**DTC_06_consumption_sleep — IUT power consumption in sleep power state under high attenuation channel**
Purpose	This test case determines the IUT power consumption in sleep power state in a controlled network system at different temperatures and power supply voltages.
Reference	REQ 8.3.19
Prerequisites	IDD_DIS_{min} and IDD_DIS_{max} shall be provided by the test person. IUT shall provide access to the interfaces specified in 4.2.
Set-up	12.2 - Device-level physical layer conformance test set-up 1
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. Allow the chamber to stabilize at the target temperature before proceeding. 2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the qualified LP. 4. The TC shall power up the IUT. 5. The TC shall wait 100 ms. 6. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.2348 with 001_2. 7. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 8. The TC shall wait util the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 9. The TC shall wait 100 ms. 10. The TC shall check that the IUT MDIO register bit 2 of the MDIO register 1.1 is equal to 1_2. 11. The TC shall set the LP inside the qualified LP to sleep power mode. 12. The TC shall set the IUT to sleep power mode. 13. The TC shall measure IDD_{Device}. 14. The TC shall check that IDD_{Device} is higher than IDD_DIS_{min} and lower than IDD_DIS_{max}.
Iterations	Perform iterations with test case conditions T and U as specified in Table 11.

Item	Content
Number – Title	**DTC_06_consumption_sleep — IUT power consumption in sleep power state under high attenuation channel**
Expected response	Result of checks in steps 10 and 14 shall be OK for all iterations.
Remarks	N/A

13.3 Low attenuation channel

Table 18 specifies the device-level physical layer conformance test case DTC_07_system_reliability for the low attenuation channel specified in subclause 13.3.

Table 18 — DTC_07_system_reliability — Low attenuation channel

Item	Content
Number – Title	**DTC_07_system_reliability — System reliability under low attenuation channel**
Purpose	This test case determines the communication reliability in a controlled network system at different temperatures and power supply voltages.
Reference	REQ 7.1.1, REQ 7.1.2, REQ 7.1.3, REQ 7.1.4.
Prerequisites	IUT shall provide access to the interfaces specified in 4.2.
Set-up	12.3 -Device-level physical layer conformance test set-up 2
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the qualified LP. 4. The TC shall power up the IUT. 5. The TC shall wait 100 ms. 6. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.2348 with 001_2. 7. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 8. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 9. The TC shall wait 100 ms.

Item	Content
Number – Title	**DTC_07_system_reliability — System reliability under low attenuation channel**
	10. The TC shall check that the IUT MDIO register bit 2 of the MDIO register 1.1 is equal to 1_2. 11. The TC shall set the qualified LP to transmit continuously Ethernet frames of length randomly chosen between 1 byte and 1518 byte. Ethernet inter-frame gap shall be at least 13 byte length. 12. The TC shall wait 15 min. 13. The TC shall check that the qualified LP Ethernet frame error counter is equal to zero. 14. The TC shall check that the bit error rate reported by the qualified LP is lower than 10^{-12}. 15. The TC shall check that the OUT MDIO register bit 2 of the MDIO register 1.1 is equal to 1_2.
Iterations	Perform iterations with test case conditions T and U as specified in Table 11.
Expected response	Result of check in steps 10, 13, 14 and 15 shall be OK for all iterations.
Remarks	N/A

Table 19 specifies the device-level physical layer conformance test case DTC_08_link-up_IUT_normal for the low attenuation channel specified in subclause 13.3.

Table 19 — DTC_08_link-up_IUT_normal — Low attenuation channel

Item	Content
Number – Title	**DTC_08_link-up_IUT_normal — Link-up time when the LP and the IUT are in normal power state under low attenuation channel**
Purpose	This test case determines the link-up time when the LP and the IUT are in normal power state in a controlled network system at different temperatures and power supply voltages.
Reference	ISO 21111-3:2019 6.4, REQ 5.3.4, REQ 7.1.1, REQ 7.1.2, REQ 7.1.3, REQ 7.1.4.
Prerequisites	IUT shall provide access to the interfaces specified in 4.2.

Item	Content
Number – Title	**DTC_08_link-up_IUT_normal — Link-up time when the LP and the IUT are in normal power state under low attenuation channel**
Set-up	12.3 -Device-level physical layer conformance test set-up 2
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the qualified LP. 4. The TC shall disable qualified LP optical power transmission. 5. The TC shall power up the IUT. 6. The TC shall wait 100 ms. 7. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.2348 with 001_2. 8. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 9. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 10. The TC shall enable qualified LP optical power transmission. Then the TC shall reset to zero the T_LINKUP timer and start it. 11. The UT shall get the IUT link status at least once each ms. 12. When the IUT link status is equal to "bidirectional reliable link is established", the TC shall stop the T_LINKUP timer. 13. The UT shall monitor whether the IUT link status remains active for at least 750 ms. 14. The TC shall check that the value in the T_LINKUP timer is lower than 100 ms, and that the link did no go down during the monitoring time.
Iterations	Perform iterations with test case conditions T and U as specified in Table 11.
Expected response	Result of check in step 14 shall be OK for all iterations.
Remarks	N/A

Table 20 specifies the device-level physical layer conformance test case DTC_09_link-up_IUT_sleep for the low attenuation channel specified in subclause 13.3.

Table 20 — DTC_09_link-up_IUT_sleep — Low attenuation channel

Item	Content
Number – Title	**DTC_09_link-up_IUT_sleep — Link-up time when IUT is in sleep power state under low attenuation channel**
Purpose	This test case determines the link-up time when the IUT is in sleep power state in a controlled network system at different temperatures and power supply voltages. The procedure to wake-up the IUT is the reception of a WakeUp_request event.
Reference	ISO 21111-3:2019 6.4, REQ 5.3.2
Prerequisites	IUT shall provide access to the interfaces specified in 4.2.
Set-up	12.3 -Device-level physical layer conformance test set-up 2
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the qualified LP. 4. The TC shall disable qualified LP optical power transmission. 5. The TC shall power up the IUT. 6. The TC shall wait 100 ms. 7. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.2348 with 001_2. 8. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 9. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 10. The TC shall set IUT into sleep power state. 11. The TC shall enable qualified LP optical power transmission. Then the TC shall reset to zero the T_LINKUP timer and start it. 12. The UT shall get the IUT link status at least once each ms. 13. When the IUT link status is equal to "bidirectional reliable link is established", the TC shall stop the T_LINKUP timer. 14. The UT shall monitor whether the IUT link status remains active for at least 750 ms. 15. The TC shall check that the value in the T_LINKUP timer is lower than 100 ms, and that the link did no go down during the monitoring time.
Iterations	Perform iterations with test case conditions T and U as specified in Table 11.

Item	Content
Number – Title	**DTC_09_link-up_IUT_sleep — Link-up time when IUT is in sleep power state under low attenuation channel**
Expected response	Result of check in step 15 shall be OK for all iterations.
Remarks	N/A

Table 21 specifies the device-level physical layer conformance test case DTC_10_link-up_LP_IUT_sleep for the low attenuation channel specified in subclause 13.3.

Table 21 — DTC_10_link-up_LP_IUT_sleep — Low attenuation channel

Item	Content
Number – Title	**DTC_10_link-up_LP_IUT_sleep — Link-up time when the LP and the IUT are in sleep power state under high attenuation channel**
Purpose	This test case determines the link-up time when the LP and the IUT are in sleep power state in a controlled network system at different temperatures and power supply voltages. The LP wake-up is performed by a PHY_WakeUp_request.
Reference	ISO 21111-3:2019 6.4, REQ 5.3.1.
Prerequisites	IUT shall provide access to the interfaces specified in 4.2.
Set-up	12.3 -Device-level physical layer conformance test set-up 2
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the qualified LP. 4. The TC shall power up the IUT. 5. The TC shall wait 100 ms. 6. The TC shall set IUT and qualified LP into sleep power state. 7. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.2348 with 001_2. 8. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 9. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.

Item	Content
Number – Title	**DTC_10_link-up_LP_IUT_sleep — Link-up time when the LP and the IUT are in sleep power state under high attenuation channel**
	10. The TC shall set the qualified LP to generate the PHY_WakeUp.request. Then the TC shall reset to zero the T_LINKUP timer and start it. 11. The UT shall get the IUT link status at least once each ms. 12. When the IUT link status is equal to "bidirectional reliable link is established", the TC shall stop the T_LINKUP timer. 13. The UT shall monitor whether the IUT link status remains active for at least 750 ms. 14. The TC shall check that the value in the T_LINKUP timer is lower than 100 ms, and that the link did no go down during the monitoring time.
Iterations	Perform iterations with test case conditions T and U as specified in Table 11.
Expected response	Result of check in step 14 shall be OK for all iterations.
Remarks	N/A

Table 22 specifies the device-level physical layer conformance test case DTC_11_consumption_operation for the low attenuation channel specified in subclause 13.3.

Table 22 — DTC_11_consumption_operation — Low attenuation channel

Item	Content
Number – Title	**DTC_11_consumption_operation — IUT power consumption in operation under low attenuation channel**
Purpose	This test case determines the IUT power consumption in operation in a controlled network system at different temperatures and power supply voltages.
Reference	REQ 8.3.19
Prerequisites	IDD_{min} and IDD_{max} shall be provided by the test person. IUT shall provide access to the interfaces specified in 4.2.
Set-up	12.2 - Device-level physical layer conformance test set-up 1

Item	Content
Number – Title	**DTC_11_consumption_operation — IUT power consumption in operation under low attenuation channel**
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. Allow the chamber to stabilize at the target temperature before proceeding. 2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the qualified LP. 4. The TC shall power up the IUT. 5. The TC shall wait 100 ms. 6. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.2348 with 001_2. 7. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 8. The TC shall wait until the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 9. The TC shall wait 100 ms. 10. The TC shall check that the IUT MDIO register bit 2 of the MDIO register 1.1 is equal to 1_2. 11. The TC shall set the qualified LP to transmit continuously Ethernet frames of length randomly chosen between 1 byte and 1518 byte. Ethernet inter-frame gap shall be at least 13 byte length. 12. The TC shall wait 15 min. 13. The TC shall measure IDD_{Device}. 14. The TC shall check that IDD_{Device} is higher than IDD_{min} and lower than IDD_{max}.
Iterations	Perform iterations with test case conditions T and U as specified in Table 11.
Expected response	Result of checks in steps 10 and 14 shall be OK for all iterations.
Remarks	N/A

Table 23 specifies the device-level physical layer conformance test case DTC_12_consumption_sleep for the low attenuation channel specified in subclause 13.3.

Table 23 — DTC_12_consumption_sleep — Low attenuation channel

Item	Content
Number – Title	**DTC_12_consumption_sleep — IUT power consumption in sleep power state under low attenuation channel**
Purpose	This test case determines the IUT power consumption in sleep power state in a controlled network system at different temperatures and power supply voltages.
Reference	REQ 8.3.19
Prerequisites	IDD_DIS_{min} and IDD_DIS_{max} shall be provided by the test person. IUT shall provide access to the interfaces specified in 4.2.
Set-up	12.2 - Device-level physical layer conformance test set-up 1
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the qualified LP. 4. The TC shall power up the IUT. 5. The TC shall wait 100 ms. 6. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.2348 with 001_2. 7. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 8. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 9. The TC shall wait 100 ms. 10. The TC shall check that the IUT MDIO register bit 2 of the MDIO register 1.1 is equal to 1_2. 11. The TC shall set the LP inside the qualified LP to sleep power mode. 12. The TC shall set the IUT to sleep power mode. 13. The TC shall measure IDD_{Device}. 14. The TC shall check that IDD_{Device} is higher than IDD_DIS_{min} and lower than IDD_DIS_{max}.
Iterations	Perform iterations with test case conditions T and U as specified in Table 11.
Expected response	Result of checks in steps 10 and 14 shall be OK for all iterations.

Item	Content
Number – Title	**DTC_12_consumption_sleep — IUT power consumption in sleep power state under low attenuation channel**
Remarks	N/A

13.4 Wake-up and synchronized link sleep

The test cases in this Clause are required only for IUTs which implements wake-up and synchronized link sleep algorithms as described in ISO 21111-2 (see REQ 4.1), and covers the requirements specified in Clause 8.

Table 24 and Table 25 show the test cases specified in subclause 13.4.1 that cover the point-to-point wake-up and sleep time requirements respectively. The trigger of wake-up and sleep algorithms is determined by the reception of the PHY_Wakeup.request and PHY_Sleep.request primitives by the IUT. These primitives are commonly implemented by the change of a signal from a Wake_IO pin or from an associated microprocessor. The origin of such primitive (LP or IUT), the type of link between LP and IUT, and whether the link was already established (link active) or not (link passive), determines the different test cases defined.

Table 24 — Point to point wake-up time test cases

Origin of PHY_Wakeup.request	High attenuation channel		Low attenuation channel	
	Link Active	**Link Passive**	**Link Active**	**Link Passive**
LP	DTC_13_WUS_wake-up_time_LP_link_active	DTC_17_WUS_wake-up_time_LP_link_passive	N/A	N/A
IUT	DTC_14_WUS_wake-up_time_IUT_link_active	DTC_18_WUS_wake-up_time_IUT_link_passive	N/A	N/A

Table 25 — Point to point sleep time test cases

Origin of PHY_LinkSleep.request	High attenuation channel		Low attenuation channel	
	Link Active	**Link Passive**	**Link Active**	**Link Passive**
LP	DTC_15_WUS_sleep_time_LP_high_att	N/A	DTC_19_WUS_sleep_time_LP_low_att	N/A
IUT	DTC_14_WUS_wake-up_time_IUT_link_active	DTC_18_WUS_wake-up_time_IUT_link_passive	DTC_20_WUS_sleep_time_IUT_low_att	N/A

Table 26 shows the test cases specified in subclause 13.4.2 that cover the forwarding wake-up time requirements for an IUT with a Wake IO pin and two entities with communication with two LP (LP1 and LP2),

as shown in Figure 9. The origin of the PHY_Wakeup.request primitive is LP2 for all test cases, and the forwarding time is checked for multiple combinations of link status (active or passive), IUT power state (normal or sleep), and destination of the forwarding request (LP1 or Wake IO pin).

Table 26 — Forwarding wake-up time test cases

IUT power status	Forwarding destination LP1 (LP2 to IUT, IUT to LP1) link status				Forwarding destination Wake IO pin LP1 to IUT link status	
	(Active, Active)	**(Passive, Active)**	**(Active, Passive)**	**(Passive, Passive)**	**Active**	**Passive**
Normal	DTC_22_forward_wu_active_to_active	DTC_23_forward_wu_passive_to_active	DTC_21_forward_wu_active_to_passive	DTC_24_forward_wu_passive_to_passive	N/A	DTC_26_forward_wu_passive_to_wakeio_pin
Sleep	N/A	N/A	N/A	DTC_25_forward_wu_passive_to_passive_dev_off	N/A	N/A

13.4.1 Point-to-point test cases

Table 27 specifies the device-level physical layer conformance test case DTC_13_WUS_wake-up_time_LP_link_active for the high attenuation channel specified in subclause 13.2.

Table 27 — DTC_13_WUS_wake-up_time_LP_link_active — Wake-up and synchronized link sleep

Item	Content
Number – Title	**DTC_13_WUS_wake-up_time_LP_link_active — Wake-up time for event generated at LP, link active and high attenuation channel.**
Purpose	This test case determines the wake-up time when the wake_up event is generated in the LP, the link is active and a high attenuation channel is used and check that it is below the maximum acceptable value.
Reference	ISO 21111-2:2019, REQ 8.3.12
Prerequisites	IUT shall provide access to the interfaces specified in 4.2. IUT and LP1 shall support wake-up and synchronized link sleep functionality described in ISO 21111-2:2019.
Set-up	12.2 Device-level physical layer conformance test set-up 1

Item	Content
Number – Title	**DTC_13_WUS_wake-up_time_LP_link_active — Wake-up time for event generated at LP, link active and high attenuation channel.**
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the LP. 4. The TC shall power up the IUT. 5. The TC shall wait 100 ms. 6. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.2348 with 001_2. 7. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 8. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 9. The TC shall wait 100 ms. 10. The TC shall check that the IUT MDIO register bit 2 of the MDIO register 1.1 is equal to 1_2. 11. The TC shall set the LP1 to transmit continuously Ethernet frames of length randomly chosen between 1 byte and 1518 byte. Ethernet inter-frame gap shall be at least 13 byte length. 12. The TC shall set the LP1 to generate a PHY_WakeUp.request primitive. Then the TC shall reset to zero the T_WAKEUP timer and start it. 13. When the PHY_WakeUp.indication primitive is generated by the IUT, the TC shall stop the T_WAKEUP timer. 14. The TC shall check that the value in the T_WAKEUP timer is lower than 2 ms.
Iterations	Perform one iteration with test case conditions T and U equal to T_{typ} and U_{typ}.
Expected response	Result of check in steps 10 and 14 shall be OK.
Remarks	N/A

Table 28 specifies the device-level physical layer conformance test case DTC_14_WUS_wake-up_time_IUT_link_active for the high attenuation channel specified in subclause 13.2.

Table 28 — DTC_14_WUS_wake-up_time_IUT_link_active— Wake-up and synchronized link sleep

Item	Content
Number – Title	**DTC_14_WUS_wake-up_time_IUT_link_active — Wake_up time for event generated at IUT, link active and high attenuation channel.**
Purpose	This test case determines the wake_up time when the wake_up event is generated in the IUT, the link is active and a high attenuation channel is used and check that it is below the maximum acceptable value.
Reference	ISO 21111-2:2019, REQ 8.3.12
Prerequisites	IUT shall provide access to the interfaces specified in 4.2. IUT and LP1 shall support wake-up and synchronized link sleep functionality described in ISO 21111-2:2019.
Set-up	12.2 Device-level physical layer conformance test set-up 1.
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the LP. 4. The TC shall power up the IUT. 5. The TC shall wait 100 ms. 6. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.2348 with 001_2. 7. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 8. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 9. The TC shall wait 100 ms. 10. The TC shall check that the IUT MDIO register bit 2 of the MDIO register 1.1 is equal to 1_2. 11. The TC shall set the LP1 to transmit continuously Ethernet frames of length randomly chosen between 1 byte and 1518 byte. Ethernet inter-frame gap shall be at least 13 byte length. 12. The TC shall set the IUT to generate the PHY_WakeUp.request primitive. Then the TC shall reset to zero the T_WAKEUP timer and start it. 13. When the PHY_WakeUp.indication is generated in the LP, the TC shall stop the T_WAKEUP timer. 14. The TC shall check that the value in the T_WAKEUP timer is lower than 2 ms.

Item	Content
Number – Title	**DTC_14_WUS_wake-up_time_IUT_link_active — Wake_up time for event generated at IUT, link active and high attenuation channel.**
Iterations	Perform one iteration with test case conditions T and U equal to T_{typ} and U_{typ}.
Expected response	Result of check in steps 10 and 14 shall be OK.
Remarks	N/A

Table 29 specifies the device-level physical layer conformance test case DTC_15_WUS_sleep_time_LP_high_att for the high attenuation channel specified in subclause 13.2.

Table 29 — DTC_15_WUS_sleep_time_LP_high_att — Wake-up and synchronized link sleep

Item	Content
Number – Title	**DTC_15_WUS_sleep_time_LP_high_att — Synchronized link sleep time for event generated at LP, link active and high attenuation channel.**
Purpose	This test case determines the synchronized link sleep algorithm time when the initial synchronized link sleep event is generated in the LP, the link is active and a high attenuation channel is used and check that it is below the maximum acceptable value.
Reference	ISO 21111-2:2019, REQ 8.3.11
Prerequisites	IUT shall provide access to the interfaces specified in 4.2. IUT and LP shall support wake-up and synchronized link sleep functionality described in ISO 21111-2:2019. IUT and LP shall be configured to accept any LinkSleep_request events, as described in ISO 21111-2:2019.
Set-up	12.2 Device-level physical layer conformance test set-up 1.
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the LP. 4. The TC shall power up the IUT.

Item	Content
Number – Title	**DTC_15_WUS_sleep_time_LP_high_att — Synchronized link sleep time for event generated at LP, link active and high attenuation channel.**
	5. The TC shall wait 100 ms. 6. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.2348 with 001_2. 7. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 8. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 9. The TC shall wait 100 ms. 10. The TC shall check that the IUT MDIO register bit 2 of the MDIO register 1.1 is equal to 1_2. 11. The TC shall set the qualified LP to transmit continuously Ethernet frames of length randomly chosen between 1 byte and 1518 byte. Ethernet inter-frame gap shall be at least 13 byte length. 12. The TC shall set the LP to generate the PHY_LinkSleep.request. Then the TC shall reset to zero the T_SLEEP timer and start it. 13. When the PHY_LinkSleep.indication is generated with its parameter equal to TRUE at the LP, the TC shall stop the T_SLEEP timer. 14. The TC shall check that the value in the T_SLEEP timer is lower than 50 ms.
Iterations	Perform one iteration with test case conditions T and U equal to T_{typ} and U_{typ}.
Expected response	Result of check in steps 10 and 14s hall be OK.
Remarks	N/A

Table 30 specifies the device-level physical layer conformance test case DTC_16_WUS_sleep_time_IUT_high_att for the high attenuation channel specified in subclause 13.2.

Table 30 — DTC_16_WUS_sleep_time_IUT_high_att — Wake-up and synchronized link sleep

Item	Content
Number – Title	**DTC_16_WUS_sleep_time_IUT_high_att — Synchronized link sleep time for event generated at IUT, link active and high attenuation channel.**
Purpose	This test case determines the synchronized link sleep algorithm time when the initial synchronized link sleep event is generated in the IUT, the link is active and a high attenuation channel is used and check that it is below the maximum acceptable value.

Item	Content
Number – Title	**DTC_16_WUS_sleep_time_IUT_high_att — Synchronized link sleep time for event generated at IUT, link active and high attenuation channel.**
Reference	ISO 21111-2:2019, REQ 8.3.11
Prerequisites	IUT shall provide access to the interfaces specified in 4.2. IUT and LP shall support wake-up and synchronized link sleep functionality described in ISO 21111-2:2019. IUT and LP shall be configured to accept any LinkSleep_request events, as described in ISO 21111-2:2019.
Set-up	12.2 Device-level physical layer conformance test set-up 1.
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the LP. 4. The TC shall power up the IUT. 5. The TC shall wait 100 ms. 6. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.2348 with 001_2. 7. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 8. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 9. The TC shall wait 100 ms. 10. The TC shall check that the IUT MDIO register bit 2 of the MDIO register 1.1 is equal to 1_2. 11. The TC shall set the qualified LP to transmit continuously Ethernet frames of length randomly chosen between 1 byte and 1518 byte. Ethernet inter-frame gap shall be at least 13 byte length. 12. The TC shall set the IUT to generate the PHY_LinkSleep.request. Then the TC shall reset to zero the T_SLEEP timer and start it. 13. When the PHY_LinkSleep.indication is received with its parameter equal to TRUE in the IUT, the TC shall stop the T_SLEEP timer. 14. The TC shall check that the value in the T_SLEEP timer is lower than 50 ms.
Iterations	Perform one iteration with test case conditions T and U equal to T_{typ} and U_{typ}.

Item	Content
Number – Title	**DTC_16_WUS_sleep_time_IUT_high_att — Synchronized link sleep time for event generated at IUT, link active and high attenuation channel.**
Expected response	Result of check in steps 10 and 14 shall be OK.
Remarks	N/A

Table 31 specifies the device-level physical layer conformance test case DTC_17_WUS_wake-up_time_LP_link_passive for the high attenuation channel specified in subclause 13.2.

Table 31 — DTC_17_WUS_wake-up_time_LP_link_passive — Wake-up and synchronized link sleep

Item	Content
Number – Title	**DTC_17_WUS_wake-up_time_LP_link_passive — Wake_up time for event generated at LP, link passive and high attenuation channel.**
Purpose	This test case determines the wake_up time when the wake_up event is generated in the LP, the link is passive and a high attenuation channel is used and check that it is below the maximum acceptable value.
Reference	ISO 21111-2:2019, REQ 8.3.12
Prerequisites	IUT shall provide access to the interfaces specified in 4.2. IUT and LP shall support wake-up and synchronized link sleep functionality described in ISO 21111-2:2019 and ISO 21111-3:2019.
Set-up	12.2 Device-level physical layer conformance test set-up 1.
Step	The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. 1. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 2. The TC shall power up the LP. 3. The TC shall power up the IUT. 4. The TC shall wait 100 ms. 5. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.2348 with 001_2. 6. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2.

Item	Content
Number – Title	**DTC_17_WUS_wake-up_time_LP_link_passive — Wake_up time for event generated at LP, link passive and high attenuation channel.**
	7. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 8. The TC shall wait 100 ms. 9. The TC shall check that the IUT MDIO register bit 2 of the MDIO register 1.1 is equal to 1_2. 10. The TC shall set the qualified LP to transmit continuously Ethernet frames of length randomly chosen between 1 byte and 1518 byte. Ethernet inter-frame gap shall be at least 13 byte length. 11. The TC shall stop the LP to transmit Ethernet frames. 12. The TC shall set the IUT into sleep power state as specified in ISO 21111-3:2019. 13. The TC shall set the LP to generate the PHY_WakeUp.request. Then the TC shall reset to zero the T_WAKEUP timer and start it. 14. When the PHY_WakeUp.indication is generated at the IUT, the TC shall stop the T_WAKEUP timer. 15. The TC shall check that the value in the T_WAKEUP timer is lower than 2 ms.
Iterations	Perform one iteration with test case conditions T and U equal to T_{typ} and U_{typ}.
Expected response	Result of check in steps 9 and 15 shall be OK.
Remarks	N/A

Table 32 specifies the device-level physical layer conformance test case DTC_18_WUS_wake-up_time_IUT_link_passive for the high attenuation channel specified in subclause 13.2.

Table 32 — DTC_18_WUS_wake-up_time_IUT_link_passive — Wake-up and synchronized link sleep

Item	Content
Number – Title	**DTC_18_WUS_wake-up_time_IUT_link_passive — Wake_up time for event generated at IUT, link passive and high attenuation channel.**
Purpose	This test case determines the wake_up time when the wake_up event is generated in the IUT, the link is passive and a high attenuation channel is used and check that it is below the maximum acceptable value.
Reference	ISO 21111-2:2019, REQ 8.3.12

Item	Content
Number – Title	**DTC_18_WUS_wake-up_time_IUT_link_passive — Wake_up time for event generated at IUT, link passive and high attenuation channel.**
Prerequisites	IUT shall provide access to the interfaces specified in 4.2. IUT and LP shall support wake-up and synchronized link sleep functionality described in ISO 21111-2:2019.
Set-up	12.2 Device-level physical layer conformance test set-up 1.
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the LP. 4. The TC shall power up the IUT. 5. The TC shall wait 100 ms. 6. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.2348 with 001_2. 7. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 8. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 9. The TC shall wait 100 ms. 10. The TC shall check that the IUT MDIO register bit 2 of the MDIO register 1.1 is equal to 1_2. 11. The TC shall set the LP to transmit continuously Ethernet frames of length randomly chosen between 1 byte and 1518 byte. Ethernet inter-frame gap shall be at least 13 byte length. 12. The TC shall stop the LP to transmit Ethernet frames. 13. The TC shall set the LP to sleep power state as specified in ISO 21111-3:2019. 14. The TC shall set the IUT to generate the PHY_WakeUp.request primitive. Then the TC shall reset to zero the T_WAKEUP timer and start it. 15. When the PHY_WakeUp.indication is generated in the LP, the TC shall stop the T_WAKEUP timer. 16. The TC shall check that the value in the T_WAKEUP timer is lower than 2 ms.
Iterations	Perform one iteration with test case conditions T and U equal to T_{typ} and U_{typ}.
Expected response	Result of check in steps 10 and 16 shall be OK.

Item	Content
Number – Title	**DTC_18_WUS_wake-up_time_IUT_link_passive — Wake_up time for event generated at IUT, link passive and high attenuation channel.**
Remarks	N/A

Table 33 specifies the device-level physical layer conformance test case DTC_19_WUS_sleep_time_LP_low_att for the low attenuation channel specified in subclause 13.3.

Table 33 — DTC_19_WUS_sleep_time_LP_low_att — Wake-up and synchronized link sleep

Item	Content
Number – Title	**DTC_19_WUS_sleep_time_LP_low_att — Synchronized link sleep time for event generated at LP, link active and low attenuation channel.**
Purpose	This test case determines the synchronized link sleep algorithm time when the initial synchronized link sleep event is generated in the LP, the link is active and a low attenuation channel is used and check that it is below the maximum acceptable value.
Reference	ISO 21111-2:2019, REQ 8.3.11
Prerequisites	IUT shall provide access to the interfaces specified in 4.2. IUT and LP shall support wake-up and synchronized link sleep functionality described in ISO 21111-2:2019. IUT and LP shall be configured to accept any LinkSleep_request events, as described in ISO 21111-2:2019.
Set-up	12.3 Device-level physical layer conformance test set-up 2.
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the LP. 4. The TC shall power up the IUT. 5. The TC shall wait 100 ms. 6. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.2348 with 001_2. 7. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2.

Item	Content
Number – Title	**DTC_19_WUS_sleep_time_LP_low_att — Synchronized link sleep time for event generated at LP, link active and low attenuation channel.**
	8. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 9. The TC shall wait 100 ms. 10. The TC shall check that the IUT MDIO register bit 2 of the MDIO register 1.1 is equal to 1_2. 11. The TC shall set the LP to transmit continuously Ethernet frames of length randomly chosen between 1 byte and 1518 byte. Ethernet inter-frame gap shall be at least 13 byte length. 12. The TC shall set the LP to generate the PHY_LinkSleep.request. Then the TC shall reset to zero the T_SLEEP timer and start it. 13. When the PHY_LinkSleep.indication is generated with its parameter equal to TRUE in the LP, the TC shall stop the T_SLEEP timer. 14. The TC shall check that the value in the T_SLEEP timer is lower than 50 ms.
Iterations	Perform one iteration with test case conditions T and U equal to T_{typ} and U_{typ}.
Expected response	Result of check in steps 10 and 14 shall be OK.
Remarks	N/A

Table 34 specifies the device-level physical layer conformance test case DTC_20_WUS_sleep_time_IUT_low_att for the low attenuation channel specified in subclause 13.3.

Table 34 — DTC_20_WUS_sleep_time_IUT_low_att — Wake-up and synchronized link sleep

Item	Content
Number – Title	**DTC_20_WUS_sleep_time_IUT_low_att — Synchronized link sleep time for event generated at IUT, link active and low attenuation channel.**
Purpose	This test case determines the synchronized link sleep algorithm time when the initial synchronized link sleep event is generated in the IUT, the link is active and a low attenuation channel is used and check that it is below the maximum acceptable value.
Reference	ISO 21111-2:2019, REQ 8.3.12
Prerequisites	IUT shall provide access to the interfaces specified in 4.2.

Item	Content
Number – Title	**DTC_20_WUS_sleep_time_IUT_low_att — Synchronized link sleep time for event generated at IUT, link active and low attenuation channel.**
	IUT and LP shall support wake-up and synchronized link sleep functionality described in ISO 21111-2:2019. IUT and qualified LP shall be configured to accept any LinkSleep_request events, as described in ISO 21111-2:2019.
Set-up	12.3 Device-level physical layer conformance test set-up 2.
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the LP. 4. The TC shall power up the IUT. 5. The TC shall wait 100 ms. 6. The UT shall write the IUT MDIO register bit 12 to bit 10 of the MDIO register 3.2348 with 001_2. 7. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 8. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 9. The TC shall wait 100 ms. 10. The TC shall check that the IUT MDIO register bit 2 of the MDIO register 1.1 is equal to 1_2. 11. The TC shall set the qualified LP to transmit continuously Ethernet frames of length randomly chosen between 1 byte and 1518 byte. Ethernet inter-frame gap shall be at least 13 byte length. 12. The TC shall set the IUT to generate the PHY_LinkSleep.request. Then the TC shall reset to zero the T_SLEEP timer and start it. 13. When the PHY_LinkSleep.indication is received with its parameter equal to TRUE in the IUT, the TC shall stop the T_SLEEP timer. 14. The TC shall check that the value in the T_SLEEP timer is lower than 50 ms.
Iterations	Perform one iteration with test case conditions T and U equal to T_{typ} and U_{typ}.
Expected response	Result of check in steps 10 and 14 shall be OK.
Remarks	N/A

13.4.2 Device with multiple physical entities test cases

Table 35 specifies the device-level physical layer conformance test case DTC_21_forward_wu_active_to_passive for the low attenuation channel specified in subclause 13.3.

Table 35 — DTC_21_forward_wu_active_to_passive — Wake-up and synchronized link sleep

Item	Content
Number – Title	**DTC_21_forward_wu_active_to_passive — Forwarding wake-up request from active to passive link.**
Purpose	This test case determines that a wake-up request received by a device over the active link with LP2 is forwarded within the expected time to LP1 via a passive link.
Reference	ISO 21111-2:2019, REQ 8.3.13, REQ 8.3.14, REQ 8.3.15
Prerequisites	IUT shall provide access to the interfaces specified in 4.2. IUT, LP1 and LP2 shall support wake-up functionality described in ISO 21111-2:2019.
Set-up	9.3 Interoperability test set-up 3
Step	1. The TC shall set the IUT climatic chamber temperature to T_{typ}. 2. The TC shall set the IUT power supply voltage to U_{typ}. 3. The TC shall set LP1 climatic chamber temperature to T_{typ}. 4. The TC shall set LP1 power supply voltage to U_{typ}. 5. The TC shall set LP2 climatic chamber temperature to T_{typ}. 6. The TC shall set LP2 power supply voltage to U_{typ}. 7. The TC shall power up the LP1 8. The TC shall power up the LP2 9. The TC shall power up the IUT 10. The TC shall set LP1 into sleep power state 11. The TC shall set LP2 into normal power state 12. The TC shall set nGBASE-AU entity 2 in device into normal power state 13. The TC shall set nGBASE-AU entity 1 in device into sleep power state 14. The TC shall wait 100 ms 15. The TC shall set T_WKP_FWD timer to zero 16. The TC shall check that link status in nGBASE-AU entity 1 of the device is not equal to "bidirectional reliable link is established" 17. The TC shall check that link status in nGBASE-AU entity 2 of the device is equal to "bidirectional reliable link is established" 18. The TC shall set the LP2 to generate a PHY_WakeUp.request primitive. The TC shall start T_WKP_FWD timer

Item	Content
Number – Title	**DTC_21_forward_wu_active_to_passive — Forwarding wake-up request from active to passive link.**
	19. The TC shall wait till LP1 generates a PHY_WakeUp.indication. The TC shall stop T_WKP_FWD timer 20. The TC shall check that T_WKP_FWD is lower than (TWU_Link_Active + TWU_Forwarding + TWU_Link_Passive) = 5 ms
Iterations	N/A
Expected response	Result of check in step 20 shall be OK.
Remarks	N/A

Table 36 specifies the device-level physical layer conformance test case DTC_22_forward_wu_active_to_active for the low attenuation channel specified in subclause 13.3.

Table 36 — DTC_22_forward_wu_active_to_active — Wake-up and synchronized link sleep

Item	Content
Number – Title	**DTC_22_forward_wu_active_to_active — Forwarding wake-up request from active to active link.**
Purpose	This test case determines that a wake-up request received by a device over the active link with LP2 is forwarded within the expected time to LP1 via an active link.
Reference	ISO 21111-2:2019 REQ 8.3.13, REQ 8.3.14, REQ 8.3.15
Prerequisites	IUT shall provide access to the interfaces specified in 4.2. IUT, LP1 and LP2 shall support wake-up functionality described in ISO 21111-2:2019.
Set-up	9.3 Interoperability test set-up 3
Step	1. The TC shall set the IUT climatic chamber temperature to T_{typ}. 2. The TC shall set the IUT power supply voltage to U_{typ}. 3. The TC shall set LP1 climatic chamber temperature to T_{typ}. 4. The TC shall set LP1 power supply voltage to U_{typ}. 5. The TC shall set LP2 climatic chamber temperature to T_{typ}. 6. The TC shall set LP2 power supply voltage to U_{typ}.

Item	Content
Number – Title	**DTC_22_forward_wu_active_to_active — Forwarding wake-up request from active to active link.**
	7. The TC shall power up the LP1 8. The TC shall power up the LP2 9. The TC shall power up the device 10. The TC shall set LP1 into normal power state 11. The TC shall set LP2 into normal power state 12. The TC shall set nGBASE_AU entity 2 in device into normal power state 13. The TC shall set nGBASE_AU entity 1 in device into normal power state 14. The TC shall wait 100 ms 15. The TC shall set T_WKP_FWD timer to zero 16. The TC shall check that link status in nGBASE_AU entity 1 of the device is equal to "bidirectional reliable link is established" 17. The TC shall check that link status in nGBASE_AU entity 2 of the device is equal to "bidirectional reliable link is established" 18. The TC shall set the LP2 to generate a PHY_WakeUp.request primitive. The TC shall start T_WKP_FWD timer 19. The TC shall wait till LP1 generates a PHY_WakeUp.indication. The TC shall stop T_WKP_FWD timer 20. The TC shall check that T_WKP_FWD is lower than (TWU_Link_Active + TWU_Forwarding + TWU_Link_Active) = 5 ms
Iterations	N/A
Expected response	Result of check in step 20 shall be OK.
Remarks	N/A

Table 37 specifies the device-level physical layer conformance test case DTC_23_forward_wu_passive_to_active for the low attenuation channel specified in subclause 13.3.

Table 37 — DTC_23_forward_wu_passive_to_active — Wake-up and synchronized link sleep

Item	Content
Number – Title	**DTC_23_forward_wu_passive_to_active — Forwarding wake-up request from passive to active link.**
Purpose	This test case determines that a wake-up request received by a device over the passive link with LP2 is forwarded within the expected time to LP1 via an active link.

Item	Content
Number – Title	**DTC_23_forward_wu_passive_to_active — Forwarding wake-up request from passive to active link.**
Reference	ISO 21111-2:2019, REQ 8.3.13, REQ 8.3.14, REQ 8.3.15
Prerequisites	IUT shall provide access to the interfaces specified in 4.2. IUT, LP1 and LP2 shall support wake-up functionality described in ISO 21111-2:2019.
Set-up	9.3 Interoperability test set-up 3
Step	1. The TC shall set the IUT climatic chamber temperature to T_{typ}. 2. The TC shall set the IUT power supply voltage to U_{typ}. 3. The TC shall set LP1 climatic chamber temperature to T_{typ}. 4. The TC shall set LP1 power supply voltage to U_{typ}. 5. The TC shall set LP2 climatic chamber temperature to T_{typ}. 6. The TC shall set LP2 power supply voltage to U_{typ}. 7. The TC shall power up the LP1 8. The TC shall power up the LP2 9. The TC shall power up the device 10. The TC shall set LP1 into sleep power state 11. The TC shall set LP2 into normal power state 12. The TC shall set nGBASE_AU entity 2 in device into normal power state 13. The TC shall set nGBASE_AU entity 1 in device into sleep power state 14. The TC shall wait 100 ms 15. The TC shall set T_WKP_FWD timer to zero 16. The TC shall check that link status in nGBASE_AU entity 1 of the device is not equal to "bidirectional reliable link is established" 17. The TC shall check that link status in nGBASE_AU entity 2 of the device is equal to "bidirectional reliable link is established" 18. The TC shall set the LP2 to generate a PHY_WakeUp.request primitive. The TC shall start T_WKP_FWD timer 19. The TC shall wait till LP1 generates a PHY_WakeUp.indication. The TC shall stop T_WKP_FWD timer 20. The TC shall check that T_WKP_FWD is lower than (TWU_Link_Passive + TWU_Forwarding + TWU_Link_Active) = 5 ms
Iterations	N/A
Expected response	Result of check in step 20 shall be OK.

Item	Content
Number – Title	**DTC_23_forward_wu_passive_to_active — Forwarding wake-up request from passive to active link.**
Remarks	N/A

Table 38 specifies the device-level physical layer conformance test case DTC_24_forward_wu_passive_to_passive for the low attenuation channel specified in subclause 13.3.

Table 38 — DTC_24_forward_wu_passive_to_passive — Wake-up and synchronized link sleep

Item	Content
Number – Title	**DTC_24_forward_wu_passive_to_passive — Forwarding wake-up request from passive to passive link.**
Purpose	This test case determines that a wake-up request received by a device over the passive link with LP2 is forwarded within the expected time to LP1 via a passive link. The power supply that provides energy to the nGBASE_AU entities in the device is on.
Reference	ISO 21111-2:2019, REQ 8.3.13, REQ 8.3.14, REQ 8.3.15
Prerequisites	IUT shall provide access to the interfaces specified in 4.2. IUT, LP1 and LP2 shall support wake-up functionality described in ISO 21111-2:2019.
Set-up	9.3 Interoperability test set-up 3
Step	1. The TC shall set the IUT climatic chamber temperature to T_{typ}. 2. The TC shall set the IUT power supply voltage to U_{typ}. 3. The TC shall set LP1 climatic chamber temperature to T_{typ}. 4. The TC shall set LP1 power supply voltage to U_{typ}. 5. The TC shall set LP2 climatic chamber temperature to T_{typ}. 6. The TC shall set LP2 power supply voltage to U_{typ}. 7. The TC shall power up the LP1 8. The TC shall power up the LP2 9. The TC shall power up the device 10. The TC shall set LP1 into sleep power state 11. The TC shall set LP2 into sleep power state 12. The TC shall set nGBASE_AU entity 2 in device into sleep power state 13. The TC shall set nGBASE_AU entity 1 in device into sleep power state 14. The TC shall wait 100 ms 15. The TC shall set T_WKP_FWD timer to zero

Item	Content
Number – Title	**DTC_24_forward_wu_passive_to_passive — Forwarding wake-up request from passive to passive link.**
	16. The TC shall check that link status in nGBASE_AU entity 1 of the device is not equal to "bidirectional reliable link is established" 17. The TC shall check that link status in nGBASE_AU entity 2 of the device is not equal to "bidirectional reliable link is established" 18. The TC shall set the LP2 to generate a PHY_WakeUp.request primitive. The TC shall start T_WKP_FWD timer 19. The TC shall wait till LP1 generates a PHY_WakeUp.indication. The TC shall stop T_WKP_FWD timer 20. The TC shall check that T_WKP_FWD is lower than (TWU_Link_Passive + TWU_Forwarding + TWU_Link_Passive) = 5 ms
Iterations	N/A
Expected response	Result of check in step 20 shall be OK.
Remarks	N/A

Table 39 specifies the device-level physical layer conformance test case DTC_25_forward_wu_passive_to_passive_dev_off for the low attenuation channel specified in subclause 13.3.

Table 39 — DTC_25_forward_wu_passive_to_passive_dev_off — Wake-up and synchronized link sleep

Item	Content
Number – Title	**DTC_25_forward_wu_passive_to_passive_dev_off — Forwarding wake-up request from passive to passive link with device entities power supply off.**
Purpose	This test case determines that a wake-up request received by a device over the passive link with LP2 is forwarded within the expected time to LP1 via a passive link. The power supply that provides energy to the nGBASE_AU entities in the device is off, providing only a small amount of energy to detect the presence of activity in the channel as specified in ISO 21111-2.
Reference	ISO 21111-2:2019, REQ 8.3.13, REQ 8.3.14, REQ 8.3.15, REQ 8.3.16, REQ 8.3.17.
Prerequisites	IUT shall provide access to the interfaces specified in 4.2.

Item	Content
Number – Title	**DTC_25_forward_wu_passive_to_passive_dev_off — Forwarding wake-up request from passive to passive link with device entities power supply off.**
	IUT, LP1 and LP2 shall support wake-up functionality described in ISO 21111-2:2019.
Set-up	9.3 Interoperability test set-up 3
Step	1. The TC shall set the IUT climatic chamber temperature to T_{typ}. 2. The TC shall set the IUT power supply voltage to U_{typ}. 3. The TC shall set LP1 climatic chamber temperature to T_{typ}. 4. The TC shall set LP1 power supply voltage to U_{typ}. 5. The TC shall set LP2 climatic chamber temperature to T_{typ}. 6. The TC shall set LP2 power supply voltage to U_{typ}. 7. The TC shall power up the LP1 8. The TC shall power up the LP2 9. The TC shall power up the device 10. The TC shall set LP1 into sleep power state 11. The TC shall set LP2 into sleep power state 12. Power off the device 13. The TC shall wait 100 ms 14. The TC shall set T_WKP_FWD timer to zero 15. The TC shall check that link status in nGBASE_AU entity 1 of the device is not equal to "bidirectional reliable link is established" 16. The TC shall check that link status in nGBASE_AU entity 2 of the device is not equal to "bidirectional reliable link is established" 17. The TC shall set the LP2 to generate a PHY_WakeUp.request primitive. The TC shall start T_WKP_FWD timer 18. The TC shall wait till LP1 generates a PHY_WakeUp.indication. The TC shall stop T_WKP_FWD timer 19. The TC shall check that T_WKP_FWD is lower than (TWU_Link_Passive + TWU_Forwarding + T_Powersupply_Stable + T_Initialization + TWU_Link_Passive) = 20 ms
Iterations	N/A
Expected response	Result of check in step 19 shall be OK.
Remarks	N/A

Table 40 specifies the device-level physical layer conformance test case DTC_26_forward_wu_passive_to_wakeio_pin for the low attenuation channel specified in subclause 13.3.

Table 40 — DTC_26_forward_wu_passive_to_wakeio_pin — Wake-up and synchronized link sleep

Item	Content
Number – Title	**DTC_26_forward_wu_passive_to_wakeio_pin — Forwarding wake-up request from passive link to WAKE_IO pin.**
Purpose	This test case determines that a wake-up request received by a device over the passive link with LP1 is forwarded within the expected time to LP1 via the WAKE_IO pin. The power supply that provides energy to the nGBASE_AU entities in the device is on.
Reference	ISO 21111-2:2019, REQ 8.3.13, REQ 8.3.14, REQ 8.3.15, REQ 8.3.16, REQ 8.3.17.
Prerequisites	IUT shall provide access to the interfaces specified in 4.2. IUT, LP1 and LP2 shall support wake-up functionality described in ISO 21111-2:2019.
Set-up	9.3 Interoperability test set-up 3
Step	1. The TC shall set the IUT climatic chamber temperature to T_{typ}. 2. The TC shall set the IUT power supply voltage to U_{typ}. 3. The TC shall set LP1 climatic chamber temperature to T_{typ}. 4. The TC shall set LP1 power supply voltage to U_{typ}. 5. The TC shall set LP2 climatic chamber temperature to T_{typ}. 6. The TC shall set LP2 power supply voltage to U_{typ}. 7. The TC shall power up the LP1 8. The TC shall power up the LP2 9. The TC shall power up the IUT 10. The TC shall set LP1 into sleep power state 11. The TC shall set LP2 into normal power state 12. The TC shall wait 100 ms 13. The TC shall set T_WKP_FWD timer to zero 14. The TC shall check that link status in nGBASE_AU entity 1 of the device is not equal to "bidirectional reliable link is established" 15. The TC shall set the LP2 to generate a PHY_WakeUp.request primitive. The TC shall start T_WKP_FWD timer 16. The TC shall wait till a valid wake up signal per Open Alliance TC10 is detected at the IUT Wake IO pin. The TC shall stop T_WKP_FWD timer 17. The TC shall check that T_WKP_FWD is lower than (TWU_Link_Passive + TWU_Forwarding + TWU_WakeIO) = 4 ms

Item	Content
Number – Title	**DTC_26_forward_wu_passive_to_wakeio_pin — Forwarding wake-up request from passive link to WAKE_IO pin.**
Iterations	N/A
Expected response	Result of check in step 17 shall be OK.
Remarks	N/A

14 PHYSICAL LAYER (PHY) LEVEL CONFORMANCE TEST PLAN

14.1 General

The physical layer (PHY) level conformance test plan is a set of test cases that check physical layer requirements related to the transmitted or received optical signal. The entity under test for this test plan is the PHY itself, and it is denoted as PUT (see Figure 1).

This test plan is structured in test groups. The test cases in the same test group share the same test set-up.

First test group includes the test cases to check compliance of the optical transmitter (see 14.2).

Second test group includes the test cases to check compliance of the optical receiver (see 14.3).

14.2 Optical transmitter measurements

Table 41 specifies the PHY-level conformance test case PLCT_1_AOP for measuring PUT transmitter optical parameters.

Table 41 — PLCT_1_AOP — Optical transmitter measurements

Item	Content
Number – Title	**PLCT_1_AOP — Optical PUT transmitter AOP at TP2**
Purpose	This test case determines the PUT AOP at TP2 and checks that it is in the expected range.
Reference	IEEE 802.3cz:2023, 166.6.4.3 and OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.2
Prerequisites	PUT shall provide access to the interfaces specified in 4.2.

Item	Content
Number – Title	**PLCT_1_AOP — Optical PUT transmitter AOP at TP2**
Set-up	OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.2, Figure 4.
Step	1. According to OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.2.2
Iterations	Perform iterations with test case conditions T and U as specified in Table 11.
Expected response	AOP shall be in the range specified in IEEE 802.3cz:2023, 166.6.4.3 and OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.2
Remarks	None

Table 42 specifies the PHY-level conformance test case PLCT_2_AOP_off for measuring PUT transmitter optical parameters.

Table 42 — PLCT_2_AOP_off — Optical transmitter measurements

Item	Content
Number – Title	**PLCT_2_AOP_off — Optical PUT transmitter AOP when transmission is set to OFF at TP2**
Purpose	This test case determines the PUT AOP at TP2 when the transmitter is set to off and check that it is below the value specified.
Reference	IEEE 802.3cz:2023, 166.6.4.3 and OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.2
Prerequisites	PUT shall provide access to the interfaces specified in 4.2.
Set-up	OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.2, Figure 4.
Step	According to OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.2.2

Item	Content
Number – Title	**PLCT_2_AOP_off — Optical PUT transmitter AOP when transmission is set to OFF at TP2**
Iterations	Perform iterations with test case conditions T and U as specified in Table 11.
Expected response	AOP obtained shall be lower than the maximum value specified in IEEE 802.3cz:2023, 166.6.4.3 and OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.2.
Remarks	None.

Table 43 specifies the PHY-level conformance test case PLCT_3_TDFOM for measuring PUT transmitter optical parameters.

Table 43 — PLCT_3_TDFOM — Optical transmitter measurements

Item	Content
Number – Title	**PLCT_3_TDFOM — Optical PUT transmitter distortion figure of merit (TDFOM) at TP2**
Purpose	This test case determines the PUT transmitter distortion figure of merit at TP2 and checks that it is in the expected range.
Reference	IEEE 802.3cz:2023, 166.6.4.8 and OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.3.
Prerequisites	IUT shall provide access to the interfaces specified in 4.2. TDFOM shall be the first parameter measured for the OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.3 test group.
Set-up	OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.3, Figure 6.
Step	According to OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.3.2
Iterations	Perform iterations with test case conditions T and U as specified in Table 11.

Item	Content
Number – Title	**PLCT_3_TDFOM — Optical PUT transmitter distortion figure of merit (TDFOM) at TP2**
Expected response	The mean value of TDFOM measured shall be within the limits specified in IEEE 802.3cz:2023, 166.6.4.8.
Remarks	N/A

Table 44 specifies the PHY-level conformance test case PLCT_4_OMA_outer for measuring PUT transmitter optical parameters.

Table 44 — PLCT_4_OMA_outer — Optical transmitter measurements

Item	Content
Number – Title	**PLCT_4_OMA_outer — Optical PUT transmitter outer optical modulation amplitude (OMAouter) output at TP2**
Purpose	This test case determines the PUT outer optical modulation amplitude at TP2 and checks that it is in the expected range.
Reference	IEEE 802.3cz:2023, 166.6.4.4 and OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.3.
Prerequisites	IUT shall provide access to the interfaces specified in 4.2. TDFOM shall be measured before OMA outer. OMA outer shall be the second parameter measured in the OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.3 test group.
Set-up	OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.3, Figure 6.
Step	According to OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.3.2.
Iterations	Perform iterations with test case conditions T and U as specified in Table 11.
Expected response	Outer OMA values shall be in the range specified in IEEE 802.3cz:2023, 166.6.4.4.

Item	Content
Number – Title	**PLCT_4_OMA_outer — Optical PUT transmitter outer optical modulation amplitude (OMAouter) output at TP2**
Remarks	N/A

Table 45 specifies the PHY-level conformance test case PLCT_5_wavelength for measuring PUT transmitter optical parameters.

Table 45 — PLCT_5_wavelength — Optical transmitter measurements

Item	Content
Number – Title	**PLCT_5_wavelength — Optical PUT transmitter center wavelength and RMS spectral width at TP2**
Purpose	This test case determines the PUT the center wavelength and RMS spectral width at TP2 and checks that they are in the expected range.
Reference	IEEE 802.3cz:2023, 166.6.4.2 and OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.1.
Prerequisites	IUT shall provide access to the interfaces specified in 4.2.
Set-up	OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.1, Figure 3.
Step	According to OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.1.2
Iterations	Perform iterations with test case conditions T and U as specified in Table 11.
Expected response	Center wavelength and RMS spectral width are in the range specified in IEEE 802.3cz:2023, 166.6.4.2.
Remarks	N/A

Table 46 specifies the PHY-level conformance test case PLCT_6_uncorrelated_jitter for measuring PUT transmitter optical parameters.

Table 46 — PLCT_6_uncorrelated_jitter — Optical transmitter measurements

Item	Content
Number – Title	**PLCT_6_uncorrelated_jitter — Optical PUT transmitter uncorrelated random jitter at TP2**
Purpose	This test case determines the PUT uncorrelated random jitter at TP2 and checks that it is in the expected range.
Reference	IEEE 802.3cz:2023, 166.6.4.7 and OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.3.
Prerequisites	PUT shall provide access to the interfaces specified in 4.2. TDFOM and Outer OMA measurements shall have been completed in the OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.3 test group.
Set-up	OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.3, Figure 6.
Step	According to OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.3.2
Iterations	Perform iterations with test case conditions T and U as specified in Table 11.
Expected response	Uncorrelated jitter obtained shall be in the range specified in IEEE 802.3cz:2023, 166.6.4.7 and Table 166-9.
Remarks	N/A

Table 47 specifies the PHY-level conformance test case PLCT_7_ER for measuring IUT transmitter optical parameters.

Table 47 — PLCT_7_ER — Optical transmitter measurements

Item	Content
Number – Title	**PLCT_7_ER — Optical PUT transmitter extintion ratio (ER) at TP2**
Purpose	This test case determines the PUT ER at TP2 and checks that it is in the expected range.

Item	Content
Number – Title	**PLCT_7_ER — Optical PUT transmitter extintion ratio (ER) at TP2**
Reference	IEEE 802.3cz:2023, 166.6.4.5 and OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.3.
Prerequisites	TDFOM and Outer OMA measurements must have been completed in the OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.3 test group.
Set-up	OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.3, Figure 6.
Step	According to OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.3.2
Iterations	Perform iterations with test case conditions T and U as specified in Table 11.
Expected response	ER obtained shall be in the range specified in IEEE 802.3cz:2023, Table 166-9.
Remarks	N/A

Table 48 specifies the PHY-level conformance test case PLCT_8_optical_return_loss for measuring PUT transmitter optical parameters.

Table 48 — PLCT_8_optical_return_loss — Optical transmitter measurements

Item	Content
Number – Title	**PLCT_8_optical_return_loss — Optical IUT return loss at TP2**
Purpose	This test case determines the PUT return loss at TP2 and checks that they are in the expected range.
Reference	IEEE 802.3cz:2023, 166.6.3.2 and Table 166-9.
Prerequisites	IUT shall provide access to the interfaces specified in 4.2.

Item	Content
Number – Title	**PLCT_8_optical_return_loss — Optical IUT return loss at TP2**
Set-up	OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.5, Figure 8.
Step	According to OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.5.2.
Iterations	Perform iterations with test case conditions T and U as specified in Table 11.
Expected response	Optical return loss obtained shall be greater than the limit specified in IEEE 802.3cz:2023, Table 166-9.
Remarks	N/A

Table 49 specifies the PHY-level conformance test case PLCT_9_RIN for measuring PUT transmitter optical parameters.

Table 49 — PLCT_9_RIN — Optical transmitter measurements

Item	Content
Number – Title	**PLCT_9_RIN — Optical PUT transmitter RIN at TP2**
Purpose	This test case determines the PUT $RIN_{12}OMA$ at TP2 and checks that it is in the expected range.
Reference	IEEE 802.3cz:2023, 166.6.3.2 and Table 166-9.
Prerequisites	PUT shall provide access to the interfaces specified in 4.2.
Set-up	OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.3, Figure 6.
Step	According to OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.3.2.4.
Iterations	Perform iterations with test case conditions T and U as specified in Table 11.

Item	Content
Number – Title	**PLCT_9_RIN — Optical PUT transmitter RIN at TP2**
Expected response	$RIN_{12}OMA$ shall be below the limit specified IEEE 802.3cz:2023, Table 166-9.
Remarks	N/A

Table 49 specifies the PHY-level conformance test case PLCT_10_tx_clk_freq for measuring PUT transmitter optical parameters.

Table 50 — PLCT_10_tx_clk_freq— Optical transmitter measurements

Item	Content
Number – Title	**PLCT_10_tx_clk_freq—PUT transmitter clock frequency**
Purpose	This test case determines the PUT transmitter clock frequency at TP2 and checks that it is in the expected range of ±100 ppm.
Reference	IEEE 802.3cz:2023, 166.3.1, Table 166-1, 166.6.3.2 and Table 166-9.
Prerequisites	PUT shall provide access to the interfaces specified in 4.2. Waveform analyzer according to OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 11.1.6.
Set-up	OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.2, Figure 5.
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the IUT. 4. The TC shall wait 100 ms. 5. The UT shall write the IUT MDIO register bit 15 to bit 13 of the MDIO register 3.2348 with 100_2 (101_2 for 50GBASE-AU) 6. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 7. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2.

Item	Content
Number – Title	**PLCT_10_tx_clk_freq—PUT transmitter clock frequency**
	8. The TC shall measure the mean symbol rate of the waveform capturing at least 10,000 symbols at the maximum rate allowed by the waveform analyzer.
Iterations	Perform iterations with test case conditions T and U as specified in Table 11.
Expected response	The mean symbol rate is within the following range: • 50GBASE-AU: 26.55984375 Gbaud and 26.56515625 Gbaud • 25GBASE-AU: 26.55984375 Gbaud and 26.56515625 Gbaud • 10GBASE-AU: 10.6239375 Gbaud and 10.6260625 Gbaud • 5GBASE-AU: 5.31196875 Gbaud and 5.31303125 Gbaud • 2.5GBASE-AU: 2.655984375 Gbaud and 2.656515625 Gbaud
Remarks	N/A

14.3 Optical receiver measurements

Table 49 specifies the PHY-level conformance test case PLCT_11_rx_clk_freq for measuring PUT receiver clock frequency.

Table 51 — PLCT_11_rx_clk_freq — Optical receiver measurements

Item	Content
Number – Title	**PLCT_11_rx_clk_freq — PUT receiver clock frequency**
Purpose	This test case determines the PUT can properly accept incoming data with the nominal symbol rate ±100 ppm.
Reference	IEEE 802.3cz:2023, 166.6.3.2 and Table 166-10.
Prerequisites	PUT shall provide access to the interfaces specified in 4.2. Arbitrary waveform generator according to OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 11.2.1.4. Waveform to be used in the arbitrary waveform generator equivalent to the one generated by a reference transmitter set to BER test mode (Register 3.2348.15:13 equal to 001_2).
Set-up	OA Requirements for the Competence of Laboratories Testing Multi-Gigabit Optical Automotive Ethernet, 10.3.8, Figure 11.

Item	Content
Number – Title	**PLCT_11_rx_clk_freq — PUT receiver clock frequency**
Step	1. The TC shall set climatic chamber temperature T to the corresponding value for the current iteration. 2. The TC shall set IUT power supply voltage U to the corresponding value for the current iteration. 3. The TC shall power up the IUT. 4. The TC shall wait 100 ms. 5. The UT shall write the IUT MDIO register bit 15 to bit 13 of the MDIO register 3.2348 with 001_2. 6. The UT shall write the IUT MDIO register bit 15 of the MDIO register 1.0 with 1_2. 7. The TC shall wait till the IUT MDIO register bit 15 of the MDIO register 1.0 is equal to 0_2. 8. The transmit/monitoring station shall send $1.08x10^{13}$ bits with nominal symbol rate according to the PHY type (2.5, 5, 10, 25 or 50GBASE-AU) under test +100 ppm 9. The TC shall check that the bit error rate reported by the IUT is lower than 10^{-12} 10. The transmit/monitoring station shall send $1.08x10^{13}$ bits with nominal symbol rate according to the PHY type (2.5, 5, 10, 25 or 50GBASE-AU) under test -100 ppm 11. The TC shall check that the bit error rate reported by the IUT is lower than 10^{-12}
Iterations	Perform iterations with test case conditions T and U as specified in Table 11.
Expected response	Result of checks in step 9 and 11 shall be OK for all iterations.
Remarks	The resulting transmitted symbols in steps 8 and 10 shall be equivalent to the symbols generated by a PHY in BER test mode (MDIO register bit 15 to bit 13 of the MDIO register 3.2348 set to 001_2).